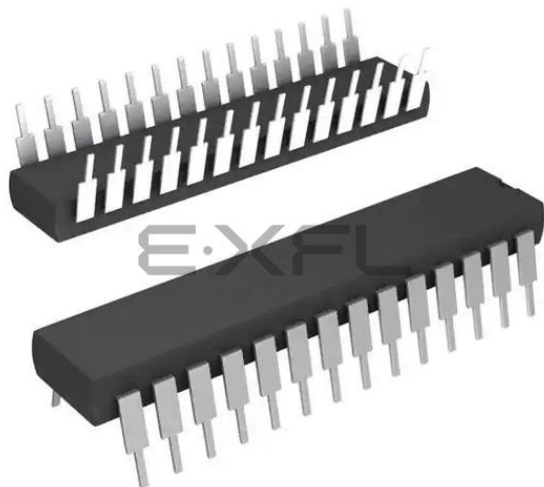




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323lsp2804g



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Table 10. AC Characteristics

T _A =0°C to +70°C 8.0MHz							Watch-Dog Timer Mode Register (D1, D0)
No	Symbol	Parameter	V _{CC}	Minimum	Maximum	Units	Notes
1	TpC	Input Clock Period	2.0–3.6	121	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–3.6		25	ns	1
3	TwC	Input Clock Width	2.0–3.6	37		ns	1
4	TwTinL	Timer Input Low Width	2.0 3.6	100 70		ns	1
5	TwTinH	Timer Input High Width	2.0–3.6	3TpC			1
6	TpTin	Timer Input Period	2.0–3.6	8TpC			1
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–3.6		100	ns	1
8	TwIL	Interrupt Request Low Time	2.0 3.6	100 70		ns	1, 2
9	TwIH	Interrupt Request Input High Time	2.0–3.6	5TpC			1, 2
10	Twsm	Stop-Mode Recovery Width Spec	2.0–3.6	12 10TpC		ns	3 4
11	Tost	Oscillator Start-Up Time	2.0–3.6		5TpC		4
12	Twdt	Watch-Dog Timer Delay Time	2.0–3.6 2.0–3.6 2.0–3.6 2.0–3.6	5 10 20 80		ms ms ms ms	0, 0 0, 1 1, 0 1, 1
13	T _{POR}	Power-On Reset	2.0–3.6	2.5	10	ms	

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. SMR – D5 = 1.
4. SMR – D5 = 0.

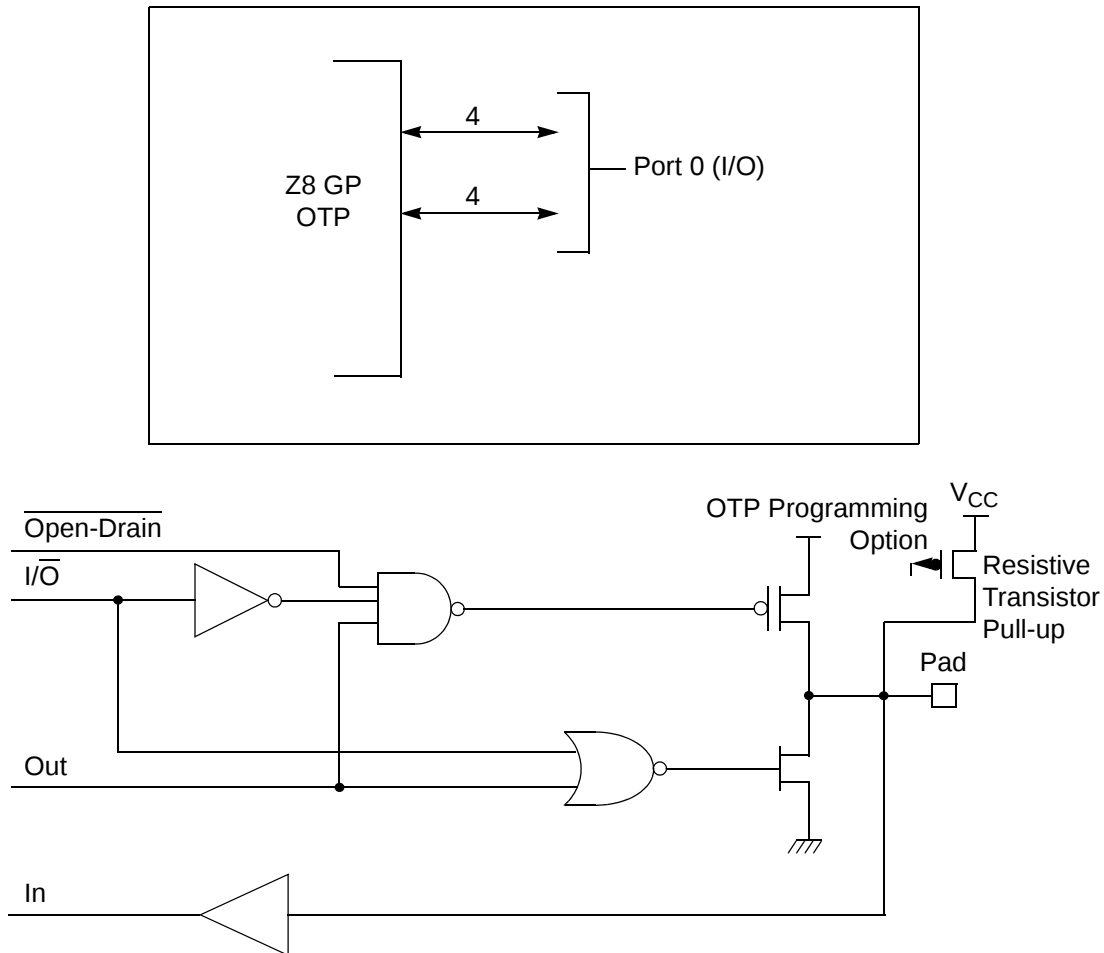


Figure 9. Port 0 Configuration

Port 1 (P17–P10)

Port 1 (see Figure 10) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

► **Note:** The Port 1 direction is reset to be input following an SMR.



ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

- **Note:** An expanded register bank is also referred to as an expanded register group (see Figure 15).

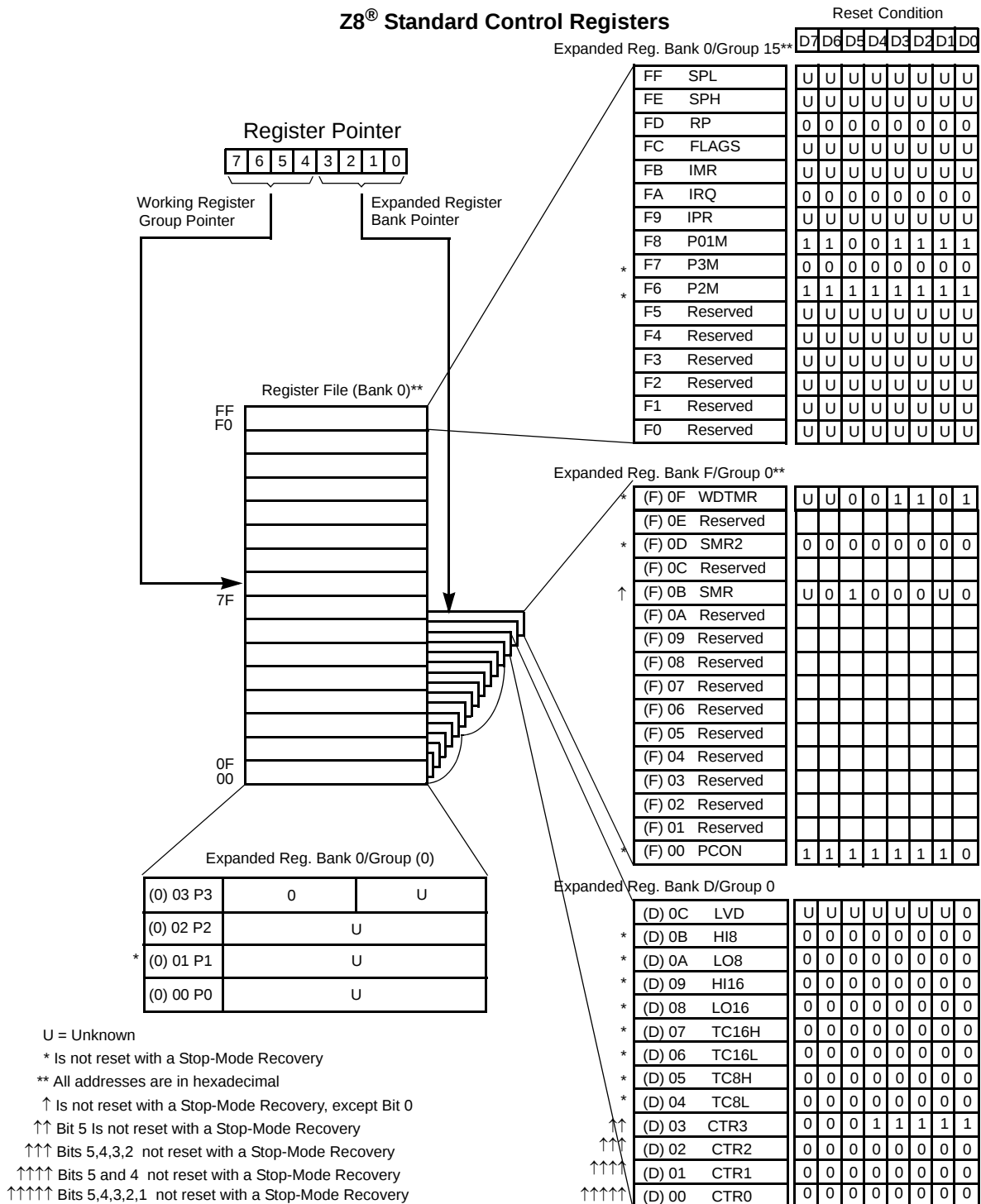


Figure 15. Expanded Register File Architecture

The counter/timers are mapped into ERF group D. Access is easily performed using the following:

```
LD          RP, #0Dh          ; Select ERF D
for access to bank D

                                ; (working
                                ; register group 0)
LD          R0, #xx          ; load CTRL0
LD          1, #xx          ; load CTRL1
LD          R1, 2            ; CTRL2→CTRL1

LD          RP, #0Dh          ; Select ERF D
for access to bank D

                                ; (working
                                ; register group 0)
LD          RP, #7Dh          ; Select
expanded register bank D and working ; register
group 7 of bank 0 for access.
LD          71h, 2
; CTRL2→register 71h
LD          R1, 2
; CTRL2→register 71h
```

Register File

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 12) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (Figure 17). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

- **Note:** Working register group E0–EF can only be accessed through working registers and indirect addressing modes.

T8/T16_Logic/Edge _Detect

In TRANSMIT Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION Mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter

In Transmit Mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to “NORMAL OPERATION Mode” terminates the “PING-PONG Mode” operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION Mode, this field defines the width of the glitch that must be filtered out.

Initial_T8_Out/Rising_Edge

In TRANSMIT Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

Initial_T16 Out/Falling _Edge

In TRANSMIT Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

- **Note:** Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/T16_OUT.

CTR2 Counter/Timer 16 Control Register—CTR2(D)02H

Table 14 lists and briefly describes the fields for this register.

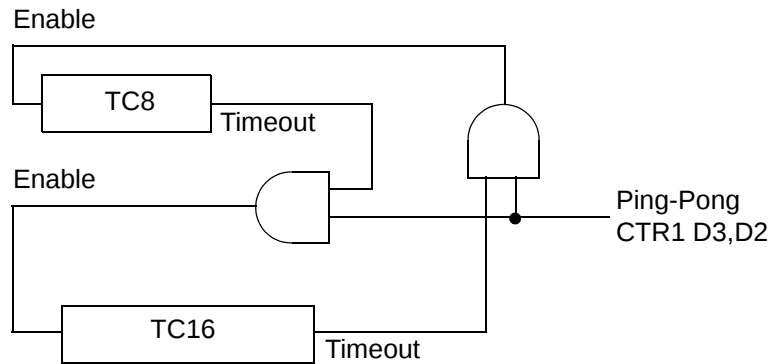


Figure 28. Ping-Pong Mode Diagram

Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the Ping-Pong mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See Figure 29.

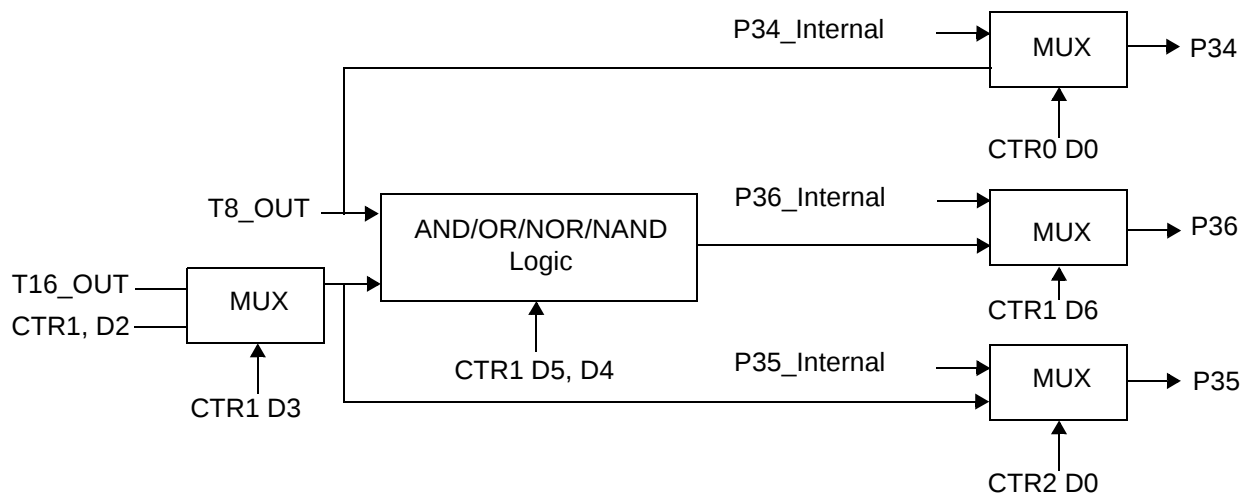


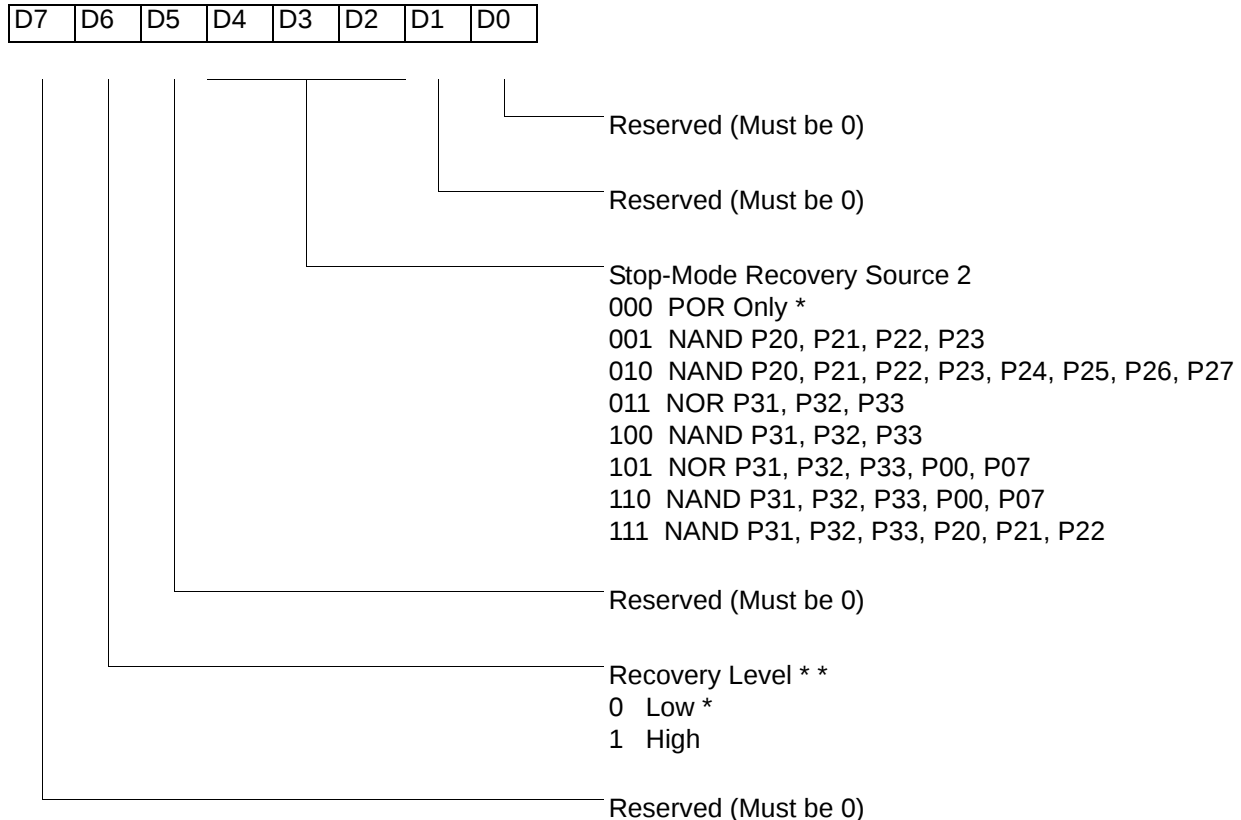
Figure 29. Output Circuit

The initial value of T8 or T16 must not be 1. Stopping the timer and restarting the timer reloads the initial value to avoid an unknown previous value.

Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (Figure 36).

SMR2(0F)DH



Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

* Default setting after reset

* * At the XOR gate input

Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.

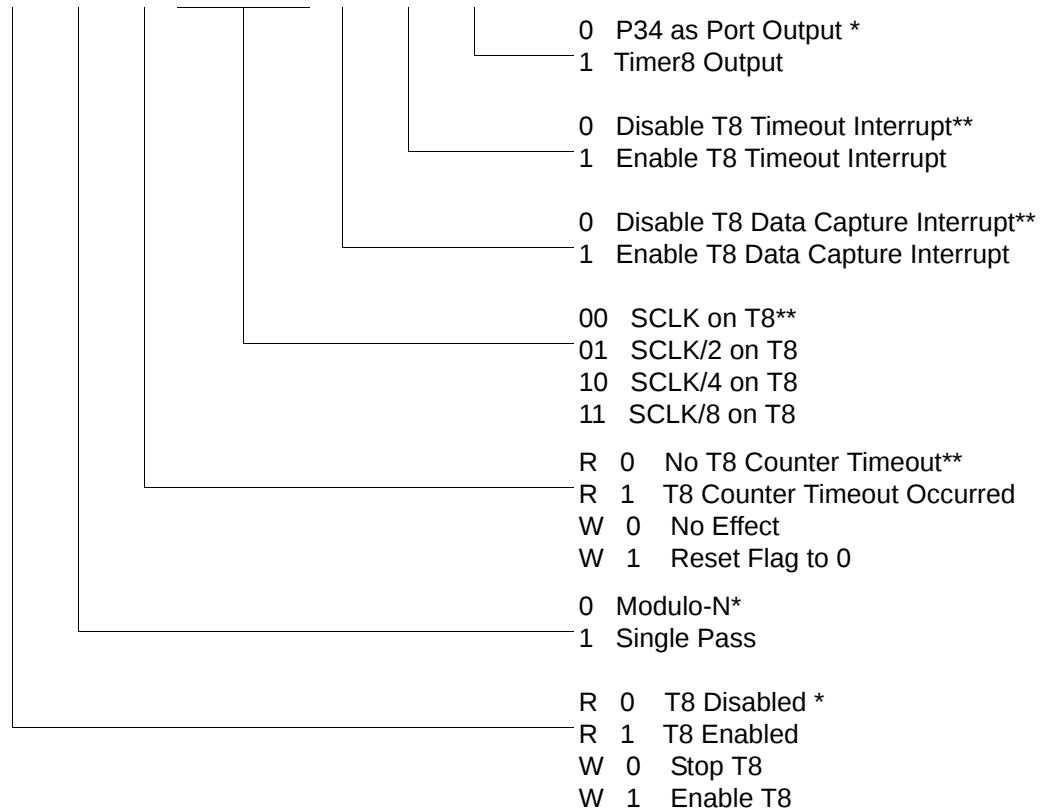
► **Note:** Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.

Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are depicted in Figure 39 through Figure 43.

CTR0(0D)00H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



* Default setting after reset

**Default setting after reset. Not reset with Stop Mode recovery.

Figure 39. TC8 Control Register ((0D)00H: Read/Write Except Where Noted)

CTR1(0D)01H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

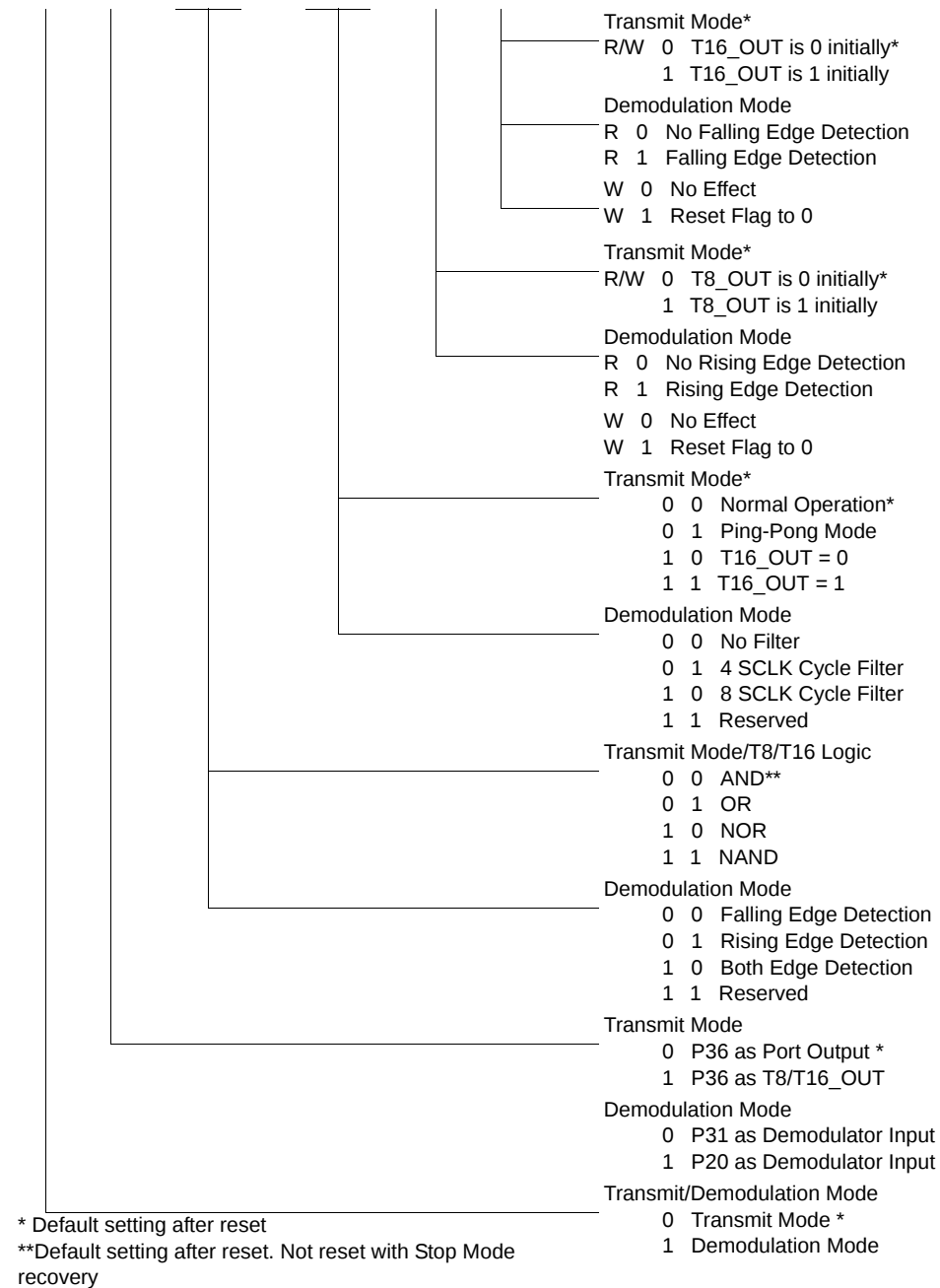
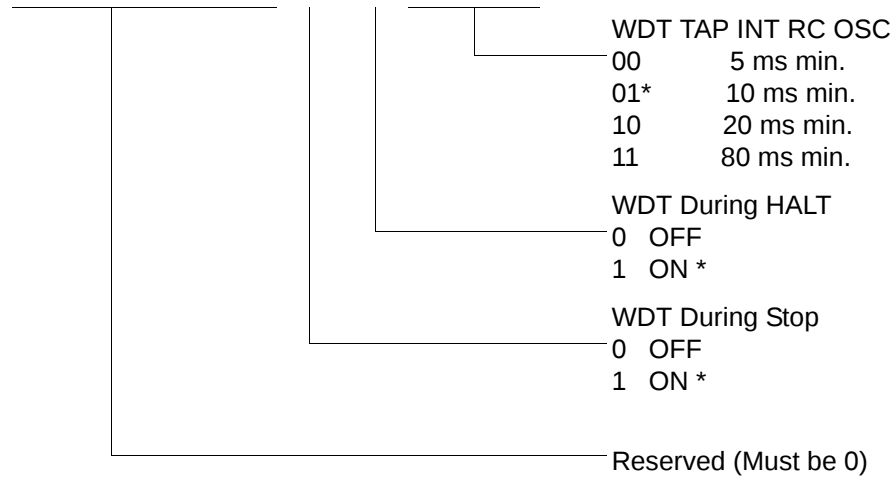


Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write)

WDTMR(0F)0FH

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



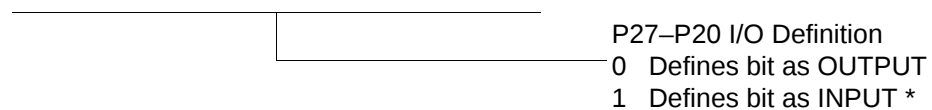
* Default setting after reset

Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)

Standard Control Registers

R246 P2M(F6H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

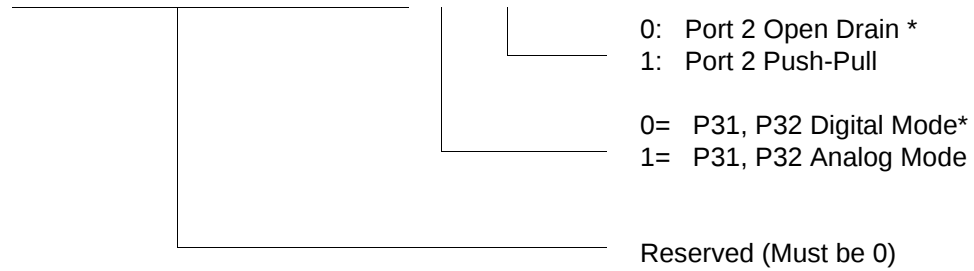


* Default setting after reset

Figure 48. Port 2 Mode Register (F6H: Write Only)

R247 P3M(F7H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



* Default setting after reset. Not reset with Stop Mode recovery.

Figure 49. Port 3 Mode Register (F7H: Write Only)

R252 Flags(FCH)

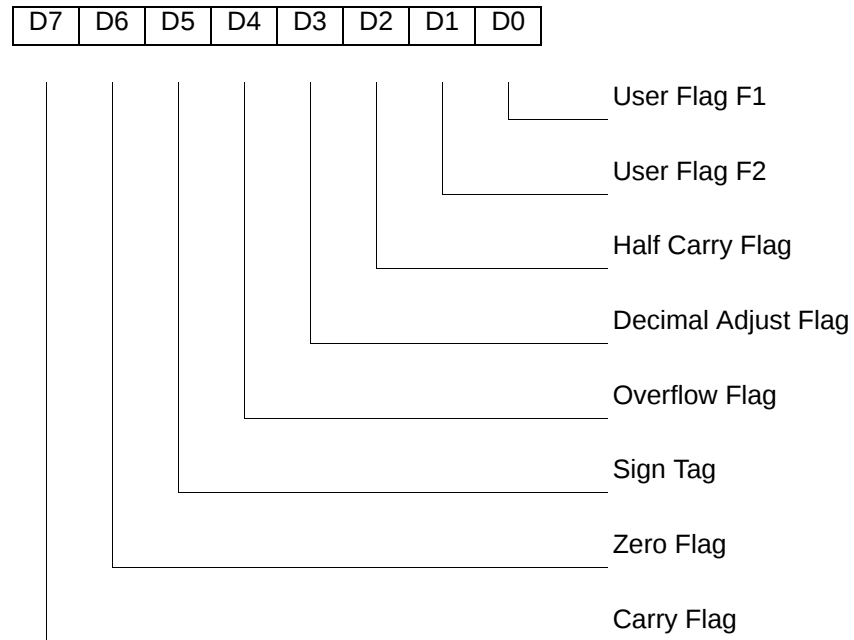
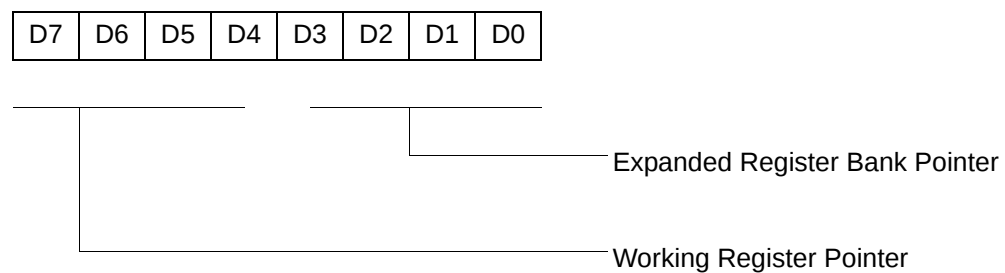


Figure 54. Flag Register (FCH: Read/Write)

R253 RP(FDH)



Default setting after reset = 0000 0000

Figure 55. Register Pointer (FDH: Read/Write)

R254 SPH(FEH)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

General-Purpose Register

Figure 56. Stack Pointer High (FEH: Read/Write)

R255 SPL(FFH)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Stack Pointer Low
Byte (SP7–SP0)

Figure 57. Stack Pointer Low (FFH: Read/Write)

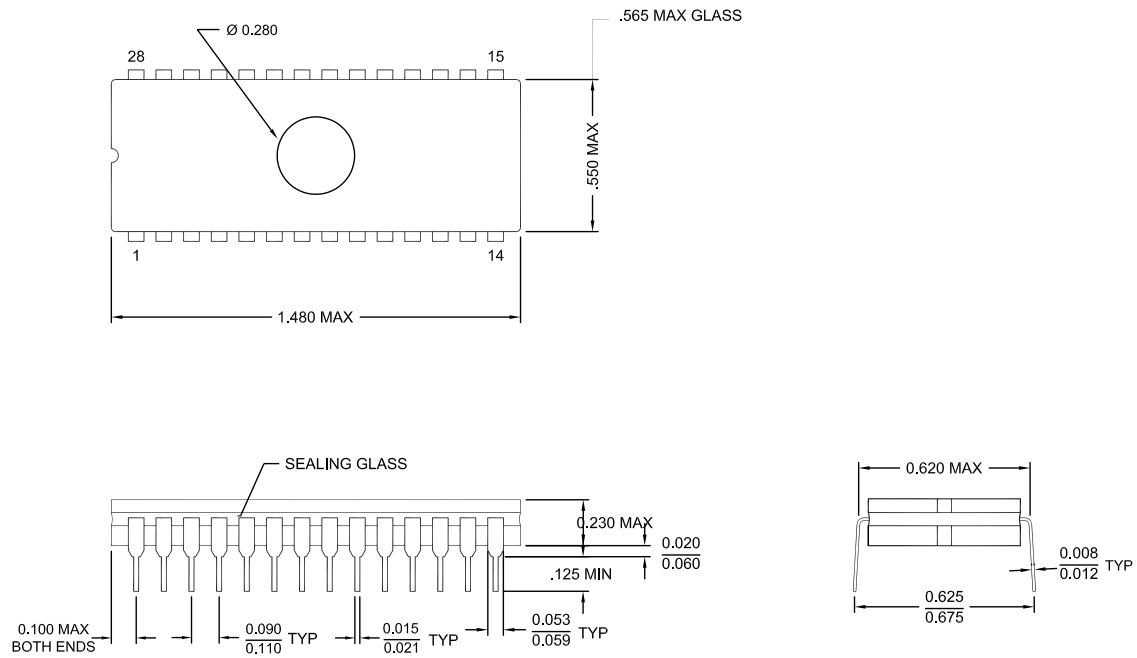


Figure 62. 28-Pin CDIP Package

Ordering Information

32KB Standard Temperature: 0° to +70°C			
Part Number	Description	Part Number	Description
ZGP323LSH4832C	48-pin SSOP 32K OTP	ZGP323LSS2832C	28-pin SOIC 32K OTP
ZGP323LSP4032C	40-pin PDIP 32K OTP	ZGP323LSH2032C	20-pin SSOP 32K OTP
ZGP323LSH2832C	28-pin SSOP 32K OTP	ZGP323LSP2032C	20-pin PDIP 32K OTP
ZGP323LSP2832C	28-pin PDIP 32K OTP	ZGP323LSS2032C	20-pin SOIC 32K OTP
ZGP323LSK2032E	20-pin CDIP 32K OTP	ZGP323LSK4032E	40-pin CDIP 32K OTP
		ZGP323LSK2832E	28-pin CDIP 32K OTP
32KB Extended Temperature: -40° to +105°C			
Part Number	Description	Part Number	Description
ZGP323LEH4832C	48-pin SSOP 32K OTP	ZGP323LES2832C	28-pin SOIC 32K OTP
ZGP323LEP4032C	40-pin PDIP 32K OTP	ZGP323LEH2032C	20-pin SSOP 32K OTP
ZGP323LEH2832C	28-pin SSOP 32K OTP	ZGP323LEP2032C	20-pin PDIP 32K OTP
ZGP323LEP2832C	28-pin PDIP 32K OTP	ZGP323LES2032C	20-pin SOIC 32K OTP
32KB Automotive Temperature: -40° to +125°C			
Part Number	Description	Part Number	Description
ZGP323LAH4832C	48-pin SSOP 32K OTP	ZGP323LAS2832C	28-pin SOIC 32K OTP
ZGP323LAP4032C	40-pin PDIP 32K OTP	ZGP323LAH2032C	20-pin SSOP 32K OTP
ZGP323LAH2832C	28-pin SSOP 32K OTP	ZGP323LAP2032C	20-pin PDIP 32K OTP
ZGP323LAP2832C	28-pin PDIP 32K OTP	ZGP323LAS2032C	20-pin SOIC 32K OTP
Note: Replace C with G for Lead-Free Packaging			



For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

Codes

ZG = ZiLOG General Purpose Family

P = OTP

323 = Family Designation

L = Voltage Range

2V to 3.6V

T = Temperature Range:

S = 0 to 70 degrees C (Standard)

E = -40 to +105 degrees C (Extended)

A = -40 to +125 degrees C (Automotive)

P = Package Type:

K = Windowed Cerdip

P = PDIP

H = SSOP

S = SOIC

= Number of Pins

CC = Memory Size

M = Packaging Options

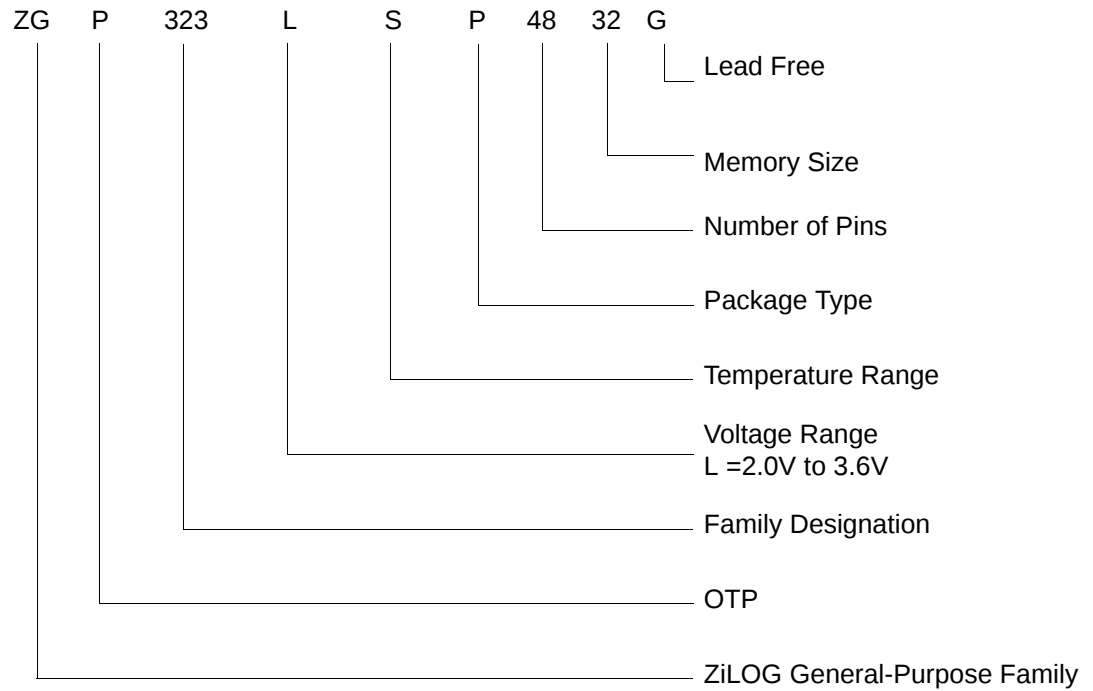
C = Non Lead-Free

G = Lead-Free

E = CDIP



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