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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323lsp4008c



List of Figures

Figure 1. Functional Block Diagram	3
Figure 2. Counter/Timers Diagram	4
Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration	5
Figure 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration	6
Figure 5. 40-Pin PDIP/CDIP* Pin Configuration	7
Figure 6. 48-Pin SSOP Pin Configuration	8
Figure 7. Test Load Diagram	10
Figure 8. AC Timing Diagram	14
Figure 9. Port 0 Configuration	17
Figure 10. Port 1 Configuration	18
Figure 11. Port 2 Configuration	19
Figure 12. Port 3 Configuration	20
Figure 13. Port 3 Counter/Timer Output Configuration	22
Figure 14. Program Memory Map (32K OTP)	24
Figure 15. Expanded Register File Architecture	26
Figure 16. Register Pointer	27
Figure 17. Register Pointer—Detail	29
Figure 18. Glitch Filter Circuitry	38
Figure 19. Transmit Mode Flowchart	39
Figure 20. 8-Bit Counter/Timer Circuits	40
Figure 21. T8_OUT in Single-Pass Mode	41
Figure 22. T8_OUT in Modulo-N Mode	41
Figure 23. Demodulation Mode Count Capture Flowchart	42
Figure 24. Demodulation Mode Flowchart	43
Figure 25. 16-Bit Counter/Timer Circuits	44
Figure 26. T16_OUT in Single-Pass Mode	45
Figure 27. T16_OUT in Modulo-N Mode	45
Figure 28. Ping-Pong Mode Diagram	47
Figure 29. Output Circuit	47
Figure 30. Interrupt Block Diagram	49
Figure 31. Oscillator Configuration	51
Figure 32. Port Configuration Register (PCON) (Write Only)	53
Figure 33. STOP Mode Recovery Register	55
Figure 34. SCLK Circuit	56

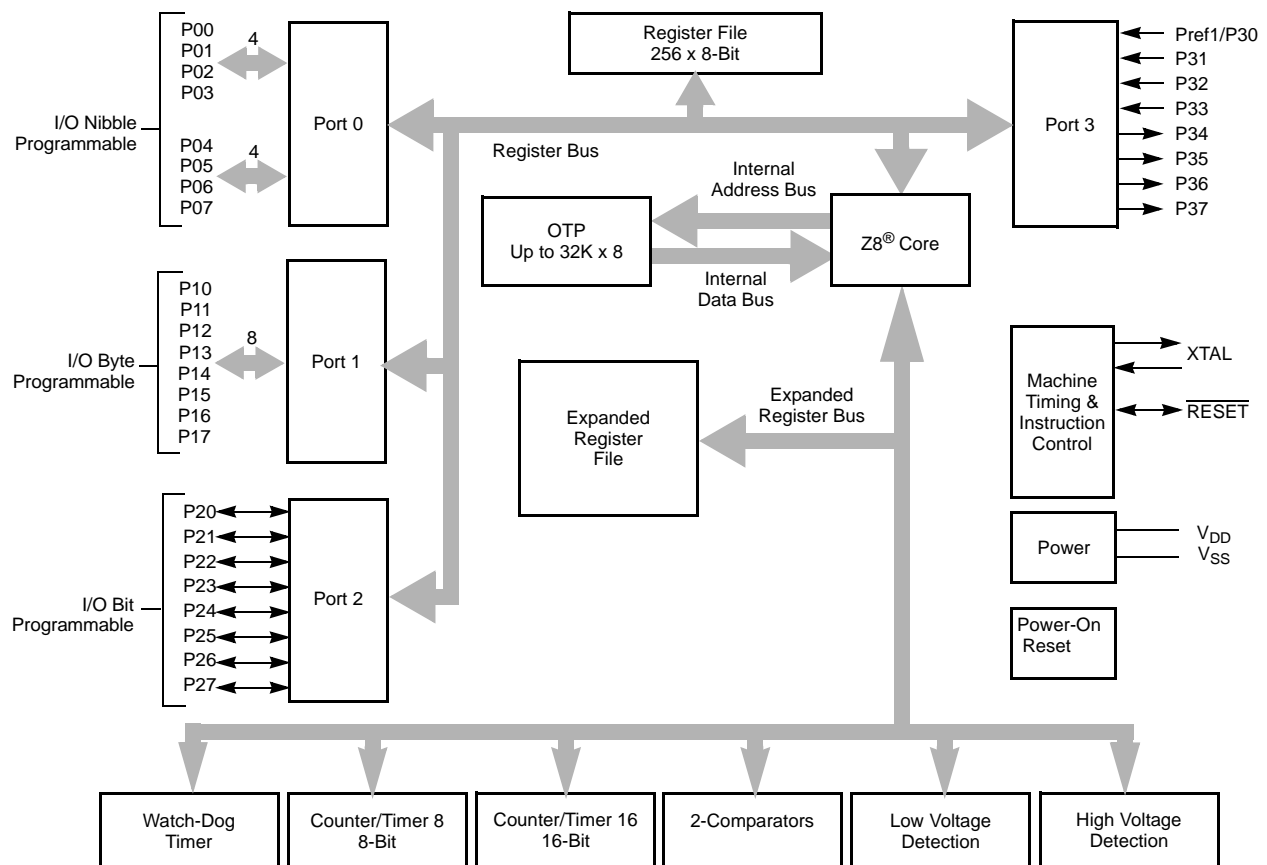


List of Tables

Table 1.	Features	1
Table 2.	Power Connections	3
Table 3.	20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification.....	5
Table 4.	28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification.....	6
Table 5.	40- and 48-Pin Configuration	8
Table 6.	Absolute Maximum Ratings	10
Table 7.	Capacitance	11
Table 8.	DC Characteristics	11
Table 9.	EPROM/OTP Characteristics	13
Table 10.	AC Characteristics	15
Table 11.	Port 3 Pin Function Summary	21
Table 12.	CTR0(D)00H Counter/Timer8 Control Register	31
Table 13.	CTR1(0D)01H T8 and T16 Common Functions.....	33
Table 14.	CTR2(D)02H: Counter/Timer16 Control Register.....	36
Table 15.	CTR3 (D)03H: T8/T16 Control Register	37
Table 16.	Interrupt Types, Sources, and Vectors.....	50
Table 17.	IRQ Register	50
Table 18.	SMR2(F)0DH:Stop Mode Recovery Register 2*	56
Table 19.	Stop Mode Recovery Source	58
Table 20.	Watch-Dog Timer Time Select	61
Table 21.	EPROM Selectable Options	62

Table 2. Power Connections

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram

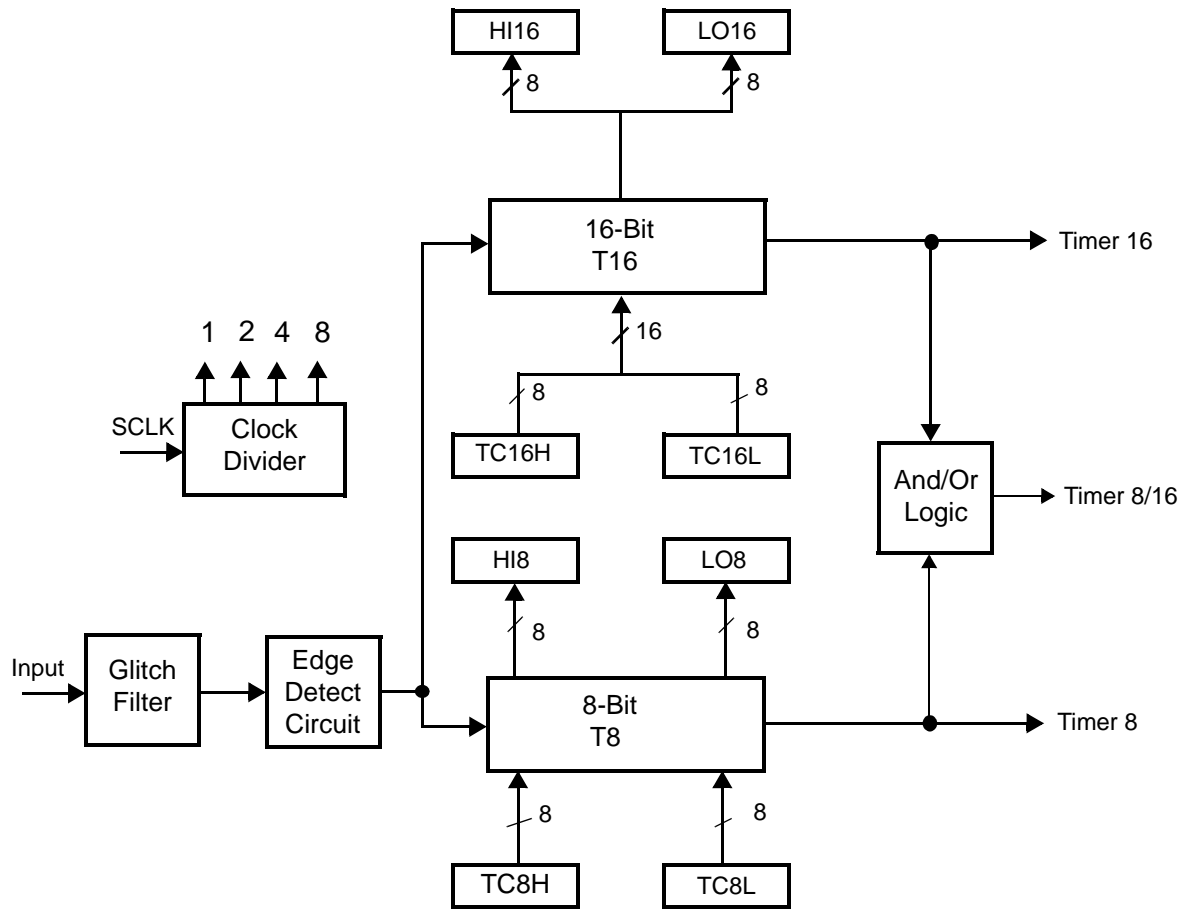


Figure 2. Counter/Timers Diagram

Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 3. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 4. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are illustrated in Figure 5, Figure 6, and described in Table 5.

For customer engineering code development, a UV eraseable windowed cerdip packaging is offered in 20-pin, 28-pin, and 40-pin configurations. ZiLOG does not recommend nor guarantee these packages for use in production.

Pin Functions

XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator output.

Port 0 (P07–P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

An optional pull-up transistor is available as a mask option on all Port 0 bits with nibble select.

- **Notes:** Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

The Port 0 direction is reset to be input following an SMR.



ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

- **Note:** An expanded register bank is also referred to as an expanded register group (see Figure 15).

In Demodulation Mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode on page 45.

Time_Out

This bit is set when T16 times out (terminal count reached). To reset the bit, write a 1 to this location.

T16_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask

This bit is set to allow an interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask

Set this bit to allow an interrupt when T16 times out.

P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

CTR3 T8/T16 Control Register—CTR3(D)03H

Table 15 lists and briefly describes the fields for this register. This register allows the T₈ and T₁₆ counters to be synchronized.

Table 15. CTR3 (D)03H: T8/T16 Control Register

Field	Bit Position		Value	Description
T ₁₆ Enable	7-----	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
T ₈ Enable	-6-----	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
Sync Mode	--5-----	R/W	0**	Disable Sync Mode
			1	Enable Sync Mode

into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFh (see Figure 23 and Figure 24).

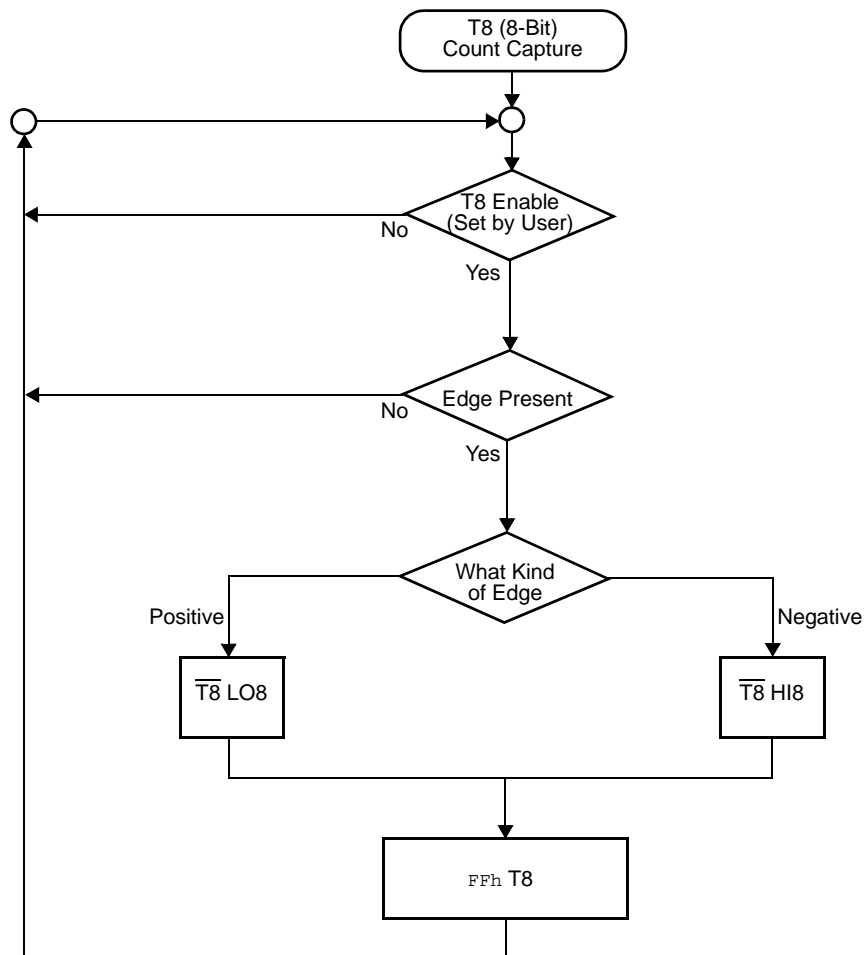


Figure 23. Demodulation Mode Count Capture Flowchart

T16 Transmit Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set. See Figure 25.

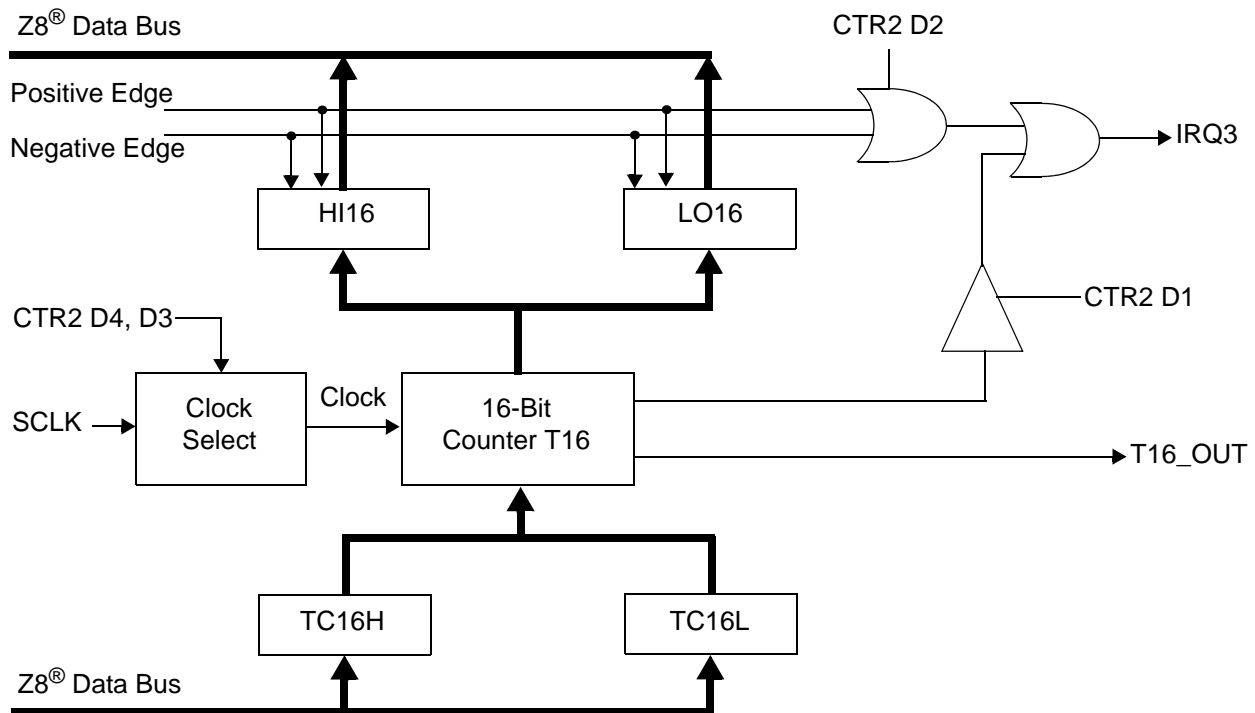


Figure 25. 16-Bit Counter/Timer Circuits

► **Note:** Global interrupts override this function as described in “Interrupts” on page 48.

If T16 is in SINGLE-PASS mode, it is stopped at this point (see Figure 26). If it is in Modulo-N Mode, it is loaded with TC16H * 256 + TC16L, and the counting continues (see Figure 27).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.

If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from `FFFFh`. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 28.

- **Note:** Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.

Table 16. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising, Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T _{IN}	4,5	External (P31), Rising, Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	T8	8,9	Internal
IRQ5	LVD	10,11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All Z8 GP™ OTP MCU Family interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable by the user. The software can poll to identify the state of the pin.

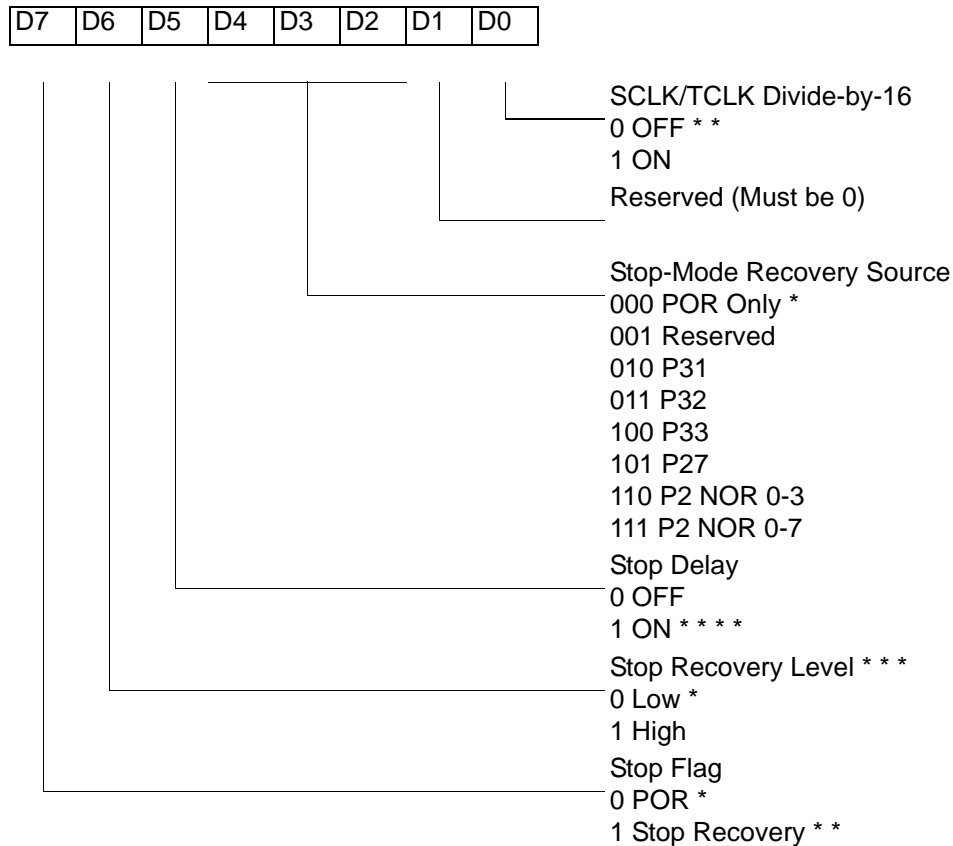
Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 17.

Table 17. IRQ Register

IRQ		Interrupt Edge	
D7	D6	IRQ2 (P31)	IRQ0 (P32)
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Note: F = Falling Edge; R = Rising Edge

SMR(0F)0BH



* Default after Power On Reset or Watch-Dog Reset

* * Set after STOP Mode Recovery

* * * At the XOR gate input

* * * * Default setting after reset. Must be 1 if using a crystal or resonator clock source.

Figure 33. STOP Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.

Table 19. Stop Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

- **Note:** Any Port 2 bit defined as an output drives the corresponding input to the default state. For example, if the NOR of P23-P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23-P21) form the NOR equation. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 59 for other recover sources.

Stop Mode Recovery Delay Select (D5)

This bit, if Low, disables the T_{POR} delay after Stop Mode Recovery. The default configuration of this bit is 1. If the “fast” wake up is selected, the Stop Mode Recovery source must be kept active for at least 5 T_{pC} .

- **Note:** It is recommended that this bit be set to 1 if using a crystal or resonator clock source. The T_{POR} delay allows the clock source to stabilize before executing instructions.

Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the device from Stop Mode. A 0 indicates Low level recovery. The default is 0 on POR.

Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery (SMR).

R252 Flags(FCH)

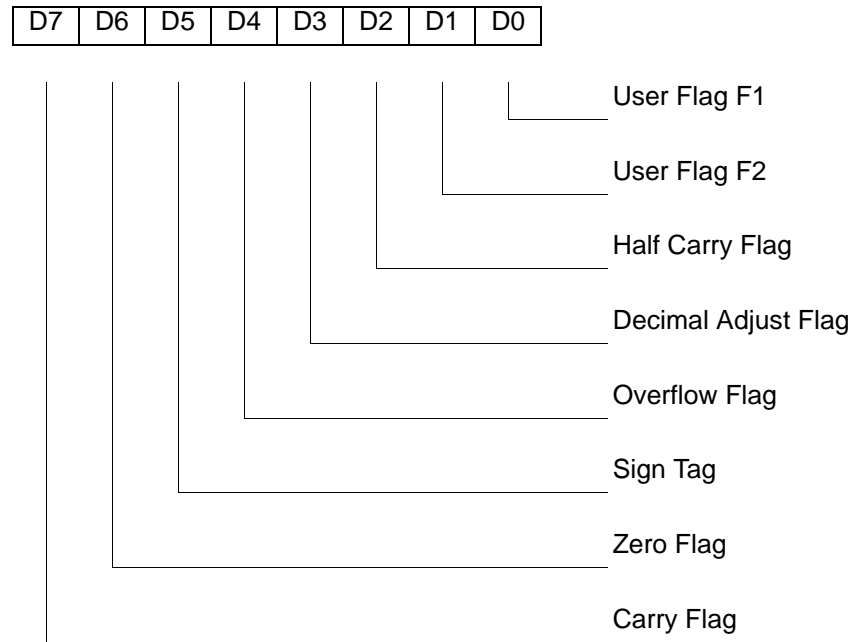
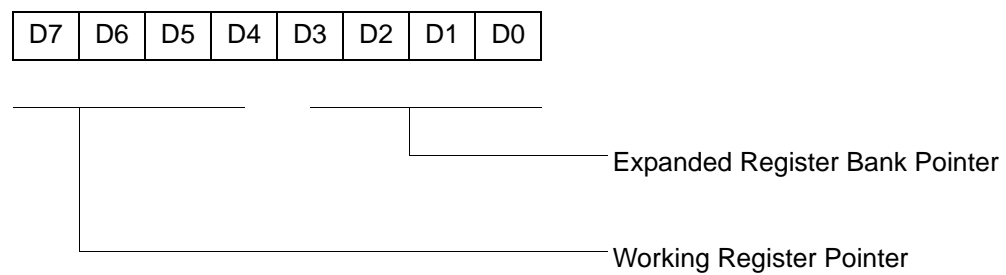


Figure 54. Flag Register (FCH: Read/Write)

R253 RP(FDH)



Default setting after reset = 0000 0000

Figure 55. Register Pointer (FDH: Read/Write)

R254 SPH(FEH)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

General-Purpose Register

Figure 56. Stack Pointer High (FEH: Read/Write)

R255 SPL(FFH)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Stack Pointer Low
Byte (SP7–SP0)

Figure 57. Stack Pointer Low (FFH: Read/Write)

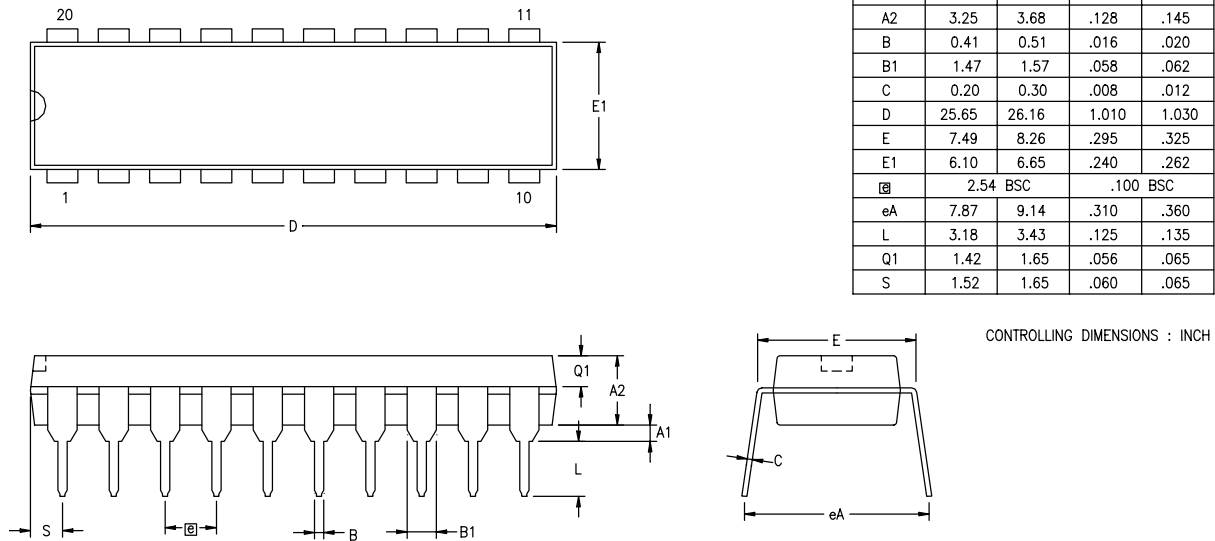


Figure 59. 20-Pin PDIP Package Diagram

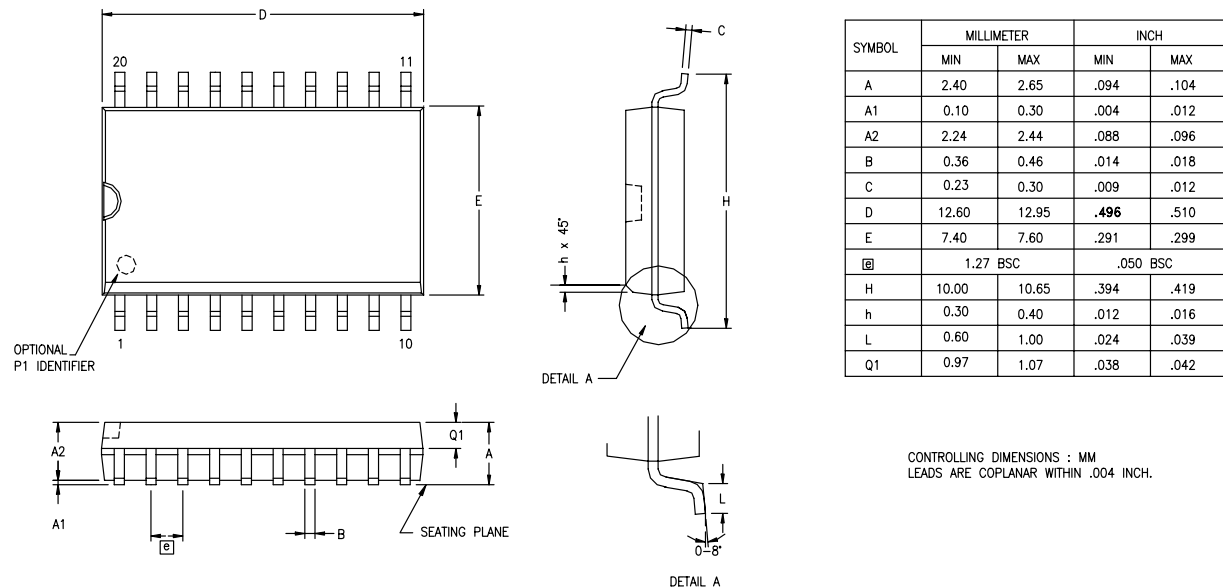


Figure 60. 20-Pin SOIC Package Diagram

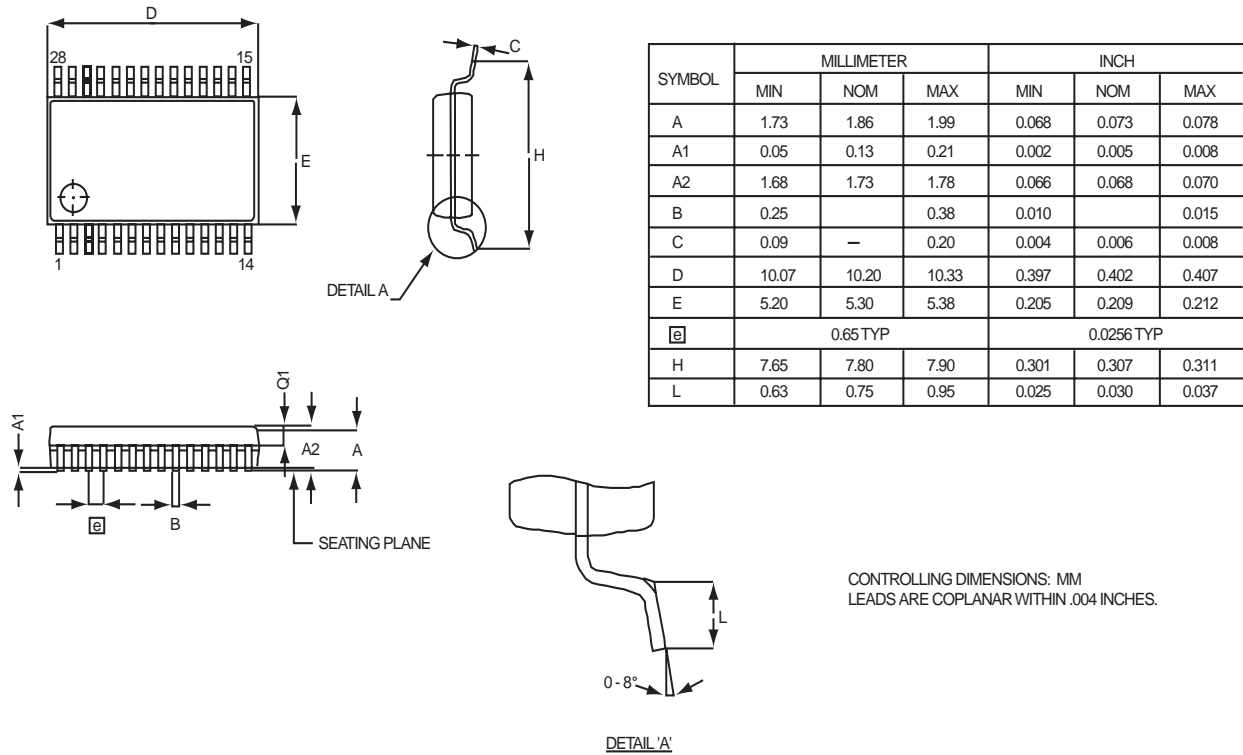


Figure 65. 28-Pin SSOP Package Diagram



16KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323LSH4816C	48-pin SSOP 16K OTP	ZGP323LSS2816C	28-pin SOIC 16K OTP
ZGP323LSP4016C	40-pin PDIP 16K OTP	ZGP323LSH2016C	20-pin SSOP 16K OTP
ZGP323LSH2816C	28-pin SSOP 16K OTP	ZGP323LSP2016C	20-pin PDIP 16K OTP
ZGP323LSP2816C	28-pin PDIP 16K OTP	ZGP323LSS2016C	20-pin SOIC 16K OTP

16KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323LEH4816C	48-pin SSOP 16K OTP	ZGP323LES2816C	28-pin SOIC 16K OTP
ZGP323LEP4016C	40-pin PDIP 16K OTP	ZGP323LES2016C	20-pin SOIC 16K OTP
ZGP323LEH2816C	28-pin SSOP 16K OTP	ZGP323LEH2016C	20-pin SSOP 16K OTP
ZGP323LEP2816C	28-pin PDIP 16K OTP	ZGP323LEP2016C	20-pin PDIP 16K OTP

16KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323LAH4816C	48-pin SSOP 16K OTP	ZGP323LAS2816C	28-pin SOIC 16K OTP
ZGP323LAP4016C	40-pin PDIP 16K OTP	ZGP323LAH2016C	20-pin SSOP 16K OTP
ZGP323LAH2816C	28-pin SSOP 16K OTP	ZGP323LAP2016C	20-pin PDIP 16K OTP
ZGP323LAP2816C	28-pin PDIP 16K OTP	ZGP323LAS2016C	20-pin SOIC 16K OTP

Note: Replace C with G for Lead-Free Packaging



For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

Codes

ZG = ZiLOG General Purpose Family

P = OTP

323 = Family Designation

L = Voltage Range

2V to 3.6V

T = Temperature Range:

S = 0 to 70 degrees C (Standard)

E = -40 to +105 degrees C (Extended)

A = -40 to +125 degrees C (Automotive)

P = Package Type:

K = Windowed Cerdip

P = PDIP

H = SSOP

S = SOIC

= Number of Pins

CC = Memory Size

M = Packaging Options

C = Non Lead-Free

G = Lead-Free

E = CDIP

D

DC characteristics 11
 demodulation mode
 count capture flowchart 42
 flowchart 43
 T16 45
 T8 41
 description
 functional 23
 general 2
 pin 4

E

EPROM
 selectable options 62
 expanded register file 24
 expanded register file architecture 26
 expanded register file control registers 69
 flag 78
 interrupt mask register 77
 interrupt priority register 76
 interrupt request register 77
 port 0 and 1 mode register 75
 port 2 configuration register 73
 port 3 mode register 74
 port configuration register 73
 register pointer 78
 stack pointer high register 79
 stack pointer low register 79
 stop-mode recovery register 71
 stop-mode recovery register 2 72
 T16 control register 67
 T8 and T16 common control functions register 65
 T8/T16 control register 68
 TC8 control register 64
 watch-dog timer register 73

F

features
 standby modes 1

functional description

counter/timer functional blocks 38
 CTR(D)01h register 33
 CTR0(D)00h register 31
 CTR2(D)02h register 35
 CTR3(D)03h register 37
 expanded register file 24
 expanded register file architecture 26
 HI16(D)09h register 30
 HI8(D)0Bh register 30
 L08(D)0Ah register 30
 L0I6(D)08h register 30
 program memory map 24
 RAM 23
 register description 63
 register file 28
 register pointer 27
 register pointer detail 29
 SMR2(F)0D1h register 38
 stack 29
 TC16H(D)07h register 30
 TC16L(D)06h register 31
 TC8H(D)05h register 31
 TC8L(D)04h register 31

G

glitch filter circuitry 38

H

halt instruction, counter/timer 52

I

input circuit 38
 interrupt block diagram, counter/timer 49
 interrupt types, sources and vectors 50

L

low-voltage detection register 63