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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323lsp4008g

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Table 8. DC Characteristics (Continued)

Symbol	Parameter	V_{CC}	Min	Typ	Max	Units	Conditions	Notes
		T_A= 0°C to +70°C						
I_{CC1}	Standby Current (HALT Mode)	2.0			3	mA	V_{IN} = 0V, V_{CC} at 8.0MHz	1, 2
		3.6			5		Same as above	1, 2
		2.0			2		Clock Divide-by-16 at 8.0MHz	1, 2
		3.6			4		Same as above	1, 2
I_{CC2}	Standby Current (Stop Mode)	2.0			8	μA	V_{IN} = 0 V, V_{CC} WDT is not Running	3
		3.6			10	μA	Same as above	3
		2.0			500	μA	V_{IN} = 0 V, V_{CC} WDT is Running	3
		3.6			800	μA	Same as above	3
I_{LV}	Standby Current (Low Voltage)				10	μA	Measured at 1.3V	4
V_{BO}	V_{CC} Low Voltage Protection				2.0	V	8MHz maximum Ext. CLK Freq.	
V_{LVD}	Vcc Low Voltage Detection			2.4		V		
V_{HVD}	Vcc High Voltage Detection			2.7		V		

Notes:
1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V_{CC} falls below V_{BO} limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to the V_{DD} and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.
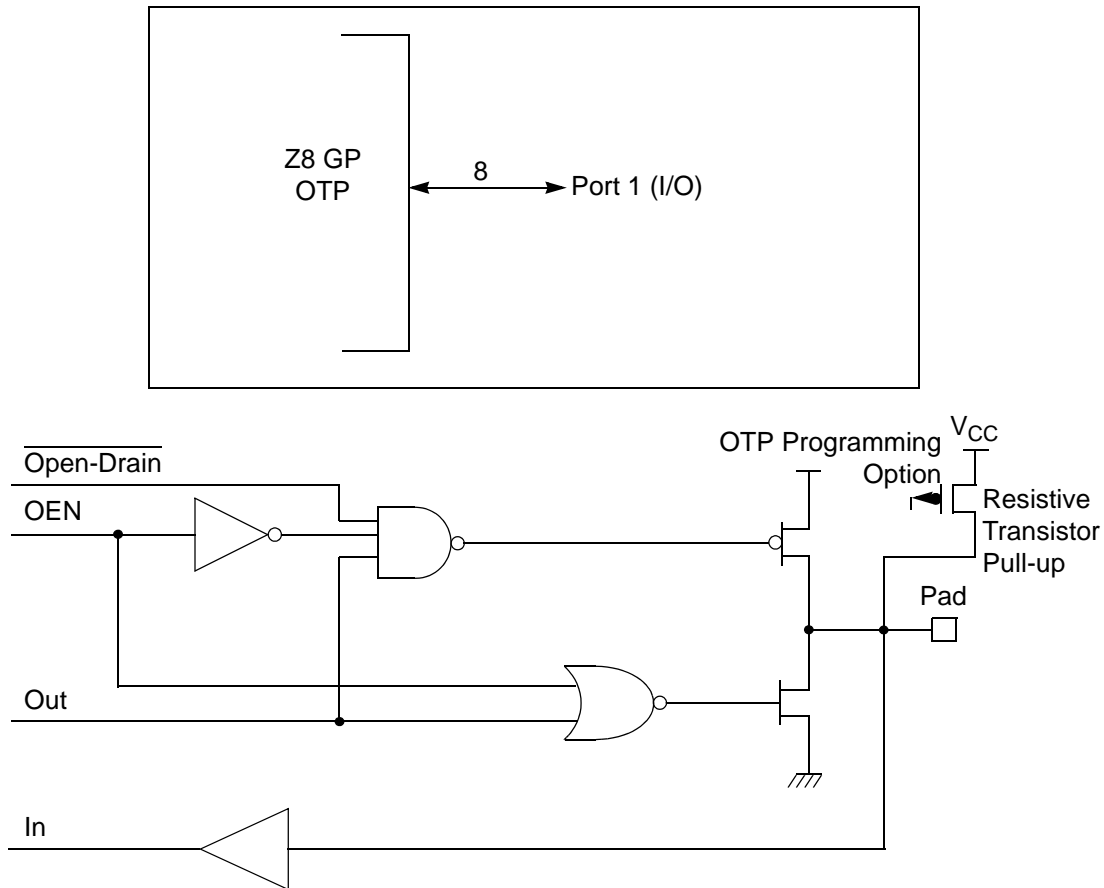
Figure 10. Port 1 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 11). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode.
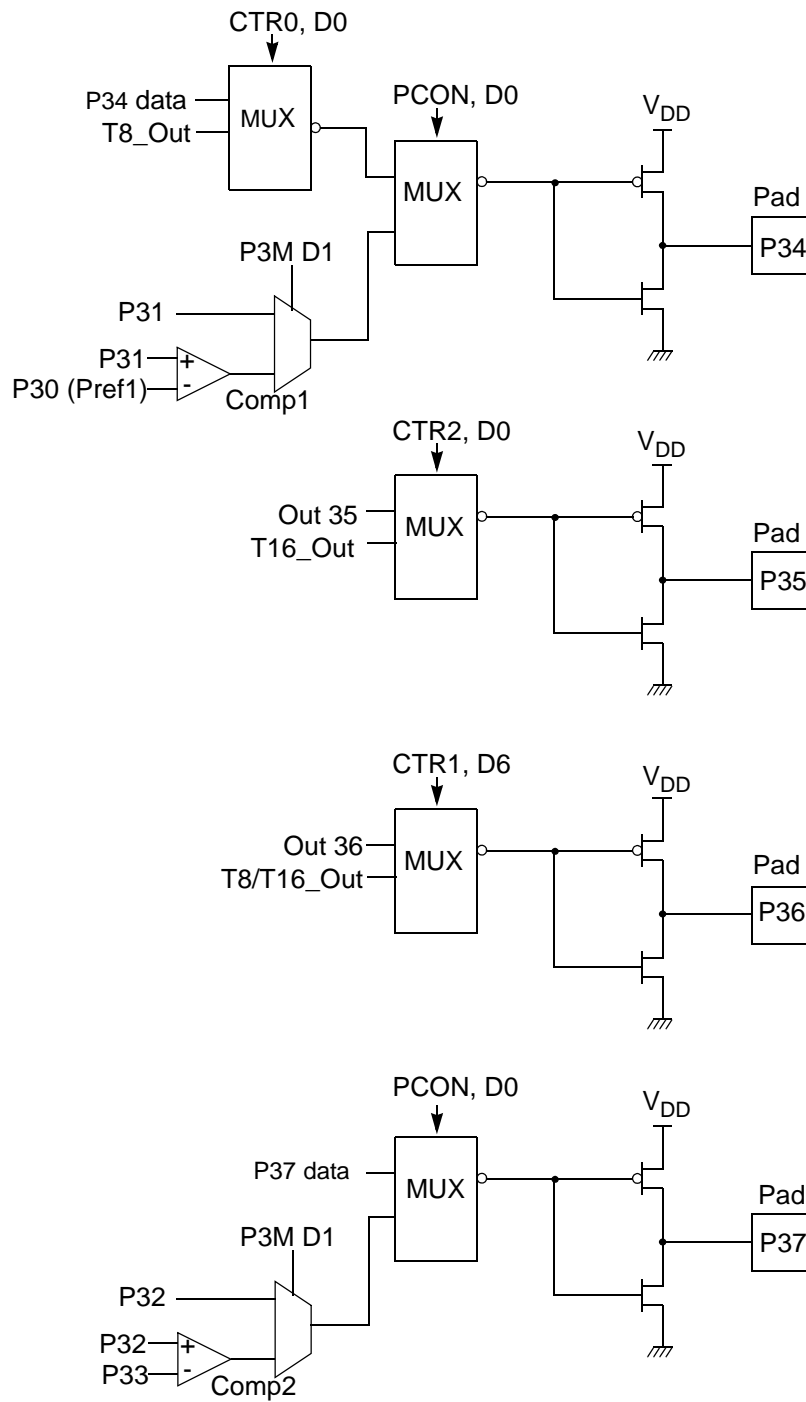
Figure 13. Port 3 Counter/Timer Output Configuration
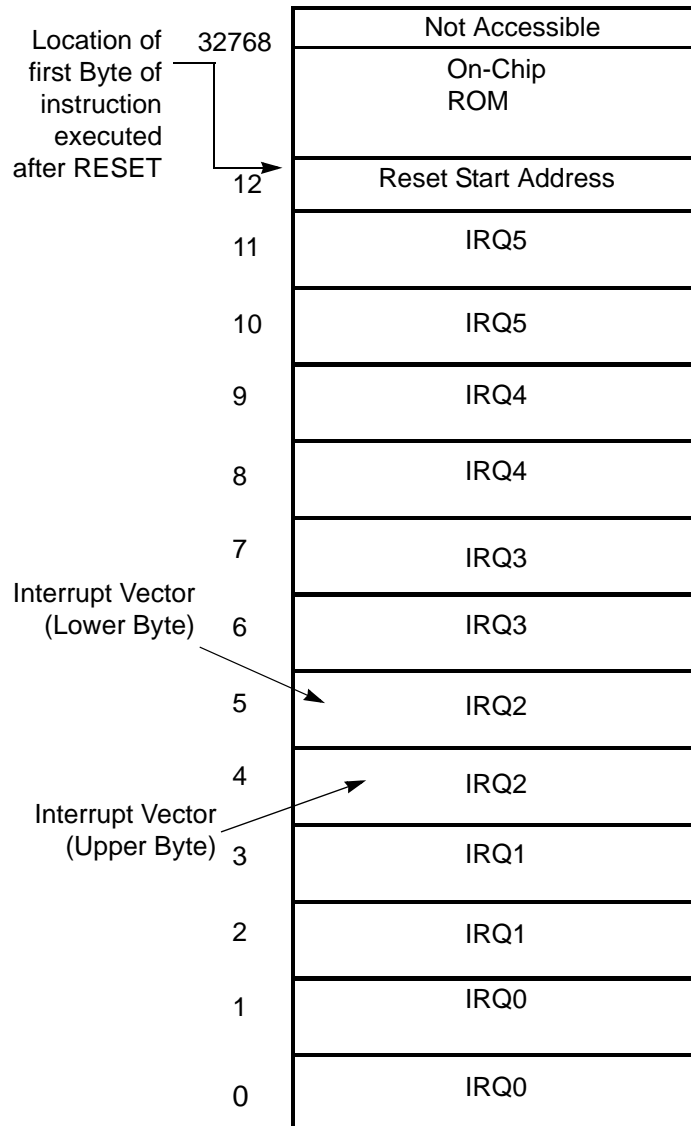
Figure 14. Program Memory Map (32K OTP)

Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8$^{®}$ register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the

Z8® Standard Control Registers

Register Pointer

7	6	5	4	3	2	1	0

Working Register Group Pointer

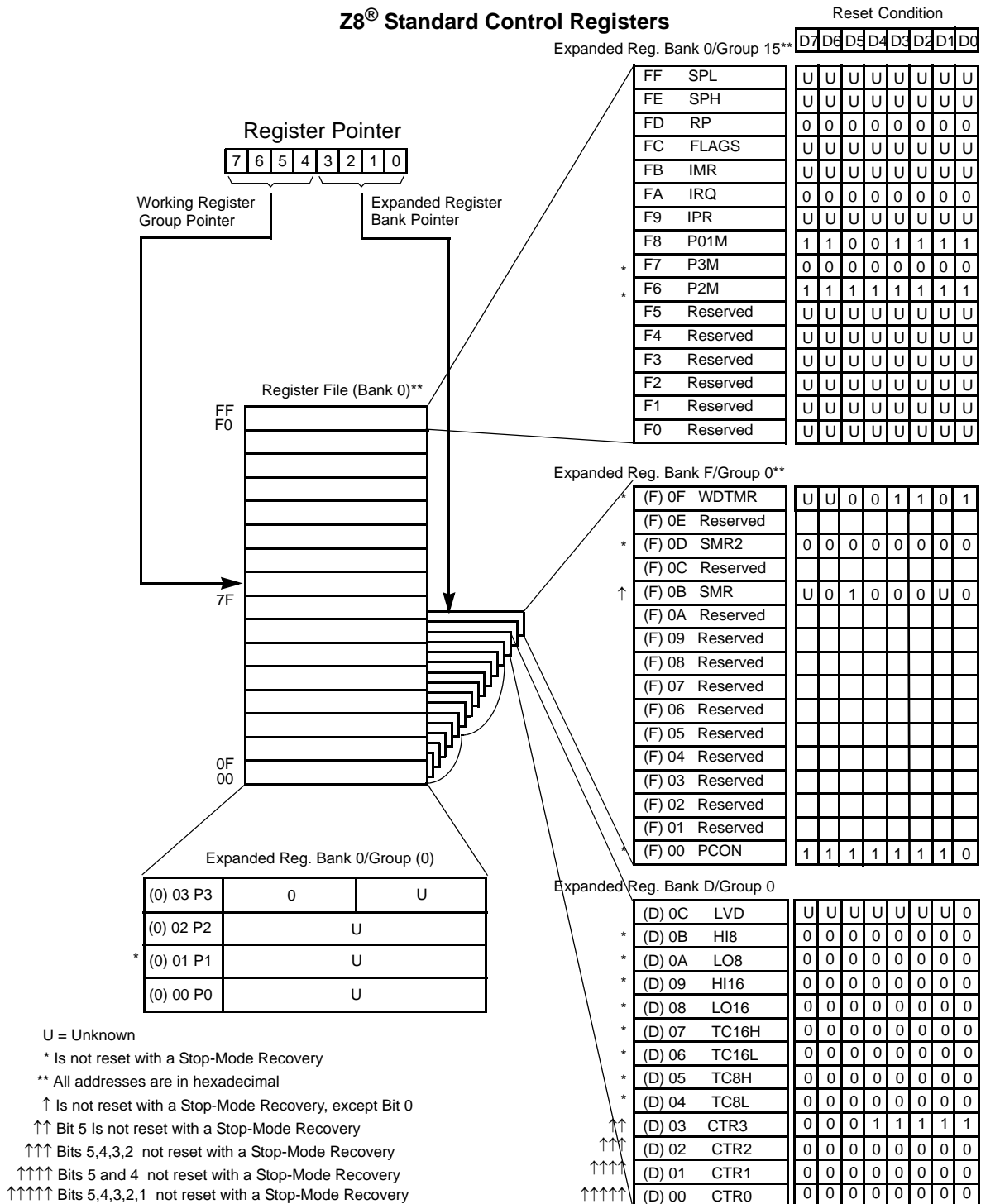Expanded Register Bank Pointer

Register File (Bank 0)**

FF
F0

7F

0F
00

Expanded Reg. Bank 0/Group 15**

Reset Condition

			D7	D6	D5	D4	D3	D2	D1	D0
	FF	SPL	U	U	U	U	U	U	U	U
	FE	SPH	U	U	U	U	U	U	U	U
	FD	RP	0	0	0	0	0	0	0	0
	FC	FLAGS	U	U	U	U	U	U	U	U
	FB	IMR	U	U	U	U	U	U	U	U
	FA	IRQ	0	0	0	0	0	0	0	0
	F9	IPR	U	U	U	U	U	U	U	U
	F8	P01M	1	1	0	0	1	1	1	1
*	F7	P3M	0	0	0	0	0	0	0	0
*	F6	P2M	1	1	1	1	1	1	1	1
	F5	Reserved	U	U	U	U	U	U	U	U
	F4	Reserved	U	U	U	U	U	U	U	U
	F3	Reserved	U	U	U	U	U	U	U	U
	F2	Reserved	U	U	U	U	U	U	U	U
	F1	Reserved	U	U	U	U	U	U	U	U
	F0	Reserved	U	U	U	U	U	U	U	U

Expanded Reg. Bank F/Group 0**

			D7	D6	D5	D4	D3	D2	D1	D0
*	(F) 0F	WDTMR	U	U	0	0	1	1	0	1
	(F) 0E	Reserved								
*	(F) 0D	SMR2	0	0	0	0	0	0	0	0
	(F) 0C	Reserved								
↑	(F) 0B	SMR	U	0	1	0	0	0	U	0
	(F) 0A	Reserved								
	(F) 09	Reserved								
	(F) 08	Reserved								
	(F) 07	Reserved								
	(F) 06	Reserved								
	(F) 05	Reserved								
	(F) 04	Reserved								
	(F) 03	Reserved								
	(F) 02	Reserved								
	(F) 01	Reserved								
*	(F) 00	PCON	1	1	1	1	1	1	1	0

Expanded Reg. Bank 0/Group (0)

	(0) 03 P3	0	U
	(0) 02 P2	U	
*	(0) 01 P1	U	
	(0) 00 P0	U	

U = Unknown

* Is not reset with a Stop-Mode Recovery

** All addresses are in hexadecimal

↑ Is not reset with a Stop-Mode Recovery, except Bit 0

↑↑ Bit 5 Is not reset with a Stop-Mode Recovery

↑↑↑ Bits 5,4,3,2 not reset with a Stop-Mode Recovery

↑↑↑↑ Bits 5 and 4 not reset with a Stop-Mode Recovery

↑↑↑↑↑ Bits 5,4,3,2,1 not reset with a Stop-Mode Recovery

Expanded Reg. Bank D/Group 0

			D7	D6	D5	D4	D3	D2	D1	D0
	(D) 0C	LVD	U	U	U	U	U	U	U	0
*	(D) 0B	HI8	0	0	0	0	0	0	0	0
*	(D) 0A	LO8	0	0	0	0	0	0	0	0
*	(D) 09	HI16	0	0	0	0	0	0	0	0
*	(D) 08	LO16	0	0	0	0	0	0	0	0
*	(D) 07	TC16H	0	0	0	0	0	0	0	0
*	(D) 06	TC16L	0	0	0	0	0	0	0	0
*	(D) 05	TC8H	0	0	0	0	0	0	0	0
*	(D) 04	TC8L	0	0	0	0	0	0	0	0
↑↑	(D) 03	CTR3	0	0	0	1	1	1	1	1
↑↑↑	(D) 02	CTR2	0	0	0	0	0	0	0	0
↑↑↑↑	(D) 01	CTR1	0	0	0	0	0	0	0	0
↑↑↑↑↑	(D) 00	CTR0	0	0	0	0	0	0	0	0

Figure 15. Expanded Register File Architecture

Counter/Timer2 LS-Byte Hold Register—TC16L(D)06H

Field	Bit Position		Description
T16_Data_LO	[7:0]	R/W	Data

Counter/Timer8 High Hold Register—TC8H(D)05H

Field	Bit Position		Description
T8_Level_HI	[7:0]	R/W	Data

Counter/Timer8 Low Hold Register—TC8L(D)04H

Field	Bit Position		Description
T8_Level_LO	[7:0]	R/W	Data

CTR0 Counter/Timer8 Control Register—CTR0(D)00H

Table 12 lists and briefly describes the fields for this register.

Table 12. CTR0(D)00H Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7-------	R/W	0* 1 0 1	Counter Disabled Counter Enabled Stop Counter Enable Counter
Single/Modulo-N	-6-------	R/W	0 1	Modulo-N Single Pass
Time_Out	--5------	R/W	0 1 0 1	No Counter Time-Out Counter Time-Out Occurred No Effect Reset Flag to 0
T8 _Clock	---43---	R/W	0 0 0 1 1 0 1 1	SCLK SCLK/2 SCLK/4 SCLK/8
Capture_INT_Mask	-----2--	R/W	0 1	Disable Data Capture Interrupt Enable Data Capture Interrupt

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 20.
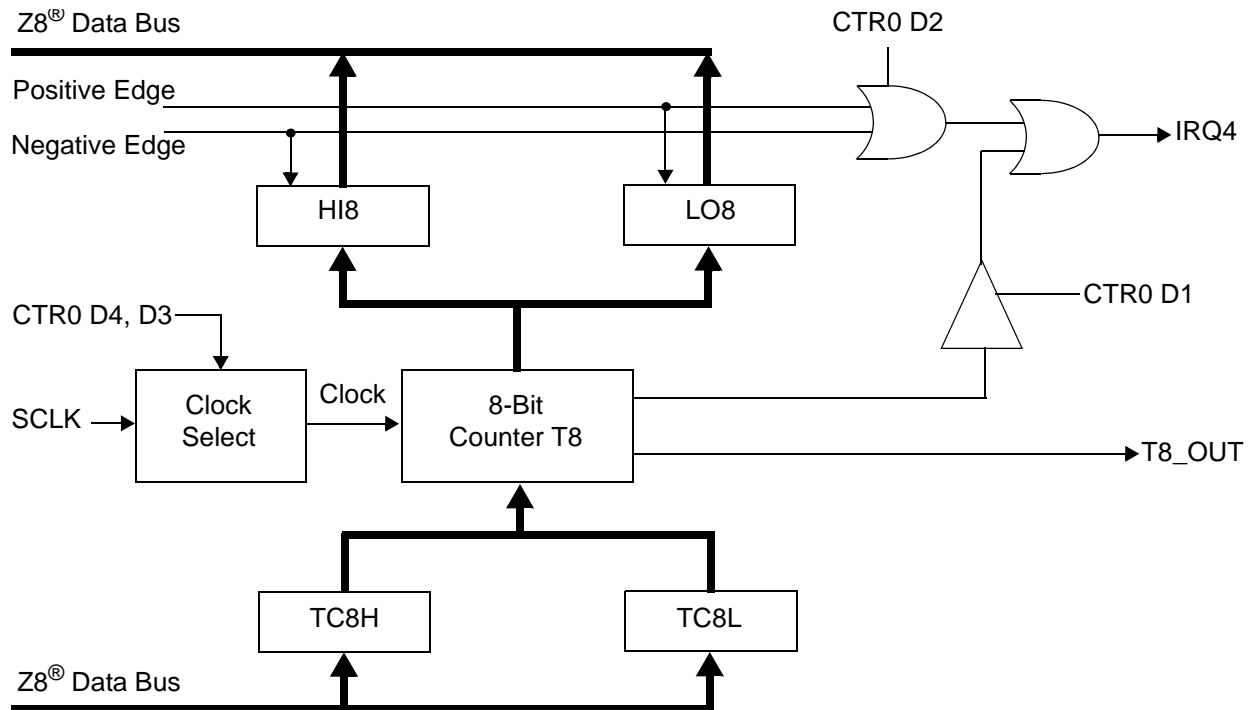

Figure 20. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.

⚠ **Caution:** To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. An initial count of 1 is not allowed (a non-function occurs). An initial count of 0 causes TC8 to count from 0 to FFH to FEH.
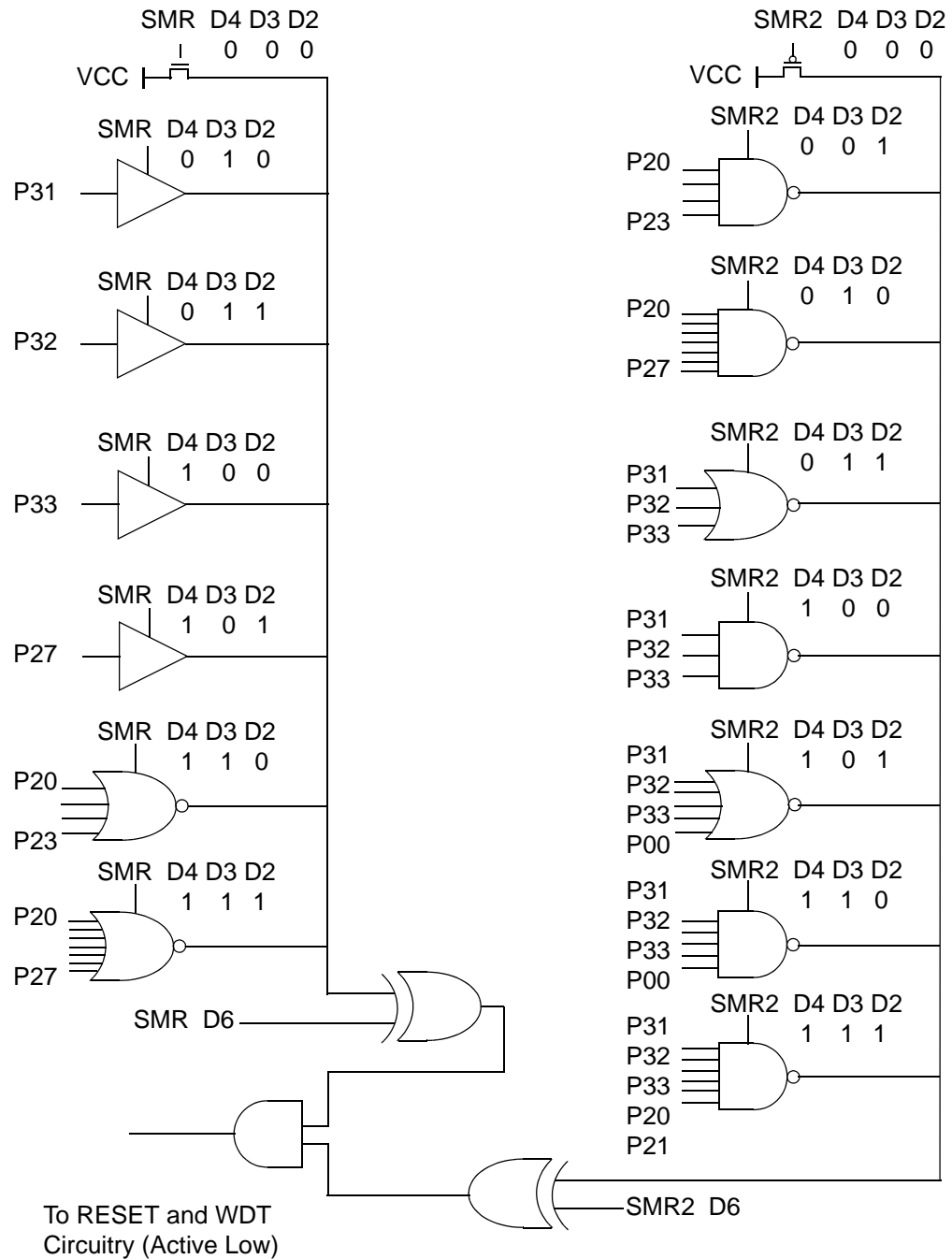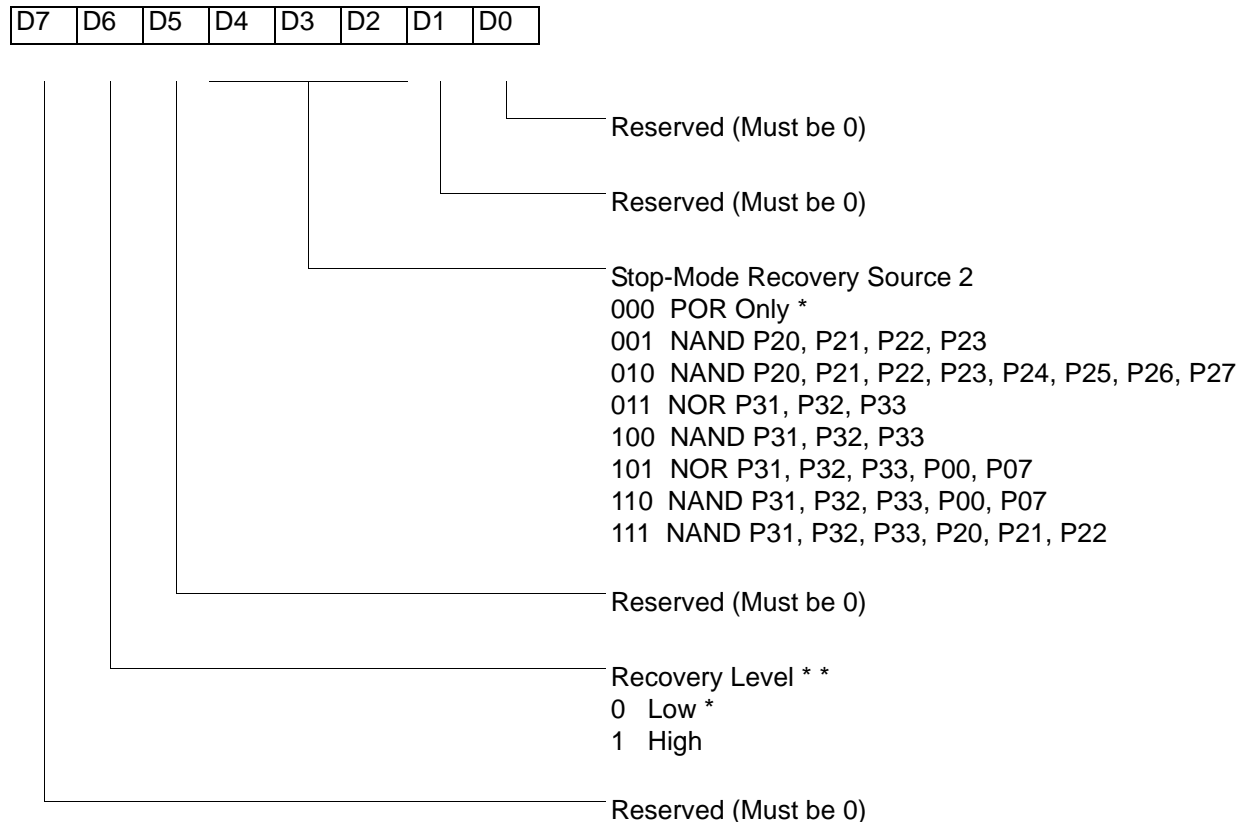
Figure 35. Stop Mode Recovery Source

Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (Figure 36).

SMR2(0F)DH

D7	D6	D5	D4	D3	D2	D1	D0

Reserved (Must be 0)

Reserved (Must be 0)

Stop-Mode Recovery Source 2
000 POR Only *
001 NAND P20, P21, P22, P23
010 NAND P20, P21, P22, P23, P24, P25, P26, P27
011 NOR P31, P32, P33
100 NAND P31, P32, P33
101 NOR P31, P32, P33, P00, P07
110 NAND P31, P32, P33, P00, P07
111 NAND P31, P32, P33, P20, P21, P22

Reserved (Must be 0)

Recovery Level * *
0 Low *
1 High

Reserved (Must be 0)

Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.
* Default setting after reset
* * At the XOR gate input

Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)

If SMR2 is used in conjunction with SMR, either of the specified events causes a
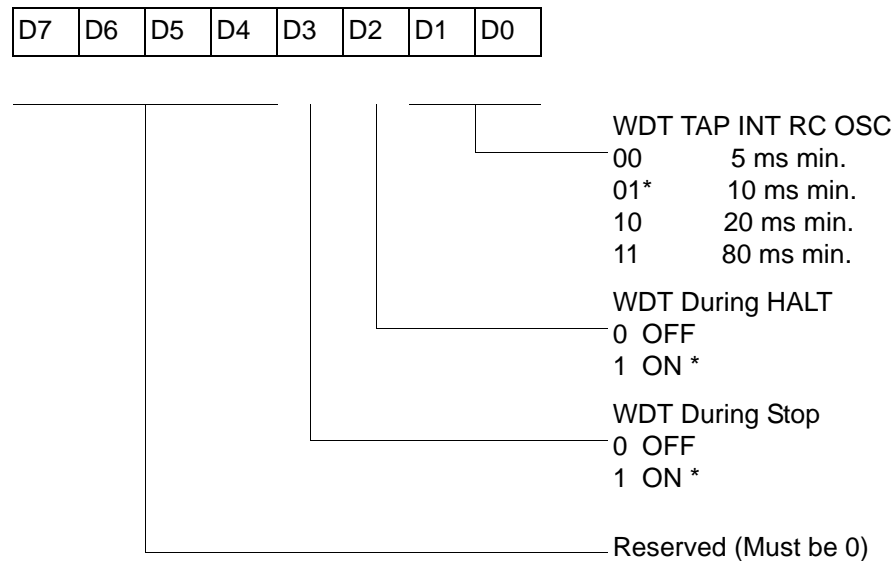Stop Mode Recovery.

Note: Port pins configured as outputs are ignored as an SMR or
SMR2 recovery source. For example, if the NAND or P23–P20
is selected as the recovery source and P20 is configured as an
output, the remaining SMR pins (P23–P21) form the NAND
equation.

Watch-Dog Timer Mode Register (WDTMR)

The Watch-Dog Timer (WDT) is a retriggerable one-shot timer that resets the Z8® CPU if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum timeout period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (Figure 37). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 36). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location `0Fh`. It is organized as shown in Figure 37.

WDTMR(0F)0Fh

D7	D6	D5	D4	D3	D2	D1	D0

WDT TAP INT RC OSC
00   5 ms min.
01*   10 ms min.
10   20 ms min.
11   80 ms min.

WDT During HALT
0 OFF
1 ON *

WDT During Stop
0 OFF
1 ON *

Reserved (Must be 0)

 * Default setting after reset

Figure 37. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as indicated in Table 20.

Notes: Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.

R249 IPR(F9H)

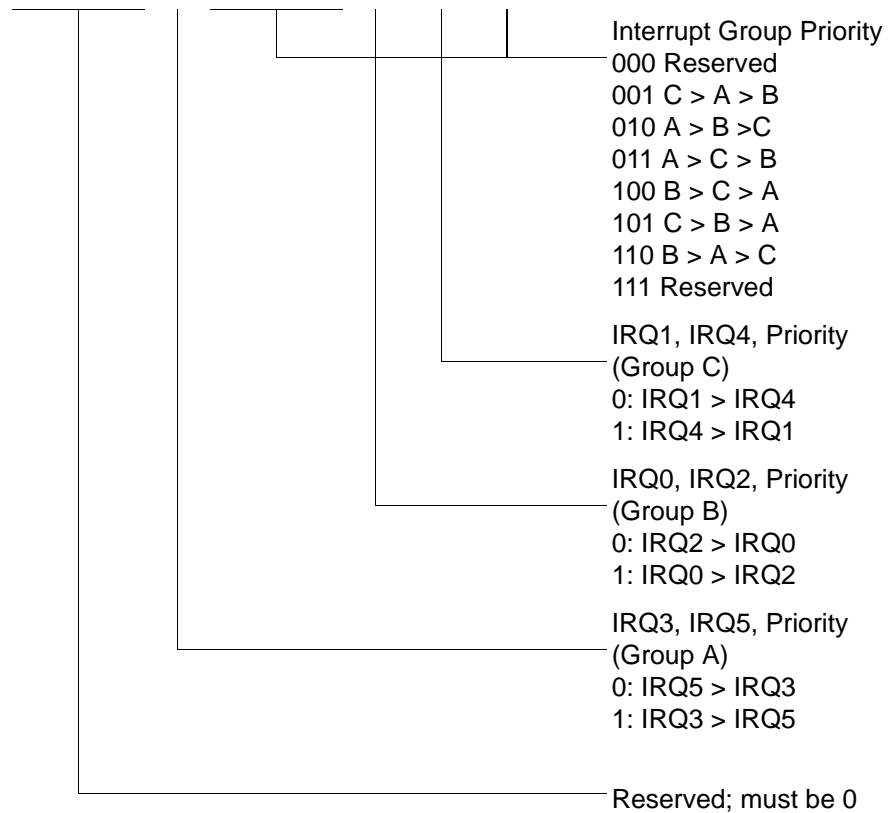| D7	D6	D5	D4	D3	D2	D1	D0

Interrupt Group Priority
000 Reserved
001 C > A > B
010 A > B >C
011 A > C > B
100 B > C > A
101 C > B > A
110 B > A > C
111 Reserved

IRQ1, IRQ4, Priority
(Group C)
0: IRQ1 > IRQ4
1: IRQ4 > IRQ1

IRQ0, IRQ2, Priority
(Group B)
0: IRQ2 > IRQ0
1: IRQ0 > IRQ2

IRQ3, IRQ5, Priority
(Group A)
0: IRQ5 > IRQ3
1: IRQ3 > IRQ5

Reserved; must be 0

Figure 51. Interrupt Priority Register (F9H: Write Only)

R250 IRQ(FAH)

D7	D6	D5	D4	D3	D2	D1	D0

IRQ0 = P32 Input
IRQ1 = P33 Input
IRQ2 = P31 Input
IRQ3 = T16
IRQ4 = T8
IRQ5 = LVD

Inter Edge
P31↓   P32↓ = 00
P31↓   P32↑ = 01
P31↑   P32↓ = 10
P31↑↓   P32↑↓ = 11
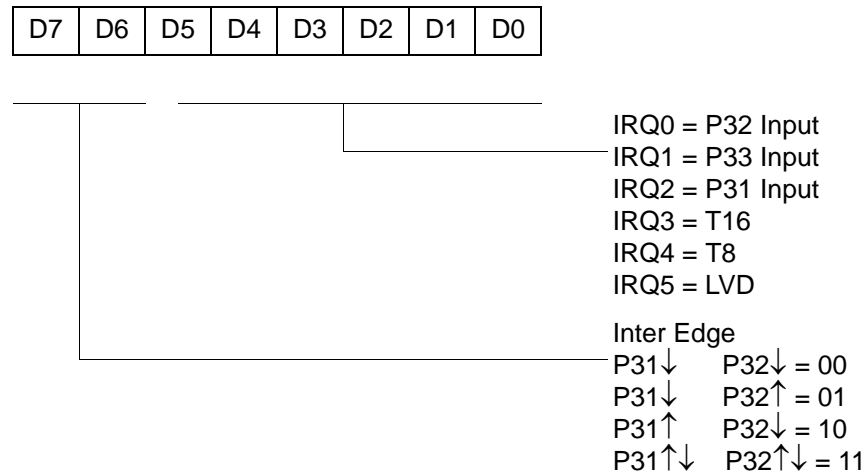
Figure 52. Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)

D7	D6	D5	D4	D3	D2	D1	D0

1 Enables IRQ5–IRQ0
   (D0 = IRQ0)

Reserved (Must be 0)

0   Master Interrupt Disable *
1   Master Interrupt Enable * *
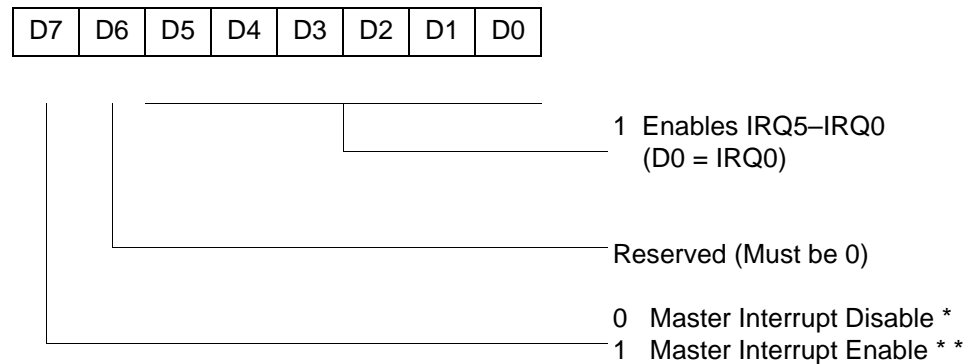
 * Default setting after reset
 * * Only by using EI, DI instruction; DI is required before changing the IMR register

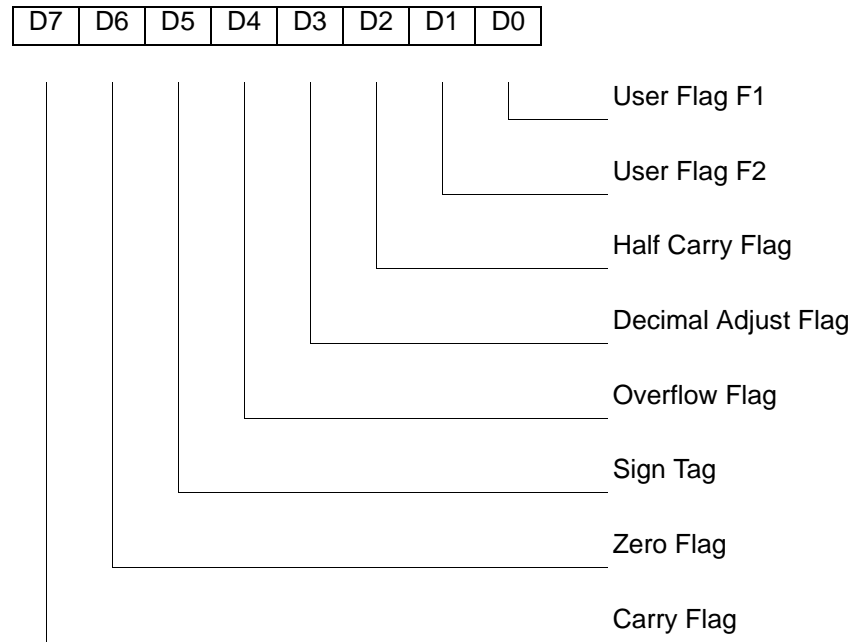**Figure 53. Interrupt Mask Register (FBH: Read/Write)**

R252 Flags(FCH)

D7	D6	D5	D4	D3	D2	D1	D0

User Flag F1

User Flag F2

Half Carry Flag

Decimal Adjust Flag

Overflow Flag

Sign Tag

Zero Flag

Carry Flag

Figure 54. Flag Register (FCH: Read/Write)

R253 RP(FDH)

D7	D6	D5	D4	D3	D2	D1	D0

Expanded Register Bank Pointer

Working Register Pointer
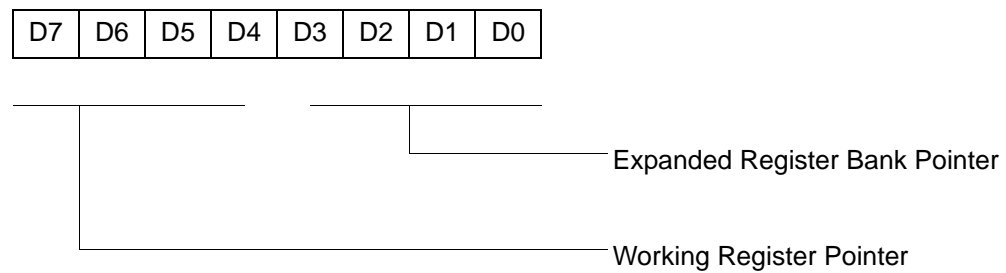
Default setting after reset = 0000 0000

Figure 55. Register Pointer (FDH: Read/Write)

SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 BSC			0.0256 BSC		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 61. 20-Pin SSOP Package Diagram
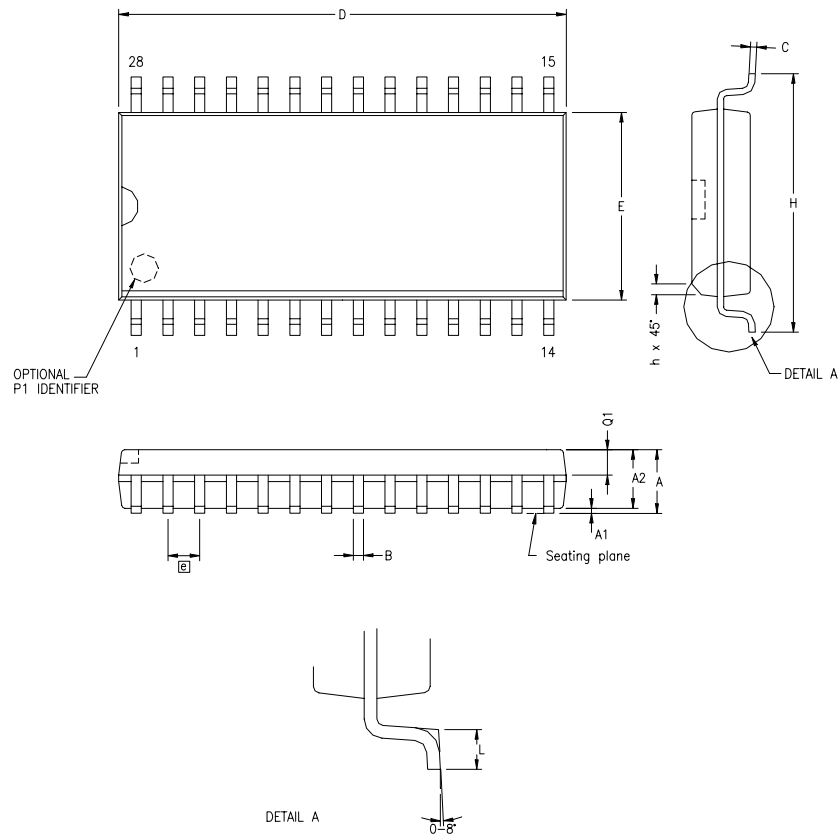
SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 63. 28-Pin SOIC Package Diagram

For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

Codes

ZG = ZiLOG General Purpose Family

P = OTP

323 = Family Designation

L = Voltage Range

   2V to 3.6V

T = Temperature Range:

   S = 0 to 70 degrees C (Standard)

   E = -40 to +105 degrees C (Extended)

   A = -40 to +125 degrees C (Automotive)

P = Package Type:

   K = Windowed Cerdip
   P = PDIP
   H = SSOP
   S = SOIC

= Number of Pins

CC = Memory Size

M = Packaging Options

   C = Non Lead-Free

   G = Lead-Free

   E = CDIP

Example

```
ZG    P    323    L    S    P    48    32    G
```

ZG — ZiLOG General-Purpose Family

P — OTP

323 — Family Designation

L — Voltage Range
L =2.0V to 3.6V

S — Temperature Range

P — Package Type

48 — Number of Pins

32 — Memory Size

G — Lead Free