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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

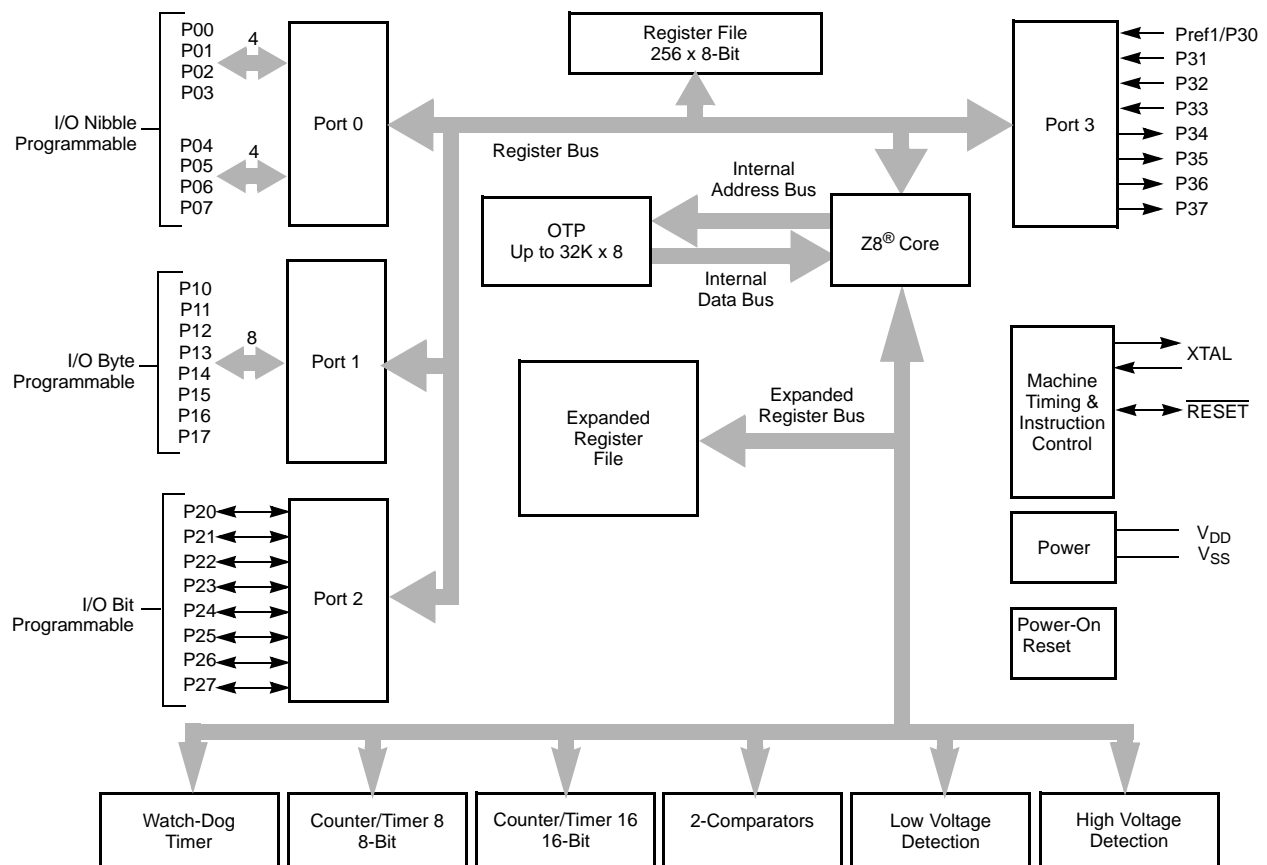
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |   |
|----------------------------|---|
| Product Status             | Obsolete  |
| Core Processor             | Z8  |
| Core Size                  | 8-Bit   |
| Speed                      | 8MHz  |
| Connectivity               | -   |
| Peripherals                | HLVD, POR, WDT  |
| Number of I/O              | 16  |
| Program Memory Size        | 8KB (8K x 8)  |
| Program Memory Type        | OTP   |
| EEPROM Size                | -   |
| RAM Size                   | 237 x 8   |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V   |
| Data Converters            | -   |
| Oscillator Type            | Internal  |
| Operating Temperature      | 0°C ~ 70°C (TA)   |
| Mounting Type              | Surface Mount   |
| Package / Case             | 20-SOIC (0.295", 7.50mm Width)  |
| Supplier Device Package    | -   |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/zilog/zgp323lss2008c">https://www.e-xfl.com/product-detail/zilog/zgp323lss2008c</a> |

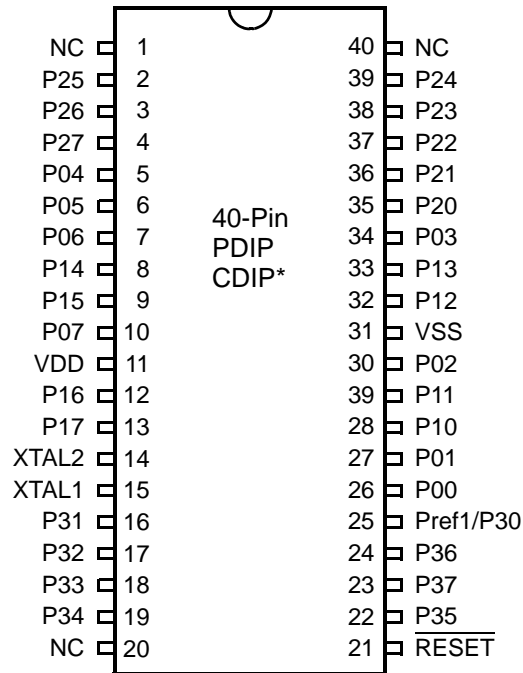
**Table 2. Power Connections**

| Connection | Circuit         | Device          |
|------------|-----------------|-----------------|
| Power      | V <sub>CC</sub> | V <sub>DD</sub> |
| Ground     | GND             | V <sub>SS</sub> |



Note: Refer to the specific package for available pins.

**Figure 1. Functional Block Diagram**

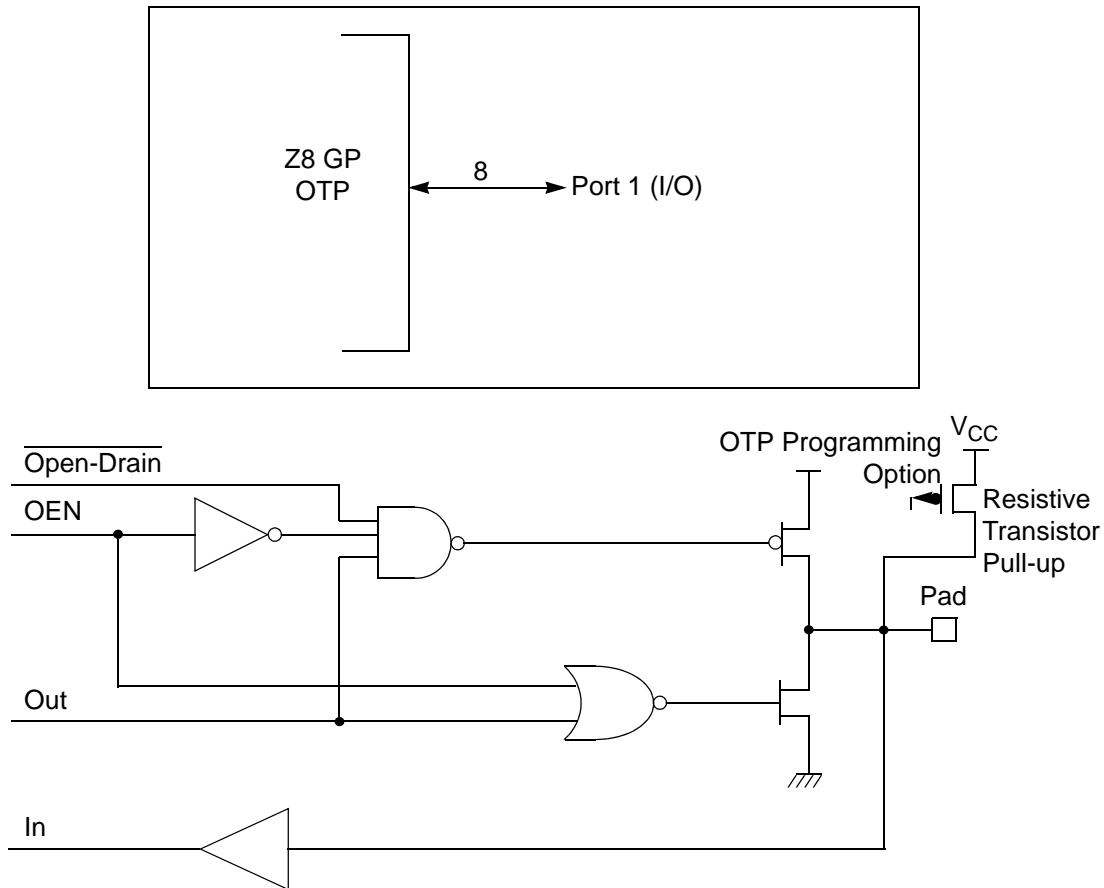


**Figure 5. 40-Pin PDIP/CDIP\* Pin Configuration**

► **Note:** \*Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

**Table 5. 40- and 48-Pin Configuration (Continued)**

| 40-Pin PDIP/CDIP* # | 48-Pin SSOP # | Symbol          |
|---------------------|---------------|-----------------|
| 33                  | 40            | P13             |
| 8                   | 9             | P14             |
| 9                   | 10            | P15             |
| 12                  | 15            | P16             |
| 13                  | 16            | P17             |
| 35                  | 42            | P20             |
| 36                  | 43            | P21             |
| 37                  | 44            | P22             |
| 38                  | 45            | P23             |
| 39                  | 46            | P24             |
| 2                   | 2             | P25             |
| 3                   | 3             | P26             |
| 4                   | 4             | P27             |
| 16                  | 19            | P31             |
| 17                  | 20            | P32             |
| 18                  | 21            | P33             |
| 19                  | 22            | P34             |
| 22                  | 26            | P35             |
| 24                  | 28            | P36             |
| 23                  | 27            | P37             |
| 20                  | 23            | NC              |
| 40                  | 47            | NC              |
| 1                   | 1             | NC              |
| 21                  | 25            | RESET           |
| 15                  | 18            | XTAL1           |
| 14                  | 17            | XTAL2           |
| 11                  | 12, 13        | V <sub>DD</sub> |
| 31                  | 24, 37, 38    | V <sub>SS</sub> |
| 25                  | 29            | Pref1/P30       |
|                     | 48            | NC              |

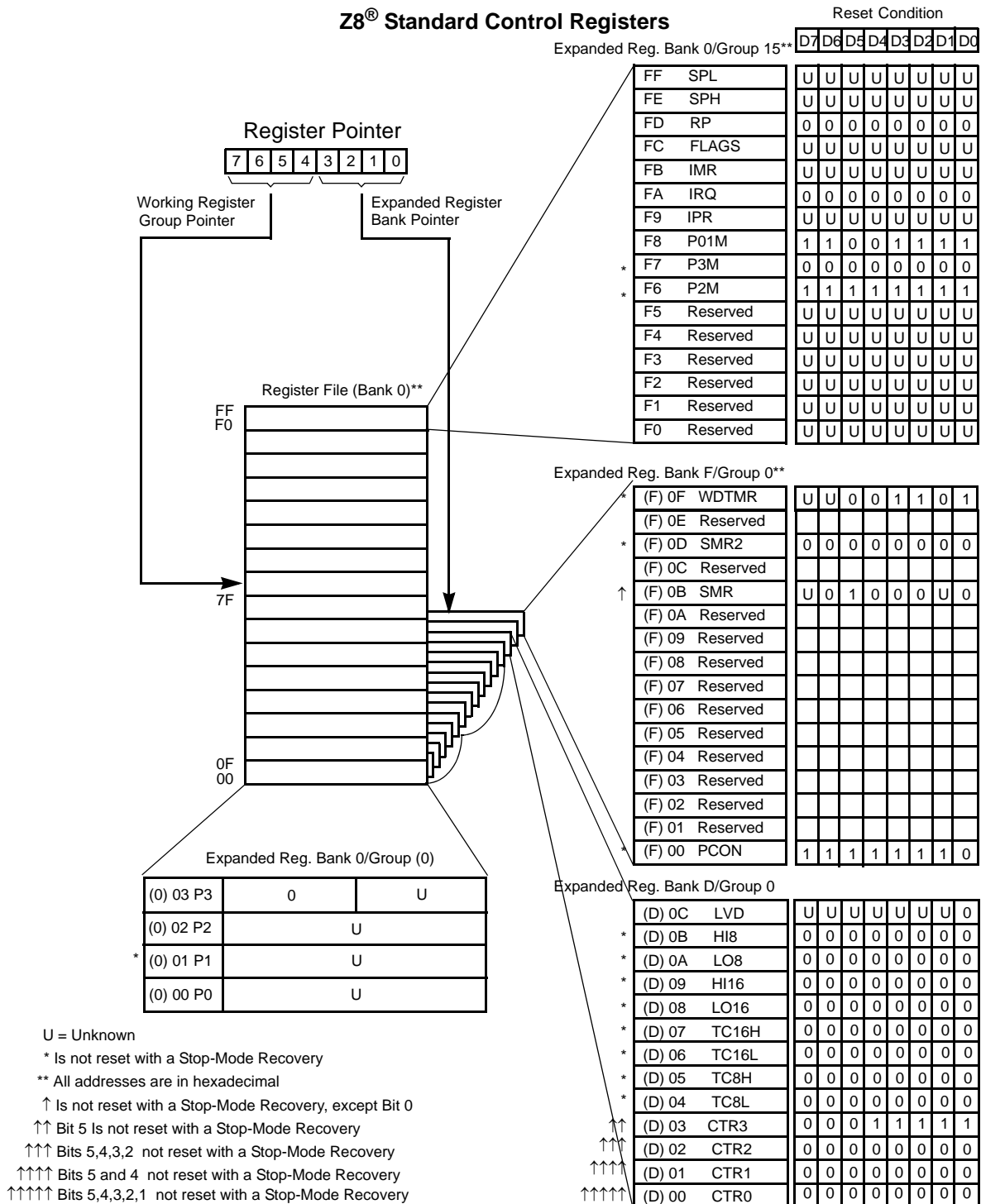


**Figure 10. Port 1 Configuration**

## Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 11). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode.



**Figure 15. Expanded Register File Architecture**

### **T8/T16\_Logic/Edge \_Detect**

In TRANSMIT Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION Mode, this field defines which edge should be detected by the edge detector.

### **Transmit\_Submode/Glitch Filter**

In Transmit Mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to “NORMAL OPERATION Mode” terminates the “PING-PONG Mode” operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION Mode, this field defines the width of the glitch that must be filtered out.

### **Initial\_T8\_Out/Rising\_Edge**

In TRANSMIT Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8\_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

### **Initial\_T16 Out/Falling \_Edge**

In TRANSMIT Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16\_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

- **Note:** Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/T16\_OUT.

### **CTR2 Counter/Timer 16 Control Register—CTR2(D)02H**

Table 14 lists and briefly describes the fields for this register.

into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFh (see Figure 23 and Figure 24).

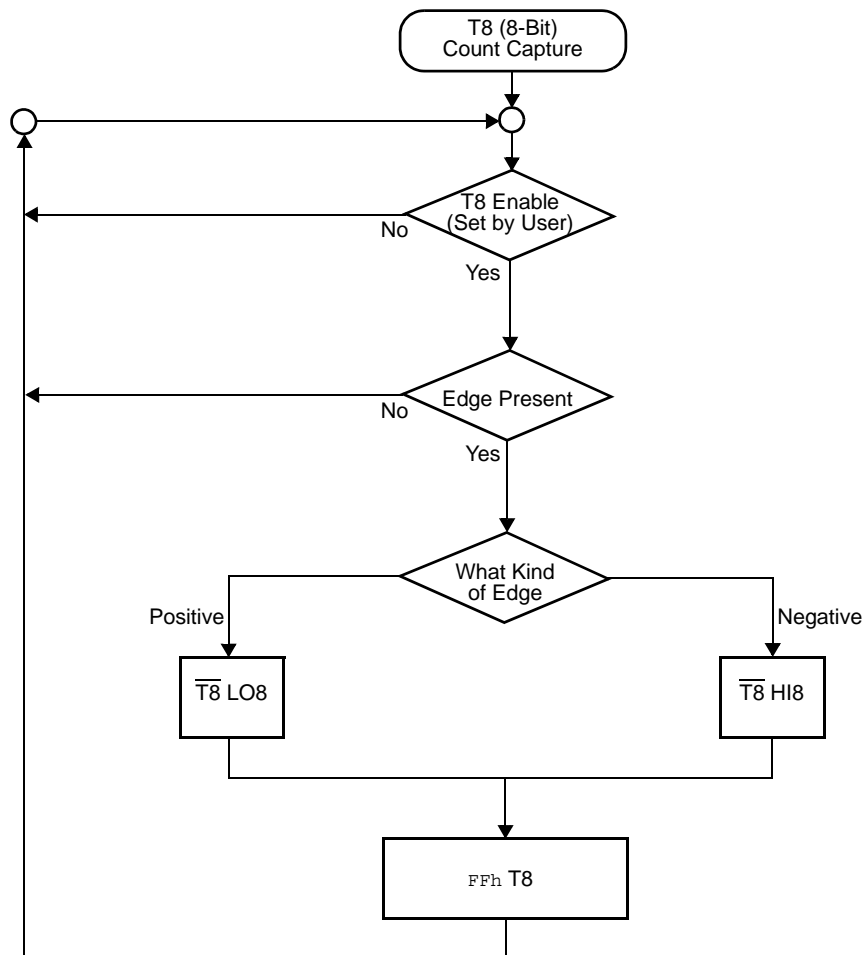


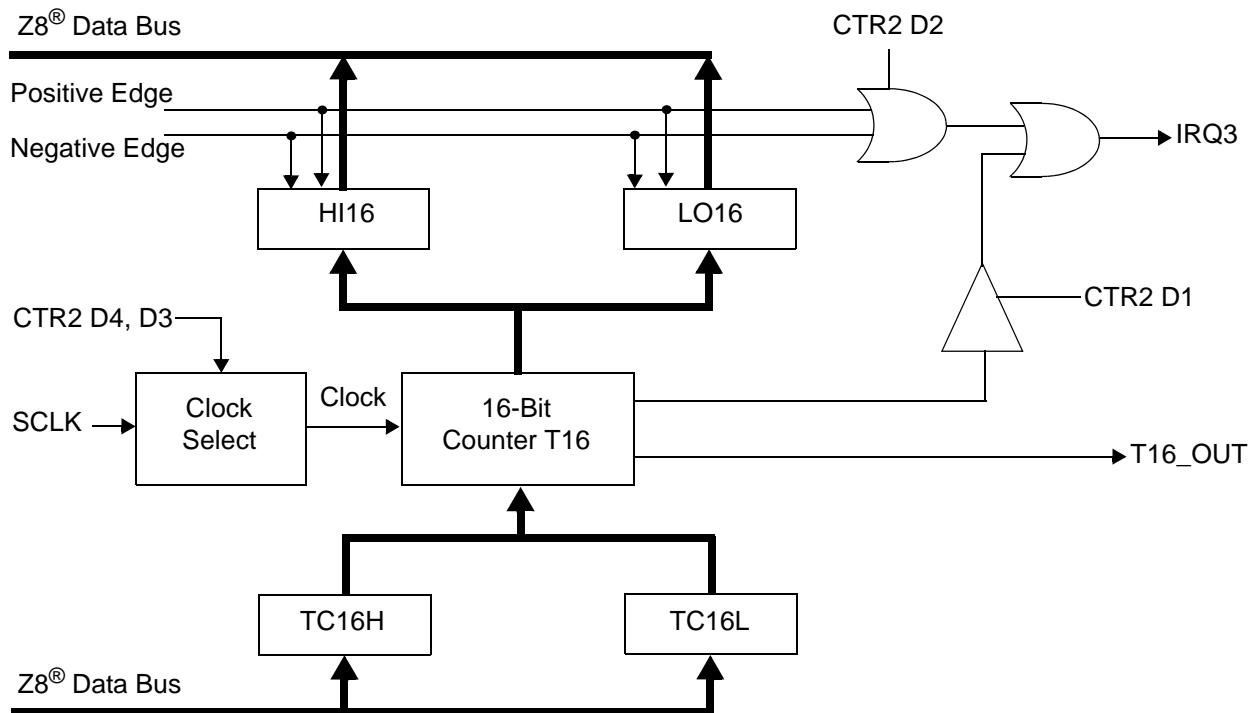
Figure 23. Demodulation Mode Count Capture Flowchart



### T16 Transmit Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16\_OUT is a 1; if it is a 1, T16\_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H \* 256 + TC16L is loaded, and T16\_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16\_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set. See Figure 25.



**Figure 25. 16-Bit Counter/Timer Circuits**

► **Note:** Global interrupts override this function as described in “Interrupts” on page 48.

If T16 is in SINGLE-PASS mode, it is stopped at this point (see Figure 26). If it is in Modulo-N Mode, it is loaded with TC16H \* 256 + TC16L, and the counting continues (see Figure 27).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.

### During PING-PONG Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

### Timer Output

The output logic for the timers is illustrated in Figure 29. P34 is used to output T8-OUT when D0 of CTR0 is set. P35 is used to output the value of T16-OUT when D0 of CTR2 is set. When D6 of CTR1 is set, P36 outputs the logic combination of T8-OUT and T16-OUT determined by D5 and D4 of CTR1.

### Interrupts

The Z8 GP™ OTP MCU Family features six different interrupts (Table 16). The interrupts are maskable and prioritized (Figure 30). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the counter/timers (Table 16) and one for low voltage detection. The Interrupt Mask Register (globally or individually) enables or disables the six interrupt requests.

The source for IRQ is determined by bit 1 of the Port 3 mode register (P3M). When in digital mode, Pin P33 is the source. When in analog mode the output of the Stop mode recovery source logic is used as the source for the interrupt. See Figure 35, Stop Mode Recovery Source, on page 57.

### Power-On Reset

A timer circuit clocked by a dedicated on-board RC-oscillator is used for the Power-On Reset (POR) timer function. The POR time allows  $V_{DD}$  and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from  $V_{BO}$  Standby
- Stop-Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is 2.5 ms minimum. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock).

### HALT Mode

This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after HALT Mode.

### STOP Mode

This instruction turns off the internal clock and external crystal oscillation, reducing the standby current to 10  $\mu$ A or less. STOP Mode is terminated only by a reset, such as WDT timeout, POR, SMR or external reset. This condition causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Opcode = FFH) immediately before the appropriate sleep instruction, as follows:

```
FF      NOP      ; clear the pipeline
6F      Stop     ; enter Stop Mode
```

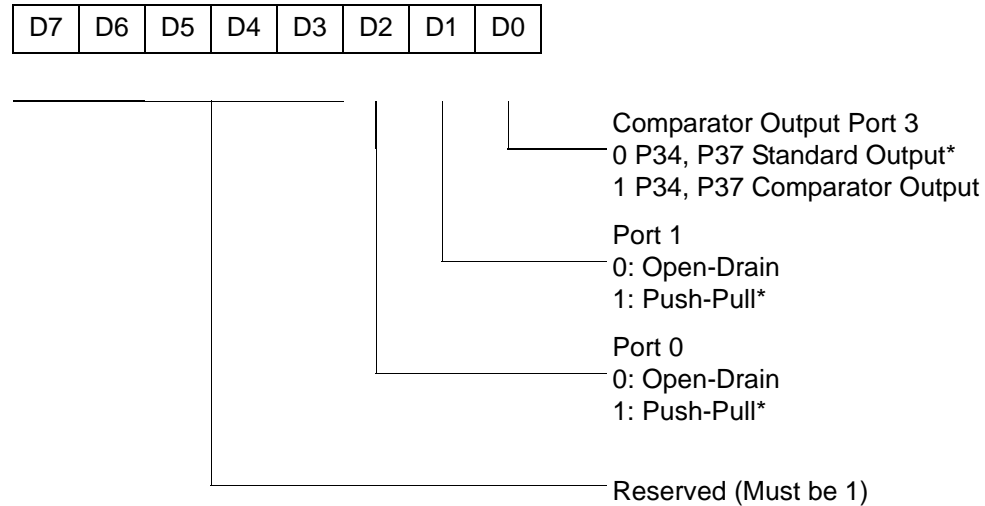
or

```
FF      NOP      ; clear the pipeline
7F      HALT     ; enter HALT Mode
```

### Port Configuration Register

The Port Configuration (PCON) register (Figure 32) configures the comparator output on Port 3. It is located in the expanded register 2 at Bank F, location 00.

PCON(FH)00H



\* Default setting after reset

**Figure 32. Port Configuration Register (PCON) (Write Only)**

#### Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

#### Port 1 Output Mode (D1)

Bit 1 controls the output mode of port 1. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

### WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

### EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 21.

**Table 21. EPROM Selectable Options**

|                                   |        |
|-----------------------------------|--------|
| Port 00–03 Pull-Ups               | On/Off |
| Port 04–07 Pull-Ups               | On/Off |
| Port 10–13 Pull-Ups               | On/Off |
| Port 14–17 Pull-Ups               | On/Off |
| Port 20–27 Pull-Ups               | On/Off |
| EPROM Protection                  | On/Off |
| Watch-Dog Timer at Power-On Reset | On/Off |

### Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the  $V_{DD}$  is at the required level for correct operation of the device. Reset is globally driven when  $V_{DD}$  falls below  $V_{BO}$ . A small drop in  $V_{DD}$  causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the  $V_{DD}$  is allowed to stay above  $V_{RAM}$ , the RAM content is preserved. When the power level is returned to above  $V_{BO}$ , the device performs a POR and functions normally.

### Low-Voltage Detection Register—LVD(D)0Ch

- **Note:** Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

| Field | Bit Position | Description           |         |                                |
|-------|--------------|-----------------------|---------|--------------------------------|
| LVD   | 76543---     | Reserved<br>No Effect |         |                                |
|       | ----2--      | R                     | 1<br>0* | HVD flag set<br>HVD flag reset |
|       | -----1-      | R                     | 1<br>0* | LVD flag set<br>LVD flag reset |
|       | -----0       | R/W                   | 1<br>0* | Enable VD<br>Disable VD        |

\*Default after POR

- **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

### Voltage Detection and Flags

The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the  $V_{CC}$  voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the  $V_{CC}$  level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if  $V_{CC}$  is higher than  $V_{HVD}$ . The LVD flag (bit 1 of the LVD register) is set only if  $V_{CC}$  is lower than the  $V_{LVD}$ . When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

- **Notes:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.

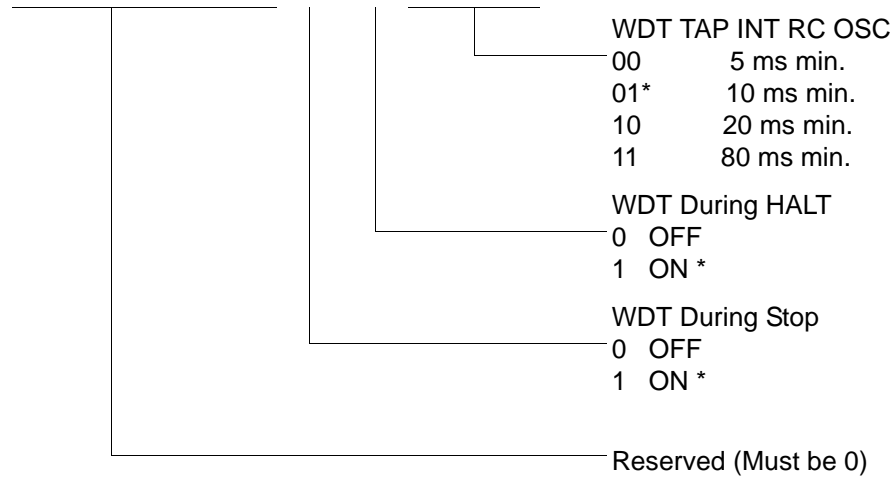


- **Notes:** Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.

WDTMR(0F)0FH

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|



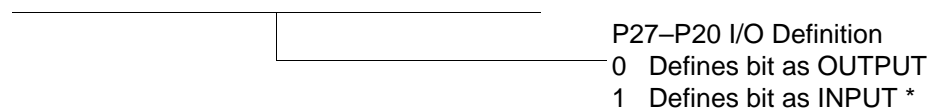
\* Default setting after reset

Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)

## Standard Control Registers

R246 P2M(F6H)

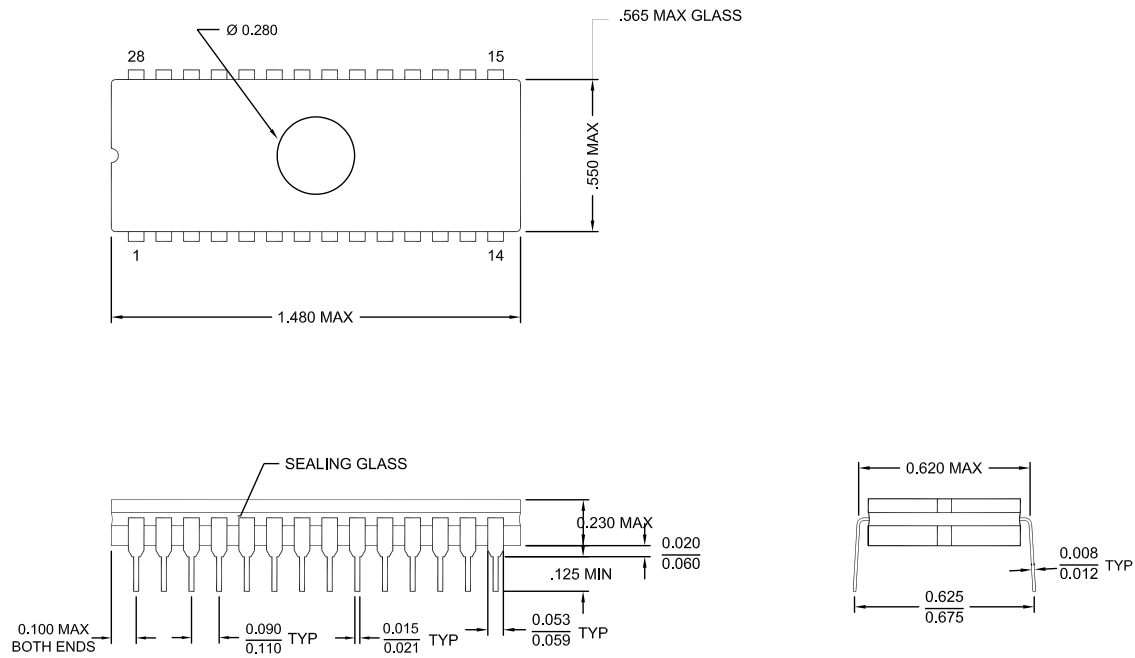
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|



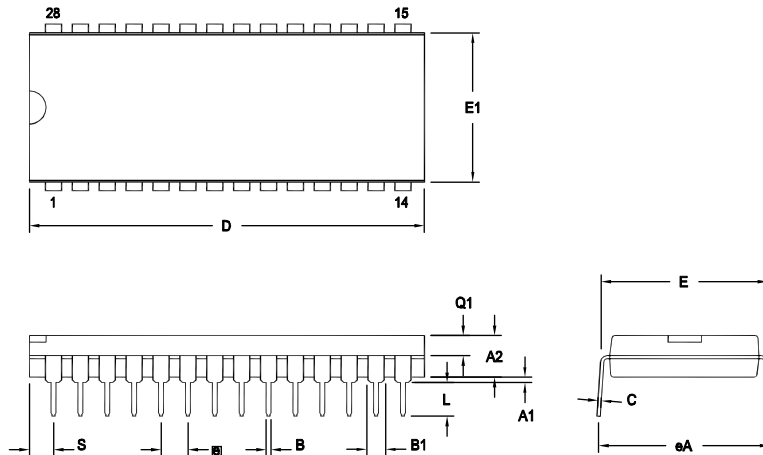
\* Default setting after reset

Figure 48. Port 2 Mode Register (F6H: Write Only)





**Figure 62. 28-Pin CDIP Package**



| OPTION TABLE |          |
|--------------|----------|
| OPTION #     | PACKAGE  |
| 01           | STANDARD |
| 02           | IDF      |

Note: ZILOG supplies both options for production. Component layout PCB design should cover bigger option 01.

| SYMBOL | OPT # | MILLIMETER |       | INCH     |       |
|--------|-------|------------|-------|----------|-------|
|        |       | MIN        | MAX   | MIN      | MAX   |
| A1     |       | 0.38       | 1.02  | .015     | .040  |
| A2     |       | 3.18       | 4.19  | .125     | .165  |
| B      |       | 0.38       | 0.53  | .015     | .021  |
| B1     | 01    | 1.40       | 1.65  | .055     | .065  |
|        | 02    | 1.14       | 1.40  | .045     | .055  |
| C      |       | 0.23       | 0.38  | .009     | .015  |
| D      | 01    | 36.58      | 37.34 | 1.440    | 1.470 |
|        | 02    | 35.31      | 35.94 | 1.390    | 1.415 |
| E      |       | 15.24      | 15.75 | .600     | .620  |
| E1     | 01    | 13.59      | 14.10 | .535     | .555  |
|        | 02    | 12.83      | 13.08 | .505     | .515  |
| e      |       | 2.54 TYP   |       | .100 BSC |       |
| eA     |       | 15.49      | 16.76 | .610     | .660  |
| L      |       | 3.05       | 3.81  | .120     | .150  |
| Q1     | 01    | 1.40       | 1.91  | .055     | .075  |
|        | 02    | 1.40       | 1.78  | .055     | .070  |
| S      | 01    | 1.52       | 2.29  | .060     | .090  |
|        | 02    | 1.02       | 1.52  | .040     | .060  |

CONTROLLING DIMENSIONS : INCH

Figure 64. 28-Pin PDIP Package Diagram



## **Precharacterization Product**

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the document might be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery might be uncertain at times, due to start-up yield issues.

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