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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/zgp323lss2016c">https://www.e-xfl.com/product-detail/zilog/zgp323lss2016c</a>



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**Table 5. 40- and 48-Pin Configuration (Continued)**

40-Pin PDIP/CDIP* #	48-Pin SSOP #	Symbol
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	RESET
15	18	XTAL1
14	17	XTAL2
11	12, 13	V <sub>DD</sub>
31	24, 37, 38	V <sub>SS</sub>
25	29	Pref1/P30
	48	NC



**Table 9. EPROM/OTP Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	Erase Time	15			Minutes	1,3
	Data Retention @ use years		10		Years	2
	Program/Erase Endurance	25			Cycles	1

Notes:

1. For windowed cerdip package only.
2. Standard: 0°C to 70°C; Extended: -40°C to +105°C; Automotive: -40°C to +125°C.  
Determined using the Arrhenius model, which is an industry standard for estimating data retention of floating gate technologies:

$$AF = \exp[(Ea/k) * (1/Tuse - 1/TStress)]$$

Where:

Ea is the intrinsic activation energy (eV; typ. 0.8)

k is Boltzman's constant (8.67 x 10<sup>-5</sup> eV/°K)

°K = -273.16°C

Tuse = Use Temperature in °K

TStress = Stress Temperature in °K

3. At a stable UV Lamp output of 20mW/CM<sup>2</sup>

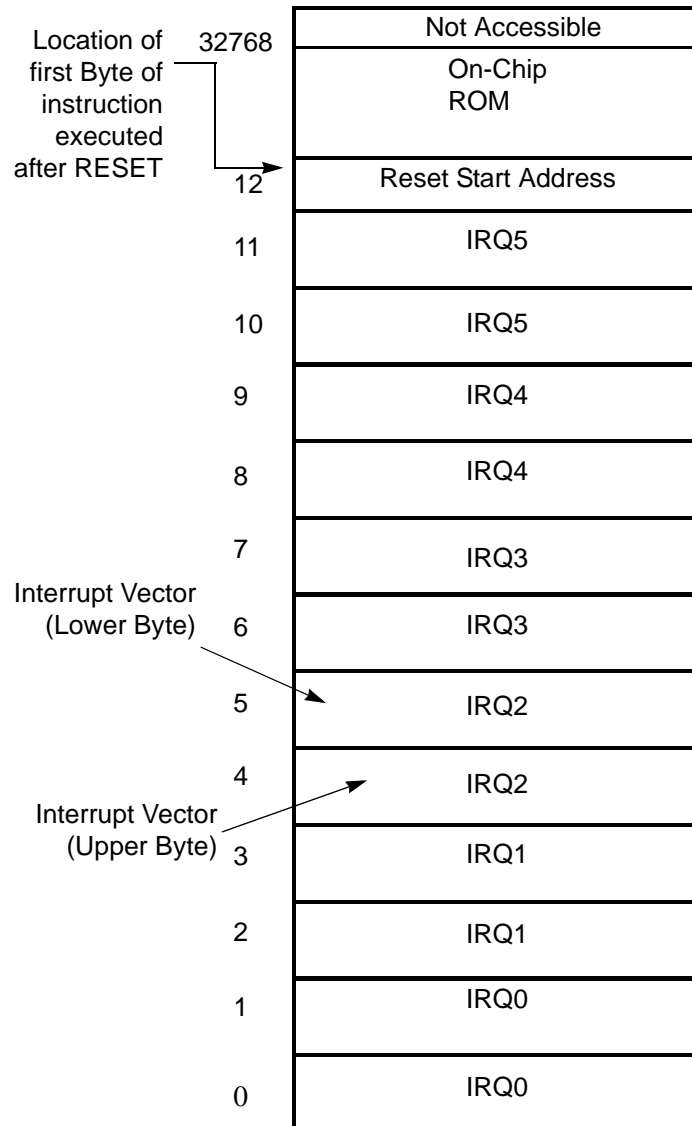


Figure 14. Program Memory Map (32K OTP)

## Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8® register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the

In Demodulation Mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode on page 45.

#### Time\_Out

This bit is set when T16 times out (terminal count reached). To reset the bit, write a 1 to this location.

#### T16\_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

#### Capture\_INT\_Mask

This bit is set to allow an interrupt when data is captured into LO16 and HI16.

#### Counter\_INT\_Mask

Set this bit to allow an interrupt when T16 times out.

#### P35\_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

#### CTR3 T8/T16 Control Register—CTR3(D)03H

Table 15 lists and briefly describes the fields for this register. This register allows the T<sub>8</sub> and T<sub>16</sub> counters to be synchronized.

**Table 15. CTR3 (D)03H: T8/T16 Control Register**

Field	Bit Position		Value	Description
T <sub>16</sub> Enable	7-----	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
T <sub>8</sub> Enable	-6-----	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
Sync Mode	--5-----	R/W	0**	Disable Sync Mode
			1	Enable Sync Mode

**Table 15. CTR3 (D)03H: T8/T16 Control Register (Continued)**

Field	Bit Position		Value	Description
Reserved	---43210	R	1	Always reads 11111
		W	x	No Effect

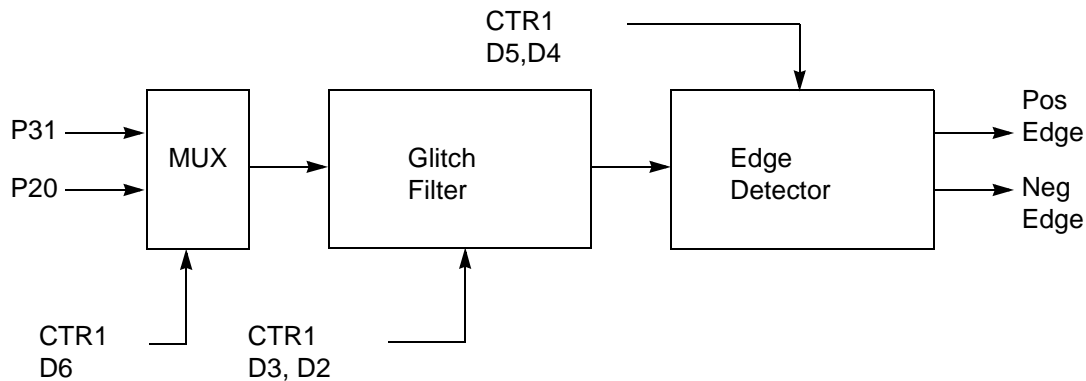
Note: \*Indicates the value upon Power-On Reset.

\*\*Indicates the value upon Power-On Reset. Not reset with Stop Mode recovery.

## Counter/Timer Functional Blocks

### Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 18).



**Figure 18. Glitch Filter Circuitry**

### T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8\_OUT is 1; if it is 1, T8\_OUT is 0. See Figure 19.

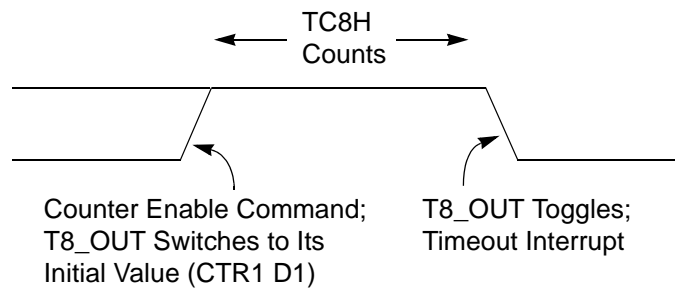
► **Note:** The letter *h* denotes hexadecimal values.

Transition from 0 to FF<sub>h</sub> is not a timeout condition.

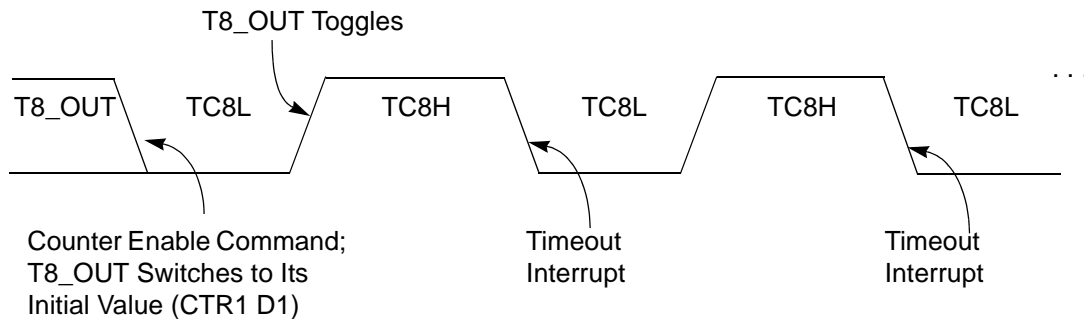


**Caution:** Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.



**Figure 21. T8\_OUT in Single-Pass Mode**



**Figure 22. T8\_OUT in Modulo-N Mode**

### T8 Demodulation Mode

The user must program TC8L and TC8H to FF<sub>h</sub>. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put



into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFh (see Figure 23 and Figure 24).

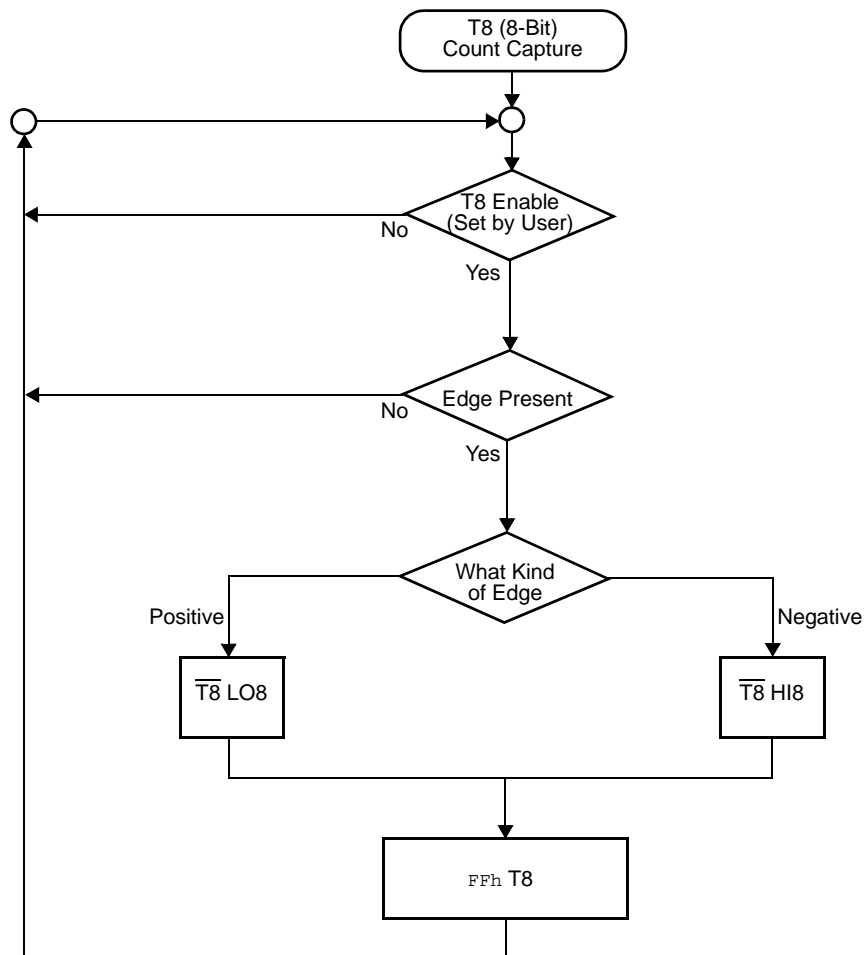
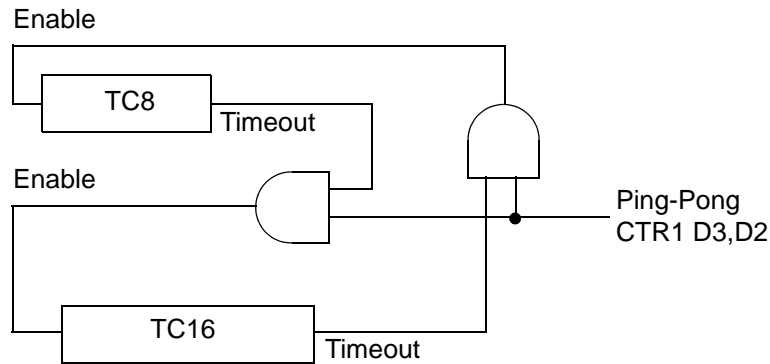


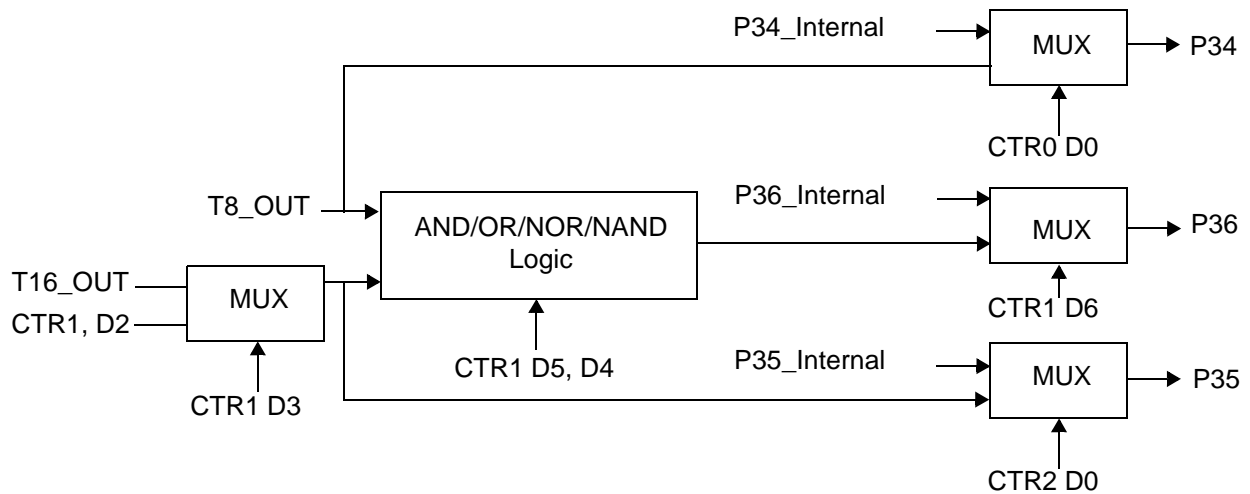
Figure 23. Demodulation Mode Count Capture Flowchart



**Figure 28. Ping-Pong Mode Diagram**

### Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the Ping-Pong mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See Figure 29.



**Figure 29. Output Circuit**

The initial value of T8 or T16 must not be 1. Stopping the timer and restarting the timer reloads the initial value to avoid an unknown previous value.

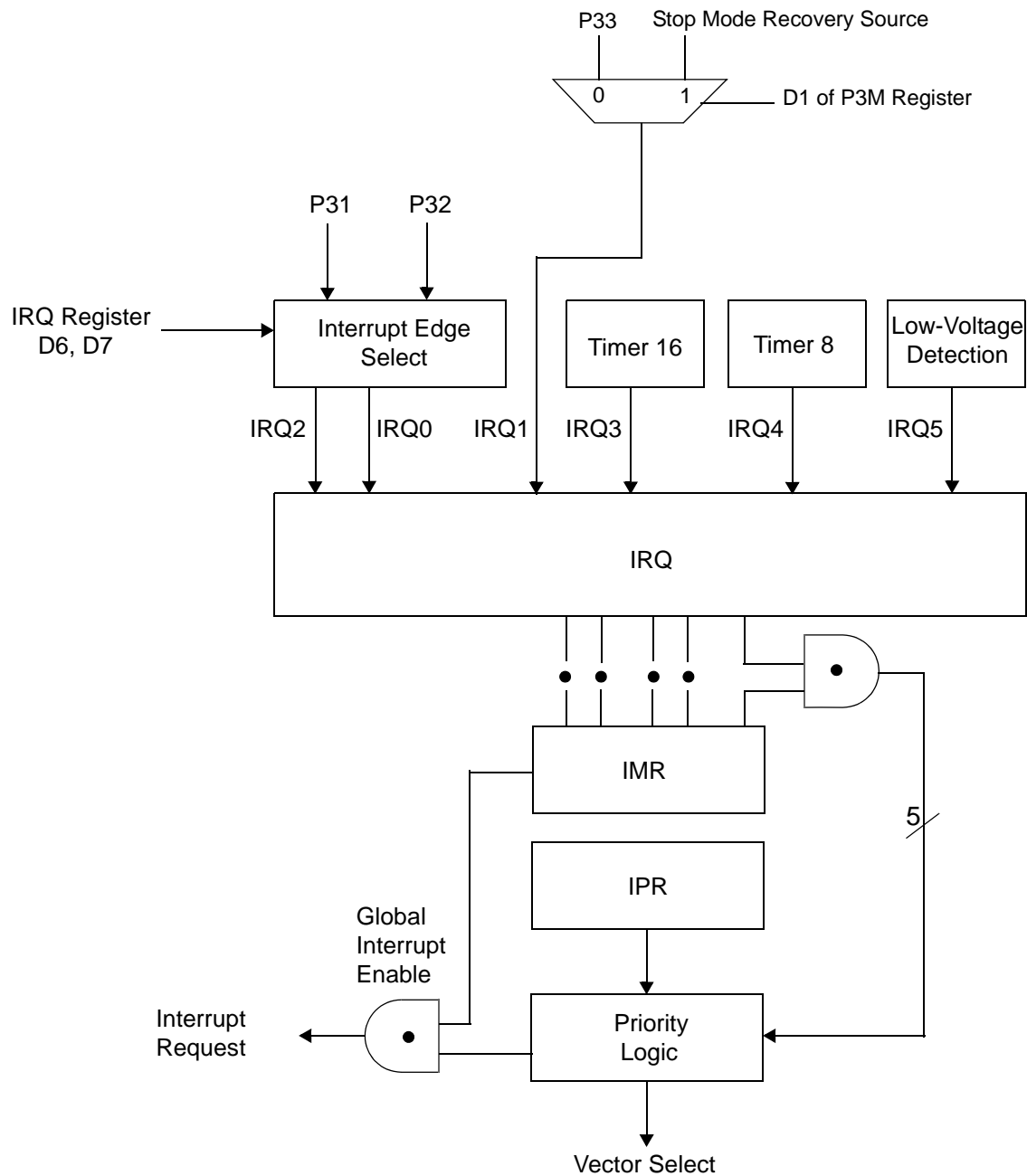
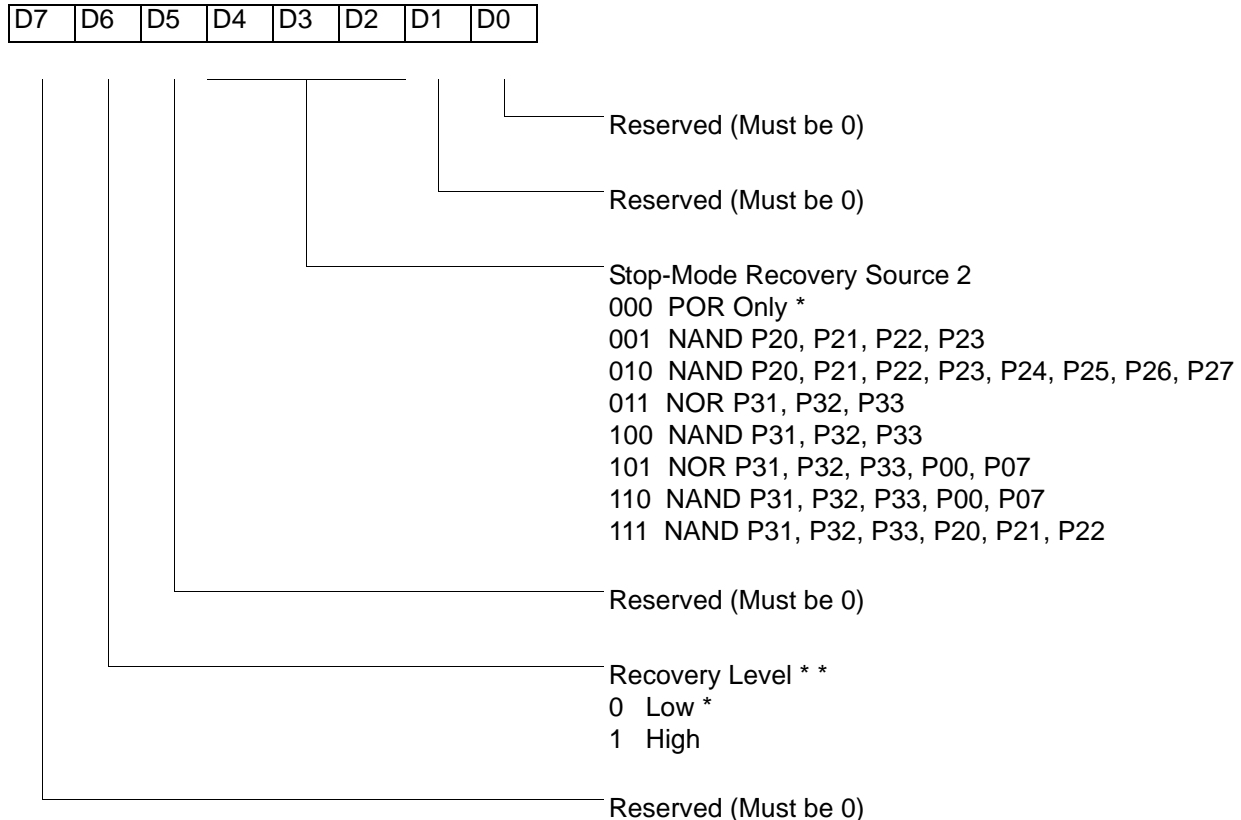


Figure 30. Interrupt Block Diagram

## Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (Figure 36).

SMR2(0F)DH



Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

\* Default setting after reset

\*\* At the XOR gate input

**Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)**

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.

► **Note:** Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.

### WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

### EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 21.

**Table 21. EPROM Selectable Options**

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
EPROM Protection	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

### Voltage Brown-Out/Standby

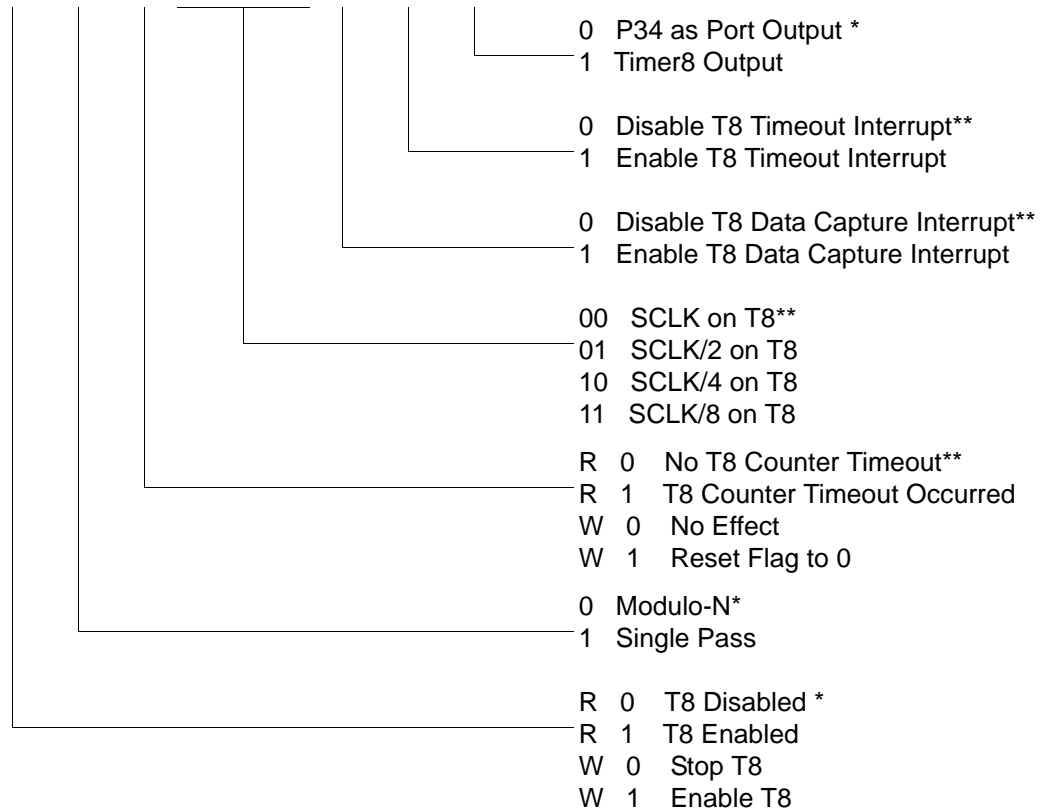
An on-chip Voltage Comparator checks that the  $V_{DD}$  is at the required level for correct operation of the device. Reset is globally driven when  $V_{DD}$  falls below  $V_{BO}$ . A small drop in  $V_{DD}$  causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the  $V_{DD}$  is allowed to stay above  $V_{RAM}$ , the RAM content is preserved. When the power level is returned to above  $V_{BO}$ , the device performs a POR and functions normally.

## Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are depicted in Figure 39 through Figure 43.

CTR0(0D)00H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



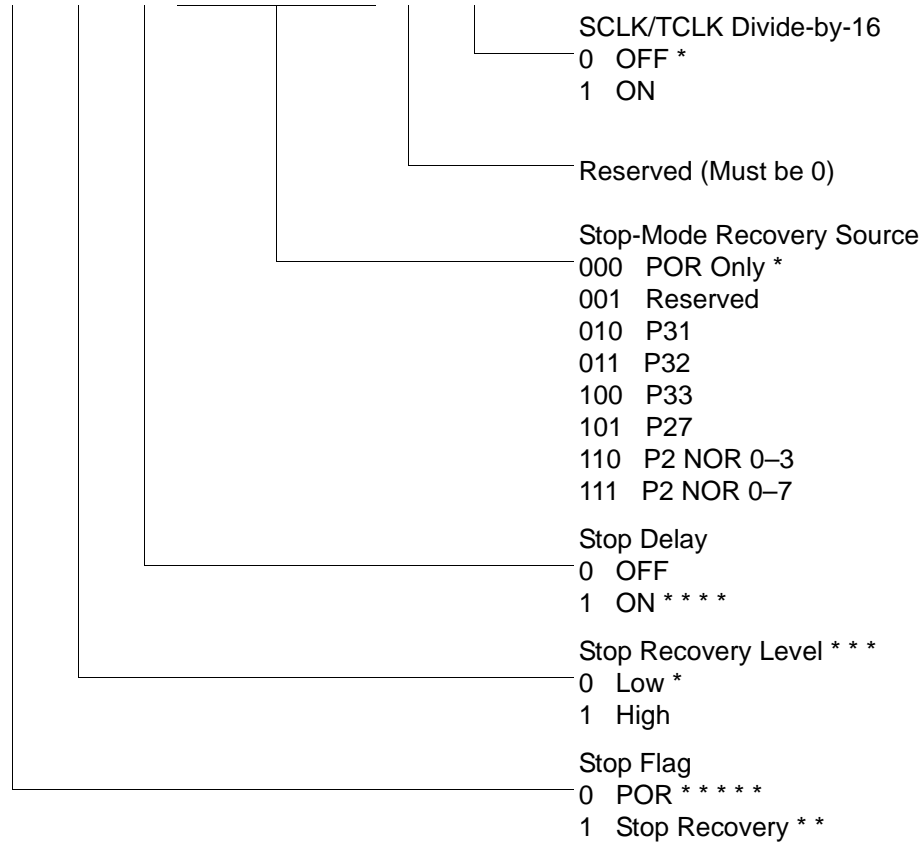
\* Default setting after reset

\*\*Default setting after reset. Not reset with Stop Mode recovery.

**Figure 39. TC8 Control Register ((0D)00H: Read/Write Except Where Noted)**

SMR(0F)0BH

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



\* Default setting after Reset

\* \* Set after STOP Mode Recovery

\* \* \* At the XOR gate input

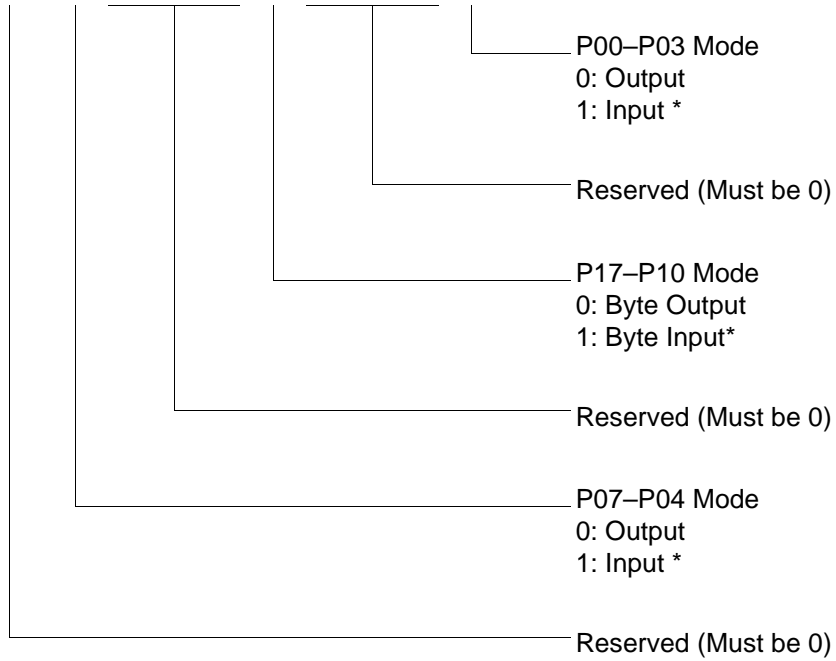
\* \* \* \* Default setting after Reset. Must be 1 if using a crystal or resonator clock source.

\* \* \* \* \* Default setting after Power On Reset. Not Reset with a Stop Mode recovery.

**Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)**

R248 P01M(F8H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



\* Default setting after reset; only P00, P01 and P07 are available in 20-pin configurations.

**Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)**



R249 IPR(F9H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

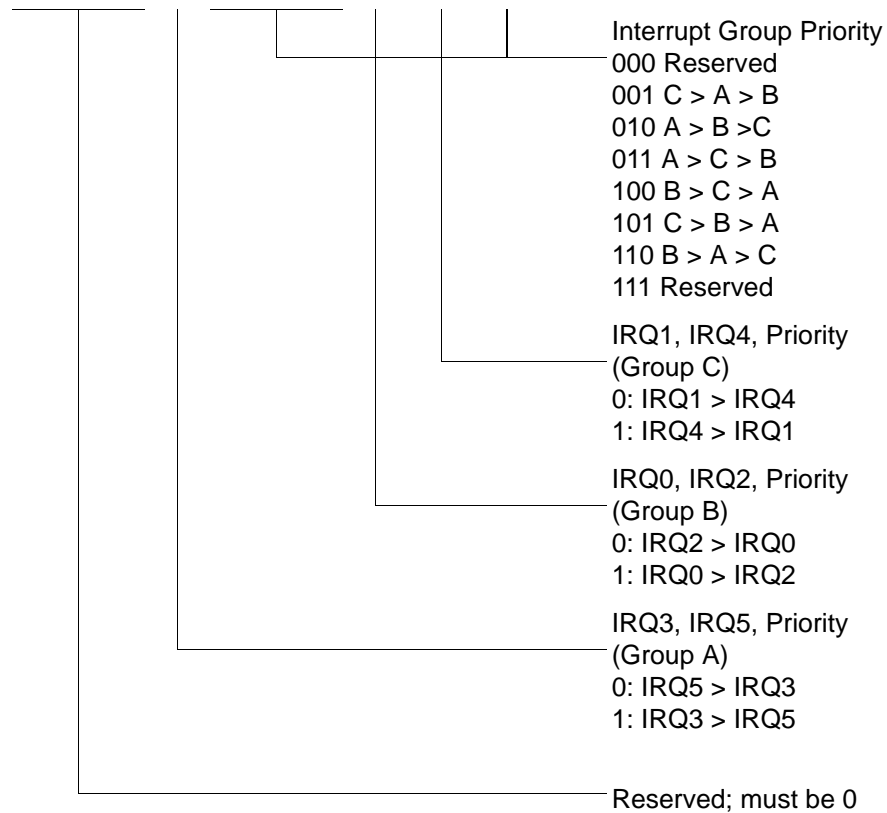
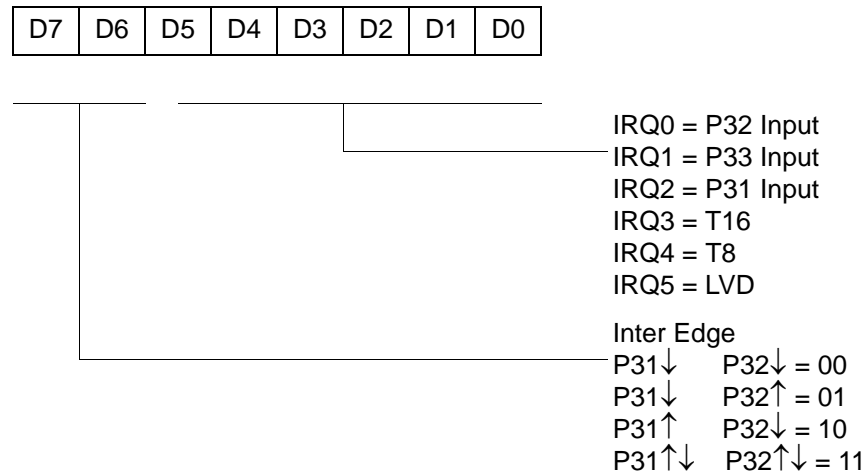


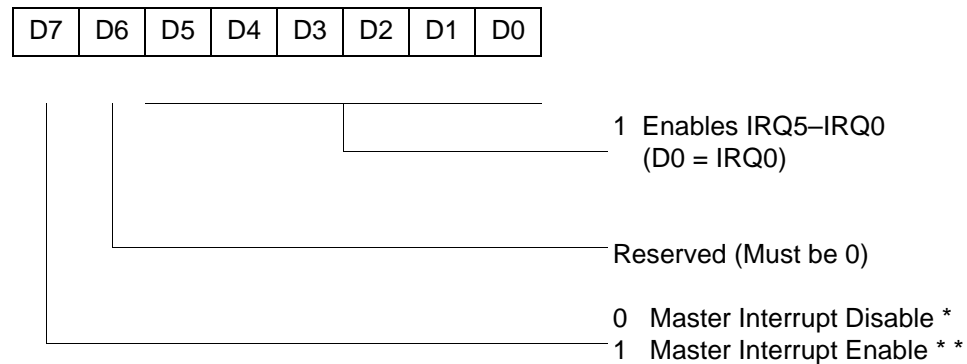
Figure 51. Interrupt Priority Register (F9H: Write Only)

R250 IRQ(FAH)



**Figure 52. Interrupt Request Register (FAH: Read/Write)**

R251 IMR(FBH)



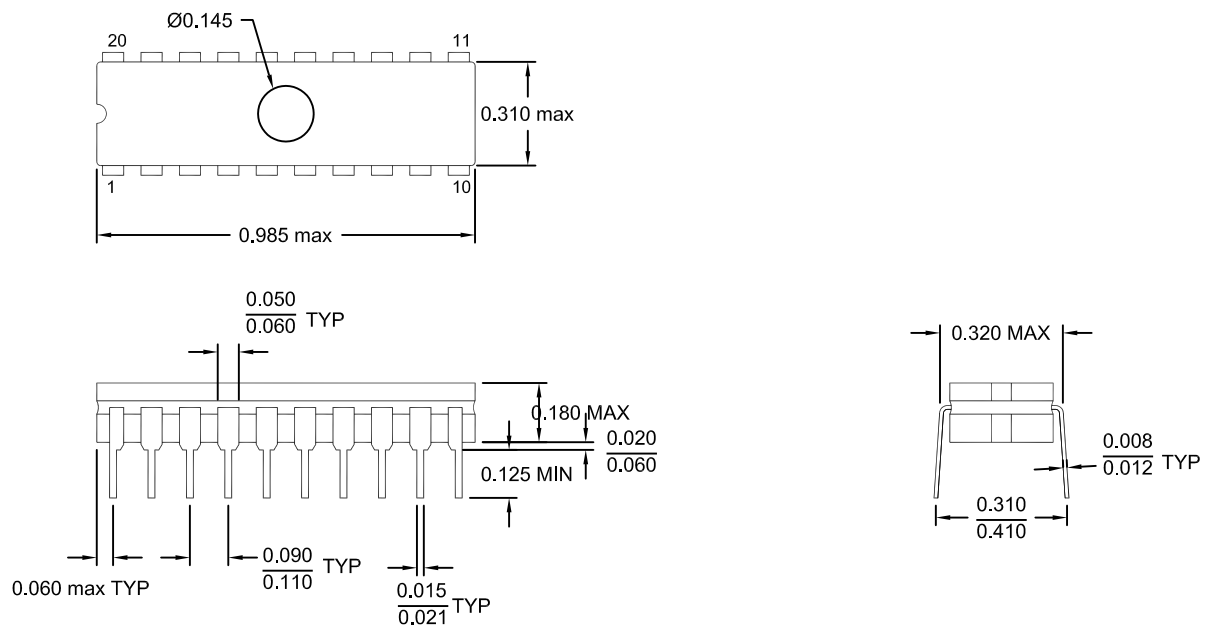
\* Default setting after reset

\*\* Only by using EI, DI instruction; DI is required before changing the IMR register

**Figure 53. Interrupt Mask Register (FBH: Read/Write)**

## Package Information

Package information for all versions of Z8 GP™ OTP MCU Family are depicted in Figures 58 through Figure 68.



**Figure 58. 20-Pin CDIP Package**

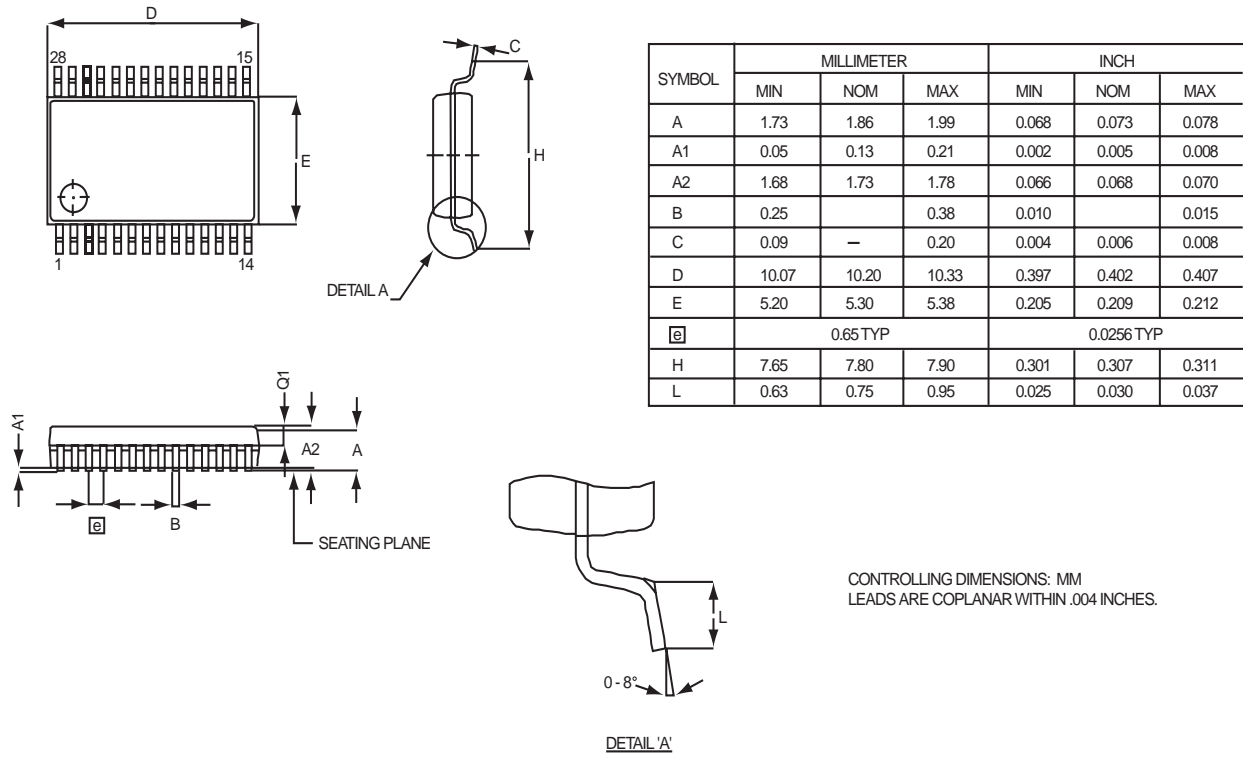


Figure 65. 28-Pin SSOP Package Diagram

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