Welcome to E-XFL.COM

Understanding **Embedded - Microprocessors**

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

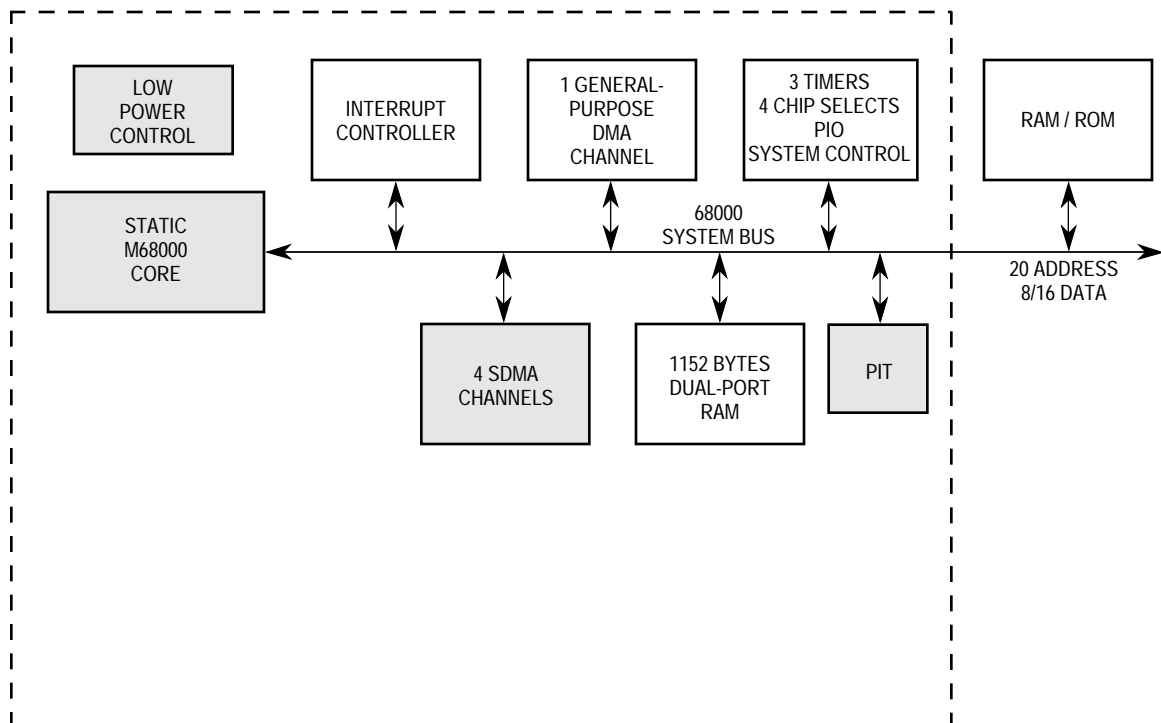| Details	
Product Status	Obsolete
Core Processor	M68000
Number of Cores/Bus Width	1 Core, 8/16-Bit
Speed	25MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc68lc302af25ct

freescale™
semiconductor

MC68LC302

Product Brief
Low Cost Integrated Multiprotocol Processor

Freescale introduces the low cost version of the well-known MC68302 Integrated Multiprotocol Processor (IMP). It will be known as the MC68LC302, and will expand a family of devices based on the MC68302.

Some features and pins have been removed while other features have been enhanced as compared to the original MC68302. Simply put, the MC68LC302 is a traditional MC68302 with a new static 68000 core, a new timer and low power modes, but without the third serial communication controller (SCC). It is packaged in a low profile 100 TQFP that requires less board space than the regular MC68302, as well as making it suitable for use in height restricted applications such as PCMCIA.

.

```
┌ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ┐
│                                                   │
│  ┌──────────┐  ┌──────────┐ ┌──────────┐ ┌──────────┐   ┌──────────┐
│  │  LOW     │  │INTERRUPT │ │1 GENERAL-│ │ 3 TIMERS │   │ RAM/ROM  │
│  │  POWER   │  │CONTROLLER│ │ PURPOSE  │ │4 CHIP SEL│   │          │
│  │ CONTROL  │  │          │ │   DMA    │ │   PIO    │   │          │
│  └──────────┘  └──────────┘ │ CHANNEL  │ │SYS CTRL  │   └──────────┘
│  ┌──────────┐               └──────────┘ └──────────┘
│  │ STATIC   │       68000 SYSTEM BUS
│  │ M68000   │ ◄──────────────────────────────────────────►
│  │  CORE    │                                   20 ADDRESS
│  └──────────┘  ┌──────────┐ ┌──────────┐ ┌──────┐  8/16 DATA
│                │ 4 SDMA   │ │1152 BYTES│ │ PIT  │
│                │ CHANNELS │ │DUAL-PORT │ │      │
│                │          │ │   RAM    │ │      │
│                └──────────┘ └──────────┘ └──────┘
└ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ┘
```

For More Information On This Product,
Go to: www.freescale.com

Freescale Semiconductor, Inc.

FEATURES

The features of the MC68LC302 are as follows. **Bold face** items show major differences from the MC68302.

- On-Chip **Static 68000 Core** Supporting a 16- or 8-Bit M68000 Family System

- SIB Including:

  — Independent Direct Memory Access (IDMA) Controller

  — Interrupt Controller with Two Modes of Operation

  — Parallel Input/Output (I/O) Ports, Some with Interrupt Capability

  — On-Chip 1152-Byte Dual-Port RAM

  — Three Timers Including a Watchdog Timer

  — New Periodic Interrupt Timer (PIT)

  — Four Programmable Chip-Select Lines with Wait-State Generator Logic

  — Programmable Address Mapping of the Dual-Port RAM and IMP Registers

  — On-Chip Clock Generator with Output Signal

  — On-Chip PLL Allows Operation with 32 kHz or 4 MHz Crystals

  — Glueless Interface to EPROM, SRAM, Flash EPROM, and EEPROM

  — Allows Boot in 8-bit Mode, and Running Switch to 16-bit Mode

  — System Control:

    System Status and Control Logic
    Disable CPU Logic (Slave Mode Operation)
    Hardware Watchdog
    New Low-Power (Standby) Modes with Wake-Up from Two Pins or PIT
    Freeze Control for Debugging (Available Only in the PGA Package)
    DRAM Refresh Controller

- CP Including:

  — Main Controller (RISC Processor)

  — **Two Independent Full-Duplex Serial Communications Controllers (SCCs)**

  — Supporting Various Protocols:

    High-Level/Synchronous Data Link Control (HDLC/SDLC)
    Universal Asynchronous Receiver Transmitter (UART)
    Binary Synchronous Communication (BISYNC)
    Transparent Modes
    Autobaud Support

MC68LC302 APPLICATIONS

The MC68LC302 excels in several applications areas.

First, any application using the MC68302,but not needing all three serial channels is a potential candidate for the MC68LC302. Note however, that the MC68LC302 sacrifices most of the provision for external bus mastership, thus the MC68LC302 may not be appropriate where the MC68302 is used as part of larger systems.

Second, the MC68LC302 excels in low power and portable applications. The inclusion of a static 68000 core, coupled with the low power modes built into the device make it ideal for handheld, or other low power applications. The new 32 kHz or 4 MHz PLL option greatly reduces the total power budget of the designer's board, and allows the MC68LC302 to be an effective device in low power systems. The MC68LC302 can then optionally generate a full frequency clock for use by the rest of the board. During low power modes, the new periodic interrupt timer (PIT) allows the device to awaken at regular intervals. In addition, two pins can awaken the device from low power modes.

Third, given that the MC68LC302 is packaged in a 100TQFP package, it allows the MC68LC302 to be used in space critical applications, as well as height critical applications such as PCMCIA cards.

Fourth, since the disable CPU mode (also known as slave mode) is still retained, the MC68LC302 can function as a fully intelligent DMA-driven peripheral chip containing serial channels, timers, chip selects, etc.

DIFFERENCES BETWEEN THE MC68LC302 AND MC68302

The MC68LC302 has some specific differences from the MC68302. Even though the functionality of the processor and the peripherals remain the same, some of the flexibility has been removed due to the pin reduction from 132 on the original MC68302, to 100 pins on the MC68LC302.

The following features have been removed or modified from the MC68302 in order to make the MC68LC302 possible.

- SCC3 and its baud rate generator (BRG3) are removed.
- External masters are not able to take the bus away from the MC68LC302 through the normal bus arbitration scheme as these pins no longer exist. An external master can still maintain bus mastership through a simple scheme using the $\overline{\text{HALT}}$ pin. This restriction does not apply when using the MC68LC302 in CPU disabled mode (slave mode), in which case $\overline{\text{BR}}$, $\overline{\text{BG}}$, and $\overline{\text{BGACK}}$ are all available.

MC68LC302 PRODUCT INFORMATION

- The SCP pins are now muxed with PA8, PA9, and PA10. The TXD3, RXD3, and RCLK3 functions associated with SCC3 are eliminated.

- The $\overline{\text{UDS}}$, $\overline{\text{LDS}}$, and R/$\overline{\text{W}}$ pins are not available except in slave mode, where they replace the $\overline{\text{IPL2-0}}$ pins. Instead, the new pins $\overline{\text{WEH}}$, $\overline{\text{WEL}}$, and $\overline{\text{OE}}$ have been defined for glueless interfacing to memory.

- PA12 is now muxed with the MODCLK pin, which is associated with the 32 KHz or 4 MHz PLL. The MODCLK pin is sampled after reset, and then becomes PA12.

- New VCCSYN, GNDSYN, and XFC pins have been added in support of the on-chip PLL.

- For purposes of emulation and development support only, a special 132 PGA version is supported. This version adds back the FC2-0, $\overline{\text{IAC}}$, $\overline{\text{FRZ}}$, and $\overline{\text{AVEC}}$ pins. The FC2-0 pins allow bus cycles to be distinguished between program and data accesses, interrupt cycles, etc. The $\overline{\text{IAC}}$, $\overline{\text{FRZ}}$, and $\overline{\text{AVEC}}$ pins are provided so that emulation vendors can quickly retrofit their existing MC68302 emulator designs to support the MC68LC302.
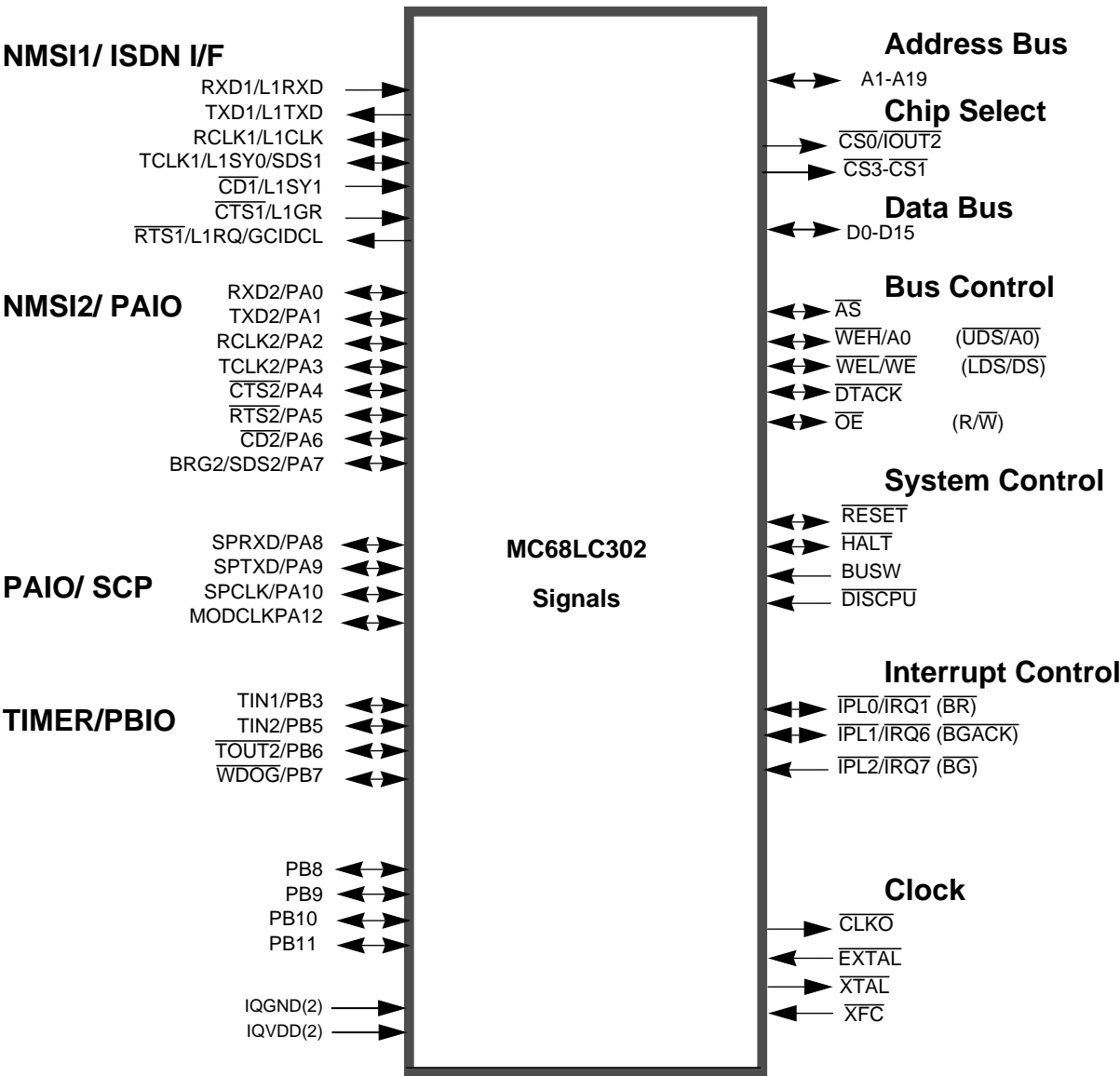
MC68LC302 PRODUCT INFORMATION

MC68LC302 PIN DESCRIPTION

NMSI1/ ISDN I/F

- RXD1/L1RXD
- TXD1/L1TXD
- RCLK1/L1CLK
- TCLK1/L1SY0/SDS1
- $\overline{CD1}$/L1SY1
- $\overline{CTS1}$/L1GR
- $\overline{RTS1}$/L1RQ/GCIDCL

NMSI2/ PAIO

- RXD2/PA0
- TXD2/PA1
- RCLK2/PA2
- TCLK2/PA3
- $\overline{CTS2}$/PA4
- $\overline{RTS2}$/PA5
- $\overline{CD2}$/PA6
- BRG2/SDS2/PA7

PAIO/ SCP

- SPRXD/PA8
- SPTXD/PA9
- SPCLK/PA10
- MODCLKPA12

TIMER/PBIO

- TIN1/PB3
- TIN2/PB5
- $\overline{TOUT2}$/PB6
- $\overline{WDOG}$/PB7

- PB8
- PB9
- PB10
- PB11

- IQGND(2)
- IQVDD(2)

MC68LC302

Signals

Address Bus

- A1-A19

Chip Select

- $\overline{CS0}$/$\overline{IOUT2}$
- $\overline{CS3}$-$\overline{CS1}$

Data Bus

- D0-D15

Bus Control

- $\overline{AS}$
- $\overline{WEH}$/A0   ($\overline{UDS}$/A0)
- $\overline{WEL}$/$\overline{WE}$ ($\overline{LDS}$/DS)
- $\overline{DTACK}$
- $\overline{OE}$ (R/$\overline{W}$)

System Control

- $\overline{RESET}$
- $\overline{HALT}$
- BUSW
- $\overline{DISCPU}$

Interrupt Control

- $\overline{IPL0}$/$\overline{IRQ1}$ ($\overline{BR}$)
- $\overline{IPL1}$/$\overline{IRQ6}$ ($\overline{BGACK}$)
- $\overline{IPL2}$/$\overline{IRQ7}$ ($\overline{BG}$)

Clock

- $\overline{CLKO}$
- $\overline{EXTAL}$
- $\overline{XTAL}$
- $\overline{XFC}$

MC68LC302 PRODUCT INFORMATION

**For More Information On This Product,
Go to: www.freescale.com**

Table 1. MC68LC302 Ordering Information

Package Type	Operating Voltage	Frequency (MHz)	Temperature	Order Number
Pin Grid Array (RC Suffix)	5V	20	0°C to 70°C	MC68LC302RC20
Thin Quad Flat Pack (PU Suffix)	5V 5V 5V 5V	16.67 16.67 20 20	0°C to 70°C −40°C to +85°C 0°C to 70°C −40°C to +85°C	MC68LC302PU16 MC68LC302CPU16 MC68LC302PU20 TBD
Thin Quad Flat Pack (PU Suffix)	3.3V 3.3V 3.3V 3.3V	16.67 16.67 20 20	0°C to 70°C −40°C to +85°C 0°C to 70°C −40°C to +85°C	MC68LC302PU16V MC68LC302CPU16V TBD TBD

Table 2. Documentation

Document Title	Order Number	Contents
MC68302 User's Manual	MC68302UM/AD	Detailed information for design
M68000 Family Programmer's Reference Manual	M68000PM/AD	M68000 Family instruction set
The 68K Source	BR729/D	Independent vendor listing supporting software and development tools
The 68LC302 Addendum		Describes the differences between the MC68302 and the MC68LC302

SEMICONDUCTOR PRODUCT INFORMATION

**For More Information On This Product,
Go to: www.freescale.com**