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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, IrDA, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 13x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f11bbcafp-50">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f11bbcafp-50</a>

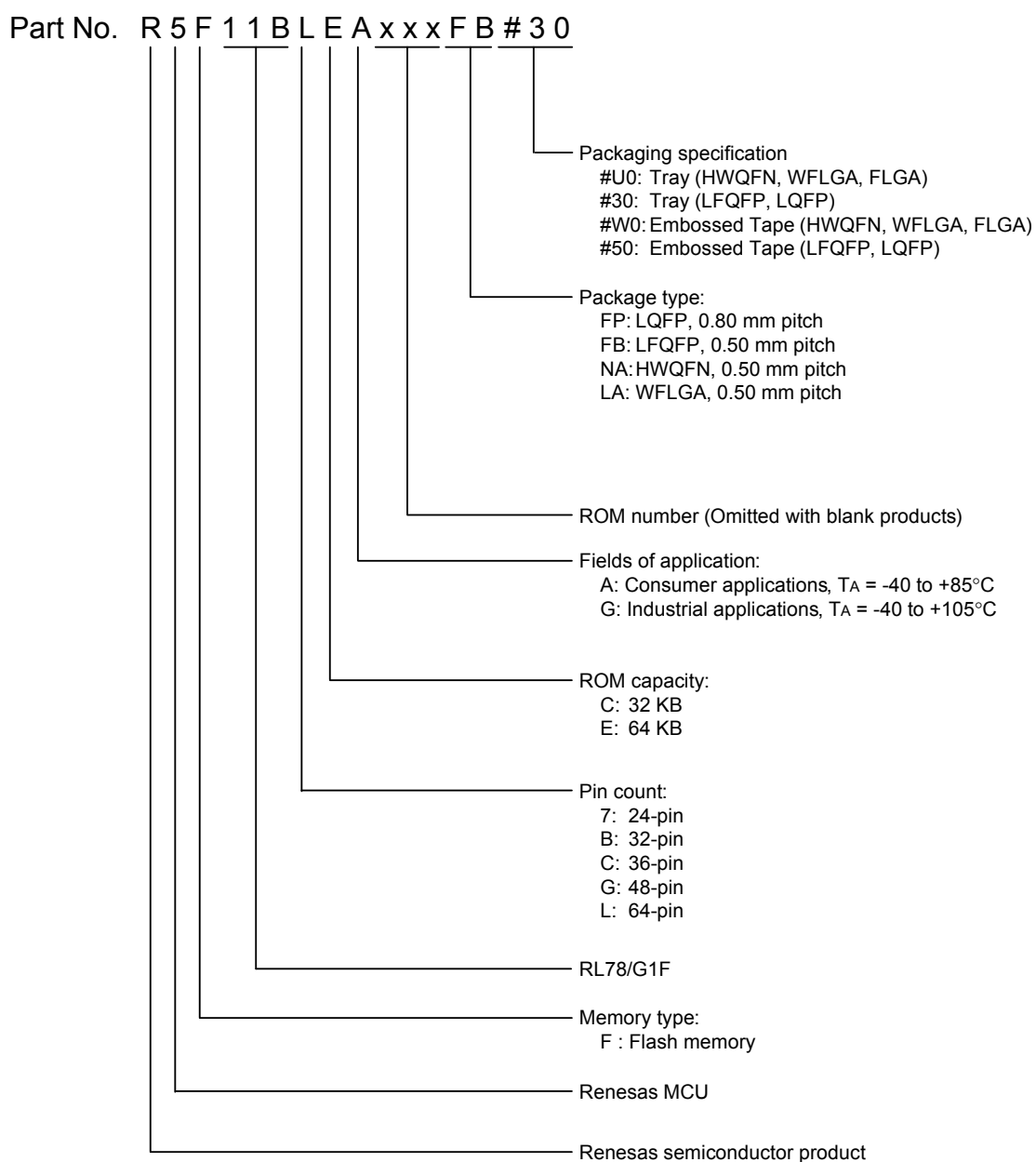
## ○ ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G1F				
			24 pins	32 pins	36 pins	48 pins	64 pins
64 KB	4 KB	5.5 KB <small>Note</small>	R5F11B7E	R5F11BBE	R5F11BCE	R5F11BGE	R5F11BLE
32 KB	4 KB	5.5 KB <small>Note</small>	R5F11B7C	R5F11BBC	R5F11BCC	R5F11BGC	R5F11BLC

**Note** This is about 4.5 KB when performing self-programming and rewriting the data flash memory (For details, see **CHAPTER 3 CPU ARCHITECTURE** in the RL78/G1F User's Manual).

## 1.2 Ordering Information

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G1F



(TA = -40 to +85°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(2/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low Note 1	IOL1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147			20.0 Note 2	mA
		Per pin for P60 to P63			15.0 Note 2	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty ≤ 70% Note 3)	4.0 V ≤ EVDD0 ≤ 5.5 V		70.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		15.0	mA
			1.8 V ≤ EVDD0 < 2.7 V		9.0	mA
			1.6 V ≤ EVDD0 < 1.8 V		4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P55, P60 to P63, P70 to P77, P146, P147 (When duty ≤ 70% Note 3)	4.0 V ≤ EVDD0 ≤ 5.5 V		80.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		35.0	mA
			1.8 V ≤ EVDD0 < 2.7 V		20.0	mA
			1.6 V ≤ EVDD0 < 1.8 V		10.0	mA
		Total of all pins (When duty ≤ 70% Note 3)			150.0	mA
	IOL2	Per pin for P20 to P27			0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	1.6 V ≤ VDD ≤ 5.5 V		5.0	mA

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EVSS0 and VSS pins.

**Note 2.** Do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA

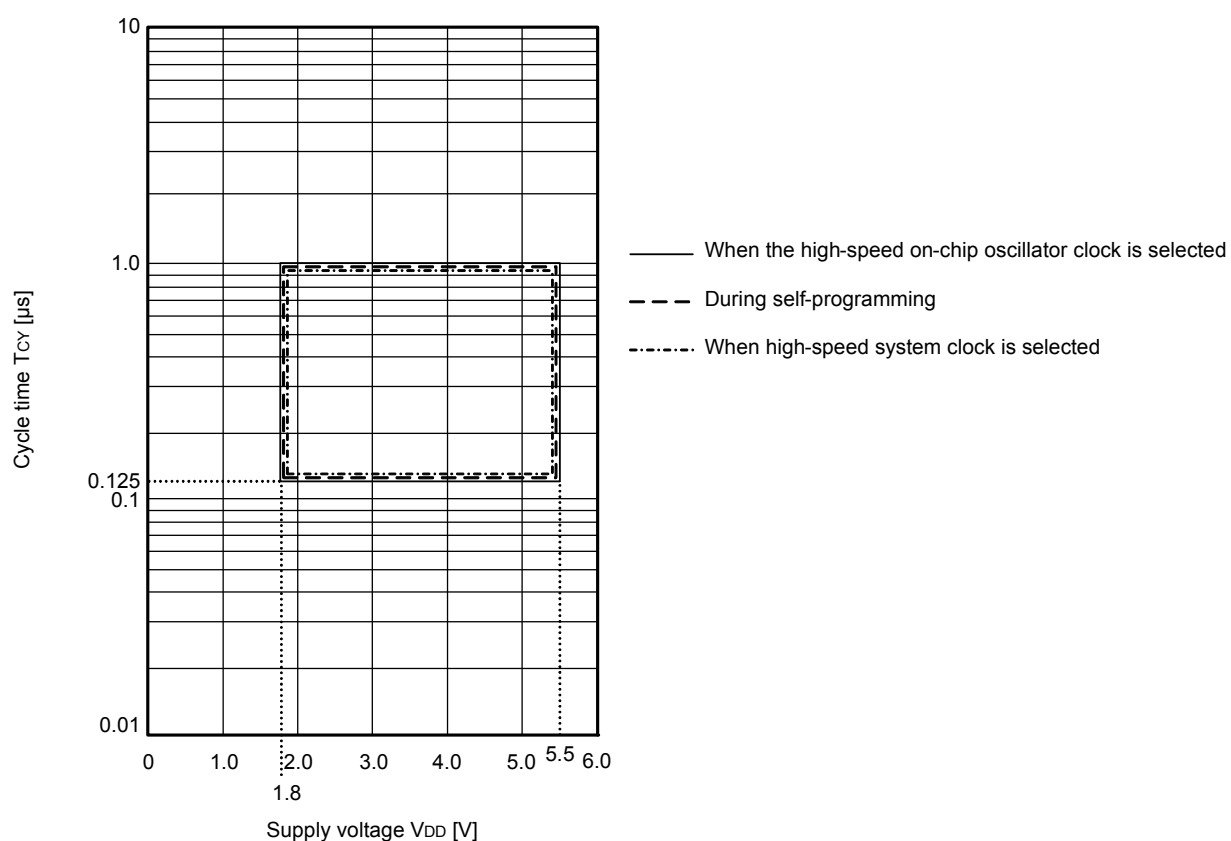
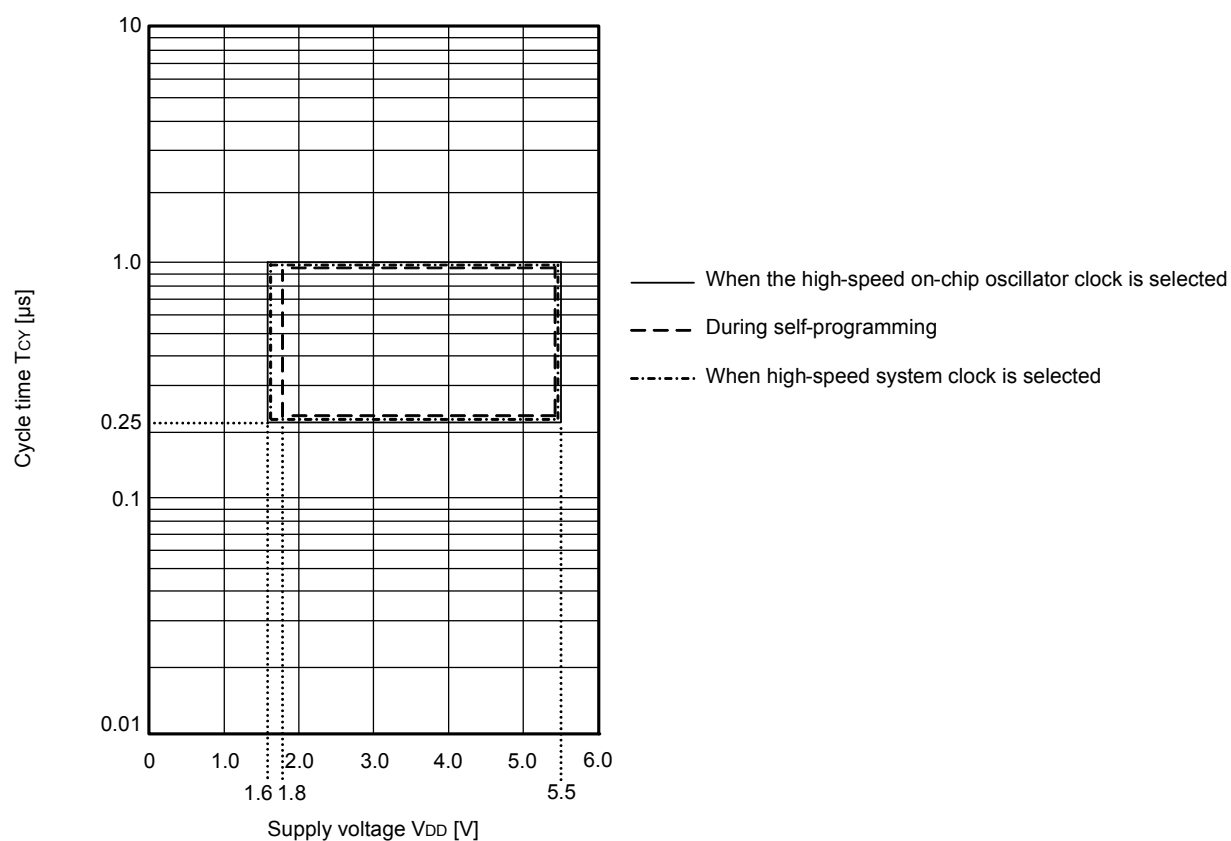
$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \approx 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- Note 11.** Current flowing only to the D/A converter. The supply current of the RL78 microcontrollers is the sum of I<sub>DD1</sub> or I<sub>DD2</sub> and I<sub>DAC</sub> when the D/A converter operates in an operation mode or the HALT mode.
- Note 12.** Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of I<sub>DD1</sub>, I<sub>DD2</sub>, or I<sub>DD3</sub> and I<sub>CMP</sub> when the comparator circuit is in operation.
- Remark 1.** f<sub>IL</sub>: Low-speed on-chip oscillator clock frequency
- Remark 2.** f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 3.** f<sub>CLK</sub>: CPU/peripheral hardware clock frequency
- Remark 4.** Temperature condition of the TYP. value is T<sub>A</sub> = 25°C

T<sub>CY</sub> vs V<sub>DD</sub> (LS (low-speed main) mode)T<sub>CY</sub> vs V<sub>DD</sub> (LV (low-voltage main) mode)

**Note 6.** The smaller maximum transfer rate derived by using  $f_{mck}/6$  or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when  $1.8\text{ V} \leq E_{VDD0} < 3.3\text{ V}$  and  $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

**Note 7.** This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V<sub>DD</sub> tolerance (for the 48-, 32-, 24-pin products)/E<sub>VDD</sub> tolerance (for the 64-, 36-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)****(TA = -40 to +85°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)****(1/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t <sub>KCY1</sub>	t <sub>KCY1</sub> ≥ 4/f <sub>CLK</sub> 4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ	300		1150		1150		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ	500		1150		1150		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <i>Note</i> , C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ	1150		1150		1150		ns
SCKp high-level width	t <sub>KH1</sub>	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ	t <sub>KCY1</sub> /2 - 75		t <sub>KCY1</sub> /2 - 75		t <sub>KCY1</sub> /2 - 75		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ	t <sub>KCY1</sub> /2 - 170		t <sub>KCY1</sub> /2 - 170		t <sub>KCY1</sub> /2 - 170		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <i>Note</i> , C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ	t <sub>KCY1</sub> /2 - 458		t <sub>KCY1</sub> /2 - 458		t <sub>KCY1</sub> /2 - 458		ns
SCKp low-level width	t <sub>KL1</sub>	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ	t <sub>KCY1</sub> /2 - 12		t <sub>KCY1</sub> /2 - 50		t <sub>KCY1</sub> /2 - 50		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ	t <sub>KCY1</sub> /2 - 18		t <sub>KCY1</sub> /2 - 50		t <sub>KCY1</sub> /2 - 50		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <i>Note</i> , C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ	t <sub>KCY1</sub> /2 - 50		t <sub>KCY1</sub> /2 - 50		t <sub>KCY1</sub> /2 - 50		ns

**Note** Use it with EVDD0 ≥ V<sub>b</sub>.

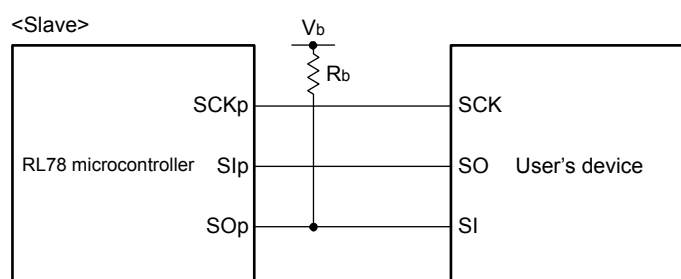
**Caution** Select the TTL input buffer for the SIp pin and the N-ch open drain output (V<sub>DD</sub> tolerance (for the 48-, 32-, 24-pin products)/EV<sub>DD</sub> tolerance (for the 64-, 36-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)



- Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps
- Note 2.** Use it with  $EV_{DD0} \geq V_b$ .
- Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 5.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Caution** Select the TTL input buffer for the SIp pin and SCKp pin, and the N-ch open drain output (V<sub>DD</sub> tolerance (for the 48-, 32-, 24-pin products)/EV<sub>DD</sub> tolerance (for the 64-, 36-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

#### CSI mode connection diagram (during communication at different potential)



- Remark 1.** R<sub>b</sub>[Ω]: Communication line (SO<sub>p</sub>) pull-up resistance, C<sub>b</sub>[F]: Communication line (SO<sub>p</sub>) load capacitance, V<sub>b</sub>[V]: Communication line voltage
- Remark 2.** p: CSI number (p = 00, 01, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 7)
- Remark 3.** f<sub>MCK</sub>: Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  
m: Unit number, n: Channel number (mn = 00, 01, 02, 10))
- Remark 4.** CSI01 of 48-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.  
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

## 2.6.2 Temperature sensor characteristics/internal reference voltage characteristic

(TA = -40 to +85°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	VTMPS25	Setting ADS register = 80H, TA = +25°C		1.05		V
Internal reference voltage	VBGR	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	FVTMPS	Temperature sensor that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	tAMP		5			μs

## 2.6.3 D/A converter characteristics

(TA = -40 to +85°C, 1.6 V ≤ EVSS0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 MΩ	1.8 V ≤ VDD ≤ 5.5 V			±2.5	LSB
		Rload = 8 MΩ	1.8 V ≤ VDD ≤ 5.5 V			±2.5	LSB
Settling time	tSET	Cload = 20 pF	2.7 V ≤ VDD ≤ 5.5 V			3	μs
			1.6 V ≤ VDD < 2.7 V			6	μs

### 3.1 Absolute Maximum Ratings

Absolute Maximum Ratings

(1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V <sub>DD</sub>		-0.5 to +6.5	V
	EV <sub>DD0</sub>		-0.5 to +6.5	V
REGC pin input voltage	V <sub>I<sub>REGC</sub></sub>	REGC	-0.3 to +2.8 and -0.3 to V <sub>DD</sub> +0.3 Note 1	V
Input voltage	V <sub>I1</sub>	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147	-0.3 to EV <sub>DD0</sub> +0.3 and -0.3 to V <sub>DD</sub> +0.3 Note 2	V
	V <sub>I2</sub>	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V <sub>I3</sub>	P20 to P27, P121 to P124, P137, EXCLK, EXCLKS, RESET	-0.3 to V <sub>DD</sub> +0.3 Note 2	V
Output voltage	V <sub>O1</sub>	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P60 to P63, P70 to P77, P120, P130, P140, P141, P146, P147	-0.3 to EV <sub>DD0</sub> +0.3 and -0.3 to V <sub>DD</sub> +0.3 Note 2	V
	V <sub>O2</sub>	P20 to P27	-0.3 to V <sub>DD</sub> +0.3 Note 2	V
Analog input voltage	V <sub>AI1</sub>	ANI16 to ANI24	-0.3 to EV <sub>DD0</sub> +0.3 and -0.3 to AV <sub>REF</sub> (+) +0.3 Notes 2, 3	V
	V <sub>AI2</sub>	ANI0 to ANI7	-0.3 to V <sub>DD</sub> +0.3 and -0.3 to AV <sub>REF</sub> (+) +0.3 Notes 2, 3	V

**Note 1.** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**Note 2.** Must be 6.5 V or lower.

**Note 3.** Do not exceed AV<sub>REF</sub> (+) + 0.3 V in case of A/D conversion target pin.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**Remark 2.** AV<sub>REF</sub> (+): + side reference voltage of the A/D converter.

**Remark 3.** V<sub>SS</sub>: Reference voltage

### 3.3 DC Characteristics

#### 3.3.1 Pin characteristics

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high <sup>Note 1</sup>	IOH1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147			-3.0 <sup>Note 2</sup>	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ EVDD0 ≤ 5.5 V		-30.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		-10.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		-5.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P53, P70 to P77, P146, P147 (When duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ EVDD0 ≤ 5.5 V		-30.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		-19.0	mA
			1.8 V ≤ EVDD0 < 2.7 V		-10.0	mA
		Total of all pins (When duty ≤ 70% <sup>Note 3</sup> )			-60.0	mA
	IOH2	Per pin for P20 to P27			-0.1 <sup>Note 2</sup>	mA
		Total of all pins (When duty ≤ 70% <sup>Note 3</sup> )	2.4 V ≤ VDD ≤ 5.5 V		-1.5	mA

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from the EVDD0, VDD pins to an output pin.

**Note 2.** Do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOH × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOH = -10.0 mA

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \approx -8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

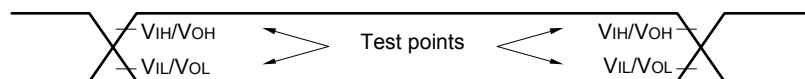
**Caution** P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43, P50 to P55, P71, P74 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- Note 11.** Current flowing only to the D/A converter. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2 and IDAC when the D/A converter operates in an operation mode or the HALT mode.
- Note 12.** Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2, or IDD3 and ICMP when the comparator circuit is in operation.
- Remark 1.** f<sub>IL</sub>: Low-speed on-chip oscillator clock frequency
- Remark 2.** f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 3.** f<sub>CLK</sub>: CPU/peripheral hardware clock frequency
- Remark 4.** Temperature condition of the TYP. value is TA = 25°C

### 3.5 Peripheral Functions Characteristics

#### AC Timing Test Points



#### 3.5.1 Serial array unit

##### (1) During communication at same potential (UART mode)

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 ≤ 5.5 V, Vss = EVSS0 = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate Note 1		2.4 V ≤ EVDD0 ≤ 5.5 V		fMCK/12 Note 2	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note 3		2.6	Mbps

**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

**Note 2.** The following conditions are required for low voltage interface when EVDD0 < VDD.

2.4 V ≤ EVDD0 < 2.7 V: MAX.1.3 Mbps

**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

HS (high-speed main) mode: 32 MHz (2.7 V ≤ VDD ≤ 5.5 V)

16 MHz (2.4 V ≤ VDD ≤ 5.5 V)

**Caution** Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**(4) During communication at same potential (simplified I<sup>2</sup>C mode)****(TA = -40 to +105°C, 2.4 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f <sub>SCL</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ		400 Note 1	kHz
		2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ		100 Note 1	kHz
Hold time when SCLr = "L"	t <sub>LOW</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1200		ns
		2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ	4600		ns
Hold time when SCLr = "H"	t <sub>HIGH</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1200		ns
		2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ	4600		ns
Data setup time (reception)	t <sub>SU: DAT</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 220 Note 2		ns
		2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ	1/f <sub>MCK</sub> + 580 Note 2		ns
Data hold time (transmission)	t <sub>HD: DAT</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	0	770	ns
		2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ	0	1420	ns

**Note 1.** The value must also be equal to or less than f<sub>MCK</sub>/4.**Note 2.** Set the f<sub>MCK</sub> value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution** Select the normal input buffer and the N-ch open drain output (V<sub>DD</sub> tolerance (for the 48-, 32-, 24-pin products)/EV<sub>DD</sub> tolerance (for the 64-, 36-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)****(TA = -40 to +105°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)****(2/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp↑) <sup>Note</sup>	tsik1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	162		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	354		ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ	958		ns
Slp hold time (from SCKp↑) <sup>Note</sup>	tkS11	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	38		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	38		ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ	38		ns
Delay time from SCKp↓ to SOp output <sup>Note</sup>	tkSO1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		200	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		390	ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ		966	ns

**Note** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance (for the 48-, 32-, 24-pin products)/EVDD tolerance (for the 64-, 36-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)



**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)****(TA = -40 to +105°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)****(3/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp↓) <sup>Note</sup>	tsIK1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	88		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	88		ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ	220		ns
Slp hold time (from SCKp↓) <sup>Note</sup>	tkS11	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	38		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	38		ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ	38		ns
Delay time from SCKp↑ to SOp output <sup>Note</sup>	tkSO1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		50	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		50	ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ		50	ns

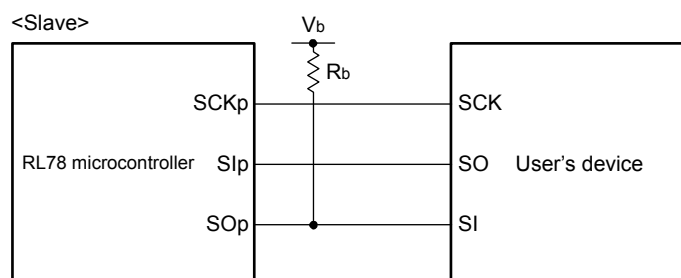
**Note** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance (for the 48-, 32-, 24-pin products)/EVDD tolerance (for the 64-, 36-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

- Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps
- Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 5.** Select the TTL input buffer for the SIp pin and SCKp pin, and the N-ch open drain output (VDD tolerance (for the 48, 32, 24-pin products)/EVDD tolerance (for the 64, 36-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

**CSI mode connection diagram (during communication at different potential)**



- Remark 1.** Rb[Ω]: Communication line (SOp) pull-up resistance, Cb[F]: Communication line (SOp) load capacitance, Vb[V]: Communication line voltage
- Remark 2.** p: CSI number (p = 00, 01, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 7)
- Remark 3.** fMCK: Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  
m: Unit number, n: Channel number (mn = 00, 01, 02, 10))
- Remark 4.** CSI01 of 48-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.  
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I<sup>2</sup>C mode)****(TA = -40 to +105°C, 2.4 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V)****(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f <sub>SCL</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ		400 Note 1	kHz
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ		400 Note 1	kHz
		4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.8 kΩ		100 Note 1	kHz
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ		100 Note 1	kHz
		2.4 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ		100 Note 1	kHz
Hold time when SCLr = "L"	t <sub>LOW</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1200		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1200		ns
		4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.8 kΩ	4600		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	4600		ns
		2.4 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	4650		ns
Hold time when SCLr = "H"	t <sub>HIGH</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	620		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	500		ns
		4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.8 kΩ	2700		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	2400		ns
		2.4 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	1830		ns

**(2) Interrupt & Reset Mode****(TA = -40 to +105°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Voltage detection threshold	VLVDD0	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage		2.64	2.75	2.86	V
	VLVDD1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	VLVDD2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V
	VLVDD3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
			Falling interrupt voltage	3.83	3.98	4.13	V

**3.6.8 Power supply voltage rising slope characteristics****(TA = -40 to +105°C, VSS = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SVDD				54	V/ms

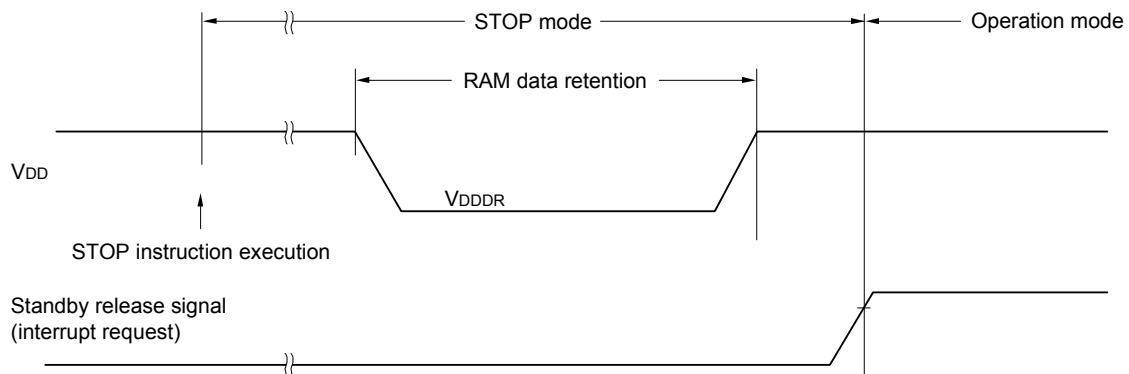
**Caution** Make sure to keep the internal reset state by the LVD circuit or an external reset until VDD reaches the operating voltage range shown in 3.4 AC Characteristics.

**3.7 RAM Data Retention Characteristics****(TA = -40 to +105°C, VSS = 0V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.44 Notes 1, 2		5.5	V

**Note 1.** The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.

**Note 2.** Enter STOP mode before the supply voltage falls below the recommended operating voltage.

**3.8 Flash Memory Programming Characteristics****(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK	2.4 V ≤ VDD ≤ 5.5 V	1		32	MHz

4.5 64-pin products

R5F11BLCAFB, R5F11BLEAFB, R5F11BLCGFB, R5F11BLEGFB

