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What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.
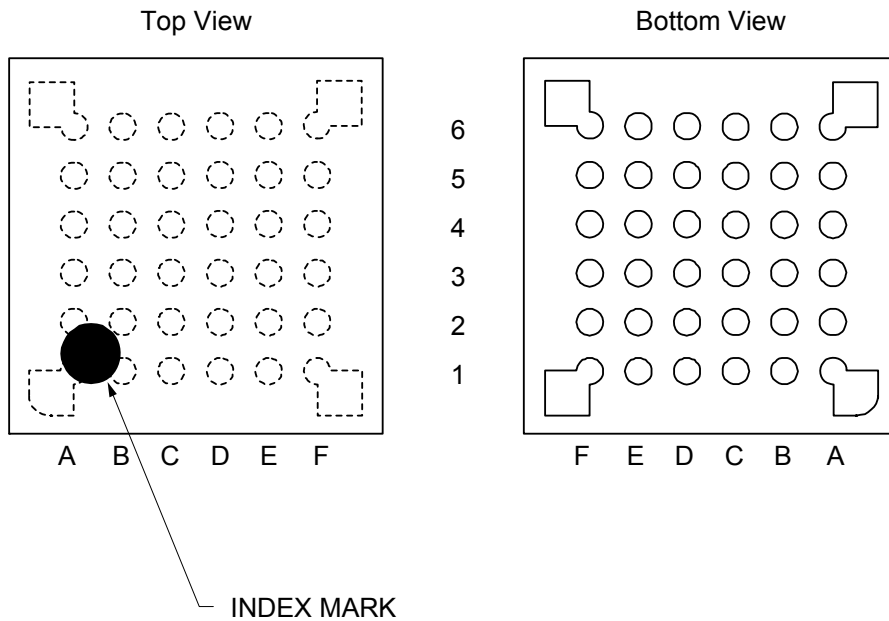
Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, IrDA, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 13x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f11bbeafp-30

1.3.3   36-pin products

• 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)

INDEX MARK

	A	B	C	D	E	F	
6	EV$_{DD0}$	V$_{DD}$	P121/X1	P122/X2/EXCLK	P137/INTP0	P40/TOOL0	6
5	P61/SDAA0	P60/SCLA0	V$_{SS}$	REGC	RESET	P124/XT2/ EXCLKS	5
4	P31/TI03/TO03/ INTP4/PCLBUZ0/ $\overline{SSI00}$/(TRJIO0)/ VCOUT1	P14/ANI24/RxD2/ SI20/SDA20/ TRDIOD0/ (SCLA0)/IrRxD	P20/ANI0/ AV$_{REFP}$/IVCMP12/ INTP11	P21/ANI1/ AV$_{REFM}$/IVCMP13	P01/ANI16/TO00/ RxD1/TRGCLKB/ TRJIO0/INTP10/ IVCMP11	P123/XT1	4
3	P50/INTP1/SI00/ RxD0/TOOLRxD/ SDA00/TRGIOA/ (TRJO0)/ (TRDIOC1)	P70/INTP6/ (VCOUT0)/ (VCOUT1)	P15/PCLBUZ1/ SCK20/SCL20/ TRDIOB0/ (SDAA0)	P23/ANI3/ANO1/ PGAGND	P00/ANI17/TI00/ TxD1/TRGCLKA/ (TRJO0)/INTP8/ IVCMP10	P120/ANI19/ VCOUT0	3
2	P30/INTP3/ RTC1HZ/SCK00/ SCL00/TRJO0/ (TRDIOB1)	P16/TI01/TO01/ INTP5/TRDIOC0/ (RxD0)/ (TRDIOA1)	P12/ANI22/SO11/ TRDIOB1	P11/ANI21/SI11/ SDA11/TRDIOC1	P24/ANI4	P22/ANI2/ANO0/ PGAI/IVCMP0	2
1	P51/INTP2/SO00/ TxD0/TOOLTxD/ TRGIOB/ (TRDIOD1)	P17/TI02/TO02/ TRDIOA0/ TRDCLK0/(TxD0)/ (TRDIOD0)	P13/ANI23/TxD2/ SO20/TRDIOA1/ IrTxD	P10/ANI20/ SCK11/SCL11/ TRDIOD1/(TxD2)	P147/ANI18/ IVREF0	P25/ANI5	1
	A	B	C	D	E	F	

Caution 1. Connect the REGC pin to V$_{SS}$ pin via a capacitor (0.47 to 1 μF).
Caution 2. Make V$_{DD}$ pin the potential that is higher than EV$_{DD0}$ pin.

Remark 1. For pin identification, see **1.4 Pin Identification**.
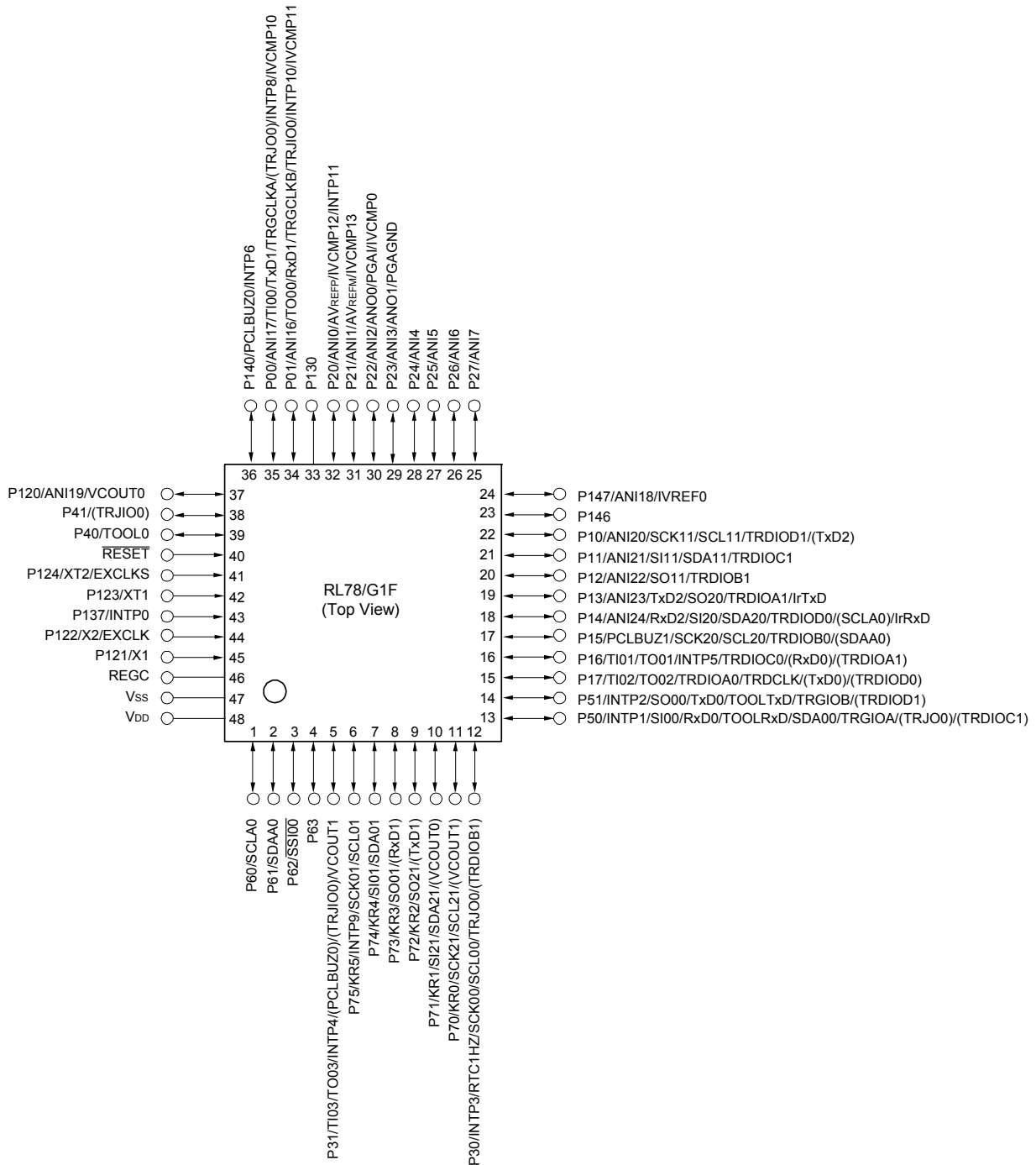**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).
Remark 3. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V$_{DD}$ and EV$_{DD0}$ pins.

1.3.4 48-pin products

• 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)

<R>

Top-edge pins (left to right, 36 to 25):
P140/PCLBUZ0/INTP6
P00/ANI17/TI00/TxD1/TRGCLKA/(TRJO0)/INTP8/IVCMP10
P01/ANI16/TO00/RxD1/TRGCLKB/TRJIO0/INTP10/IVCMP11
P130
P20/ANI0/AV$_{REFP}$/IVCMP12/INTP11
P21/ANI1/AV$_{REFM}$/IVCMP13
P22/ANI2/ANO0/PGAI/IVCMP0
P23/ANI3/ANO1/PGAGND
P24/ANI4
P25/ANI5
P26/ANI6
P27/ANI7

Left-edge pins (37 to 48):
37 P120/ANI19/VCOUT0
38 P41/(TRJIO0)
39 P40/TOOL0
40 $\overline{\text{RESET}}$
41 P124/XT2/EXCLKS
42 P123/XT1
43 P137/INTP0
44 P122/X2/EXCLK
45 P121/X1
46 REGC
47 V$_{SS}$
48 V$_{DD}$

RL78/G1F (Top View)

Right-edge pins (24 to 13):
24 P147/ANI18/IVREF0
23 P146
22 P10/ANI20/SCK11/SCL11/TRDIOD1/(TxD2)
21 P11/ANI21/SI11/SDA11/TRDIOC1
20 P12/ANI22/SO11/TRDIOB1
19 P13/ANI23/TxD2/SO20/TRDIOA1/IrTxD
18 P14/ANI24/RxD2/SI20/SDA20/TRDIOD0/(SCLA0)/IrRxD
17 P15/PCLBUZ1/SCK20/SCL20/TRDIOB0/(SDAA0)
16 P16/TI01/TO01/INTP5/TRDIOC0/(RxD0)/(TRDIOA1)
15 P17/TI02/TO02/TRDIOA0/TRDCLK/(TxD0)/(TRDIOD0)
14 P51/INTP2/SO00/TxD0/TOOLTxD/TRGIOB/(TRDIOD1)
13 P50/INTP1/SI00/RxD0/TOOLRxD/SDA00/TRGIOA/(TRJO0)/(TRDIOC1)

Bottom-edge pins (left to right, 1 to 12):
P60/SCLA0
P61/SDAA0
P62/SSI00
P63
P31/TI03/TO03/INTP4/(PCLBUZ0)/(TRJIO0)/VCOUT1
P75/KR5/INTP9/SCK01/SCL01
P74/KR4/SI01/SDA01
P73/KR3/SO01/(RxD1)
P72/KR2/SO21/(TxD1)
P71/KR1/SI21/SDA21/(VCOUT0)
P70/KR0/SCK21/SCL21/(VCOUT1)
P30/INTP3/RTC1HZ/SCK00/SCL00/TRJO0/(TRDIOB1)

Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).

Absolute Maximum Ratings (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P40 to P43,P120, P130, P140, P141	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P55, P70 to P77, P146, P147	-100	mA
	I_{OH2}	Per pin	P20 to P27	-0.5	mA
		Total of all pins		-2	mA
Output current, low	I_{OL1}	Per pin	P00 to P06, P10 to P17, P30, P31, P40-P43, P50 to P55, P60 to P63, P70 to P77, P120, P130, P140, P141, P146, P147	40	mA
		Total of all pins 170 mA	P00 to P04, P40 to P47, P120, P130, P140, P141	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P55, P70 to P77, P146, P147	100	mA
	I_{OL2}	Per pin	P20 to P27	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		-40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

Caution   **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(T_A = -40 to +85°C, 1.6 V $\leq$ EV_{DD0} $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol			Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V			2.4		mA
						V_{DD} = 3.0 V			2.4		
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V			2.1		
						V_{DD} = 3.0 V			2.1		
			HS (high-speed main) mode Note 5	f_{HOCO} = 64 MHz, f_{IH} = 32 MHz Note 3	Normal operation	V_{DD} = 5.0 V			5.2	8.7	mA
						V_{DD} = 3.0 V			5.2	8.7	
				f_{HOCO} = 32 MHz, f_{IH} = 32 MHz Note 3	Normal operation	V_{DD} = 5.0 V			4.8	8.1	
						V_{DD} = 3.0 V			4.8	8.1	
				f_{HOCO} = 48 MHz, f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V			4.1	6.9	
						V_{DD} = 3.0 V			4.1	6.9	
				f_{HOCO} = 24 MHz, f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V			3.8	6.3	
						V_{DD} = 3.0 V			3.8	6.3	
				f_{HOCO} = 16 MHz, f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V			2.8	4.6	
						V_{DD} = 3.0 V			2.8	4.6	
			LS (low-speed main) mode Note 5	f_{HOCO} = 8 MHz, f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V			1.3	2.1	mA
						V_{DD} = 2.0 V			1.3	2.1	
			LV (low-voltage main) mode Note 5	f_{HOCO} = 4 MHz, f_{IH} = 4 MHz Note 3	Normal operation	V_{DD} = 3.0 V			1.3	1.9	mA
						V_{DD} = 2.0 V			1.3	1.9	
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input			3.3	5.3	mA
						Resonator connection			3.5	5.5	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input			3.3	5.3	
						Resonator connection			3.5	5.5	
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input			2	3.1	
						Resonator connection			2.1	3.2	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input			2	3.1	
						Resonator connection			2.1	3.2	
			LS (low-speed main) mode Note 5	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input			1.2	1.9	mA
						Resonator connection			1.2	2	
				f_{MX} = 8 MHz Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input			1.2	1.9	
						Resonator connection			1.2	2	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4, T_A = -40°C	Normal operation	Square wave input			4.7	6.1	μA
						Resonator connection			4.7	6.1	
				f_{SUB} = 32.768 kHz Note 4, T_A = +25°C	Normal operation	Square wave input			4.7	6.1	
						Resonator connection			4.7	6.1	
				f_{SUB} = 32.768 kHz Note 4, T_A = +50°C	Normal operation	Square wave input			4.8	6.7	
						Resonator connection			4.8	6.7	
				f_{SUB} = 32.768 kHz Note 4, T_A = +70°C	Normal operation	Square wave input			4.8	7.5	
						Resonator connection			4.8	7.5	
				f_{SUB} = 32.768 kHz Note 4, T_A = +85°C	Normal operation	Square wave input			5.4	8.9	
						Resonator connection			5.4	8.9	

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Total current flowing into V$_{DD}$ and EV$_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$ or V$_{SS}$, EV$_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 3. When high-speed system clock and subsystem clock are stopped.

Note 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

Note 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V@1 MHz to 32 MHz

2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V@1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V@1 MHz to 8 MHz

LV (low-voltage main) mode: 1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V@1 MHz to 4 MHz

Remark 1. f$_{MX}$:   High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f$_{HOCO}$:   High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f$_{IH}$:   High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. f$_{SUB}$:   Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation, temperature condition of the TYP. value is T$_A$ = 25°C

(T$_A$ = -40 to +85°C, 1.6 V ≤ EV$_{DD0}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = 0 V) **(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I$_{DD2}$ Note 2	HALT mode	HS (high-speed main) mode Note 7	f$_{HOCO}$ = 64 MHz, f$_{IH}$ = 32 MHz Note 4	V$_{DD}$ = 5.0 V		0.8	3.09	mA
					V$_{DD}$ = 3.0 V		0.8	3.09	
				f$_{HOCO}$ = 32 MHz, f$_{IH}$ = 32 MHz Note 4	V$_{DD}$ = 5.0 V		0.54	2.4	
					V$_{DD}$ = 3.0 V		0.54	2.4	
				f$_{HOCO}$ = 48 MHz, f$_{IH}$ = 24 MHz Note 4	V$_{DD}$ = 5.0 V		0.62	2.4	
					V$_{DD}$ = 3.0 V		0.62	2.4	
				f$_{HOCO}$ = 24 MHz, f$_{IH}$ = 24 MHz Note 4	V$_{DD}$ = 5.0 V		0.44	1.83	
					V$_{DD}$ = 3.0 V		0.44	1.83	
				f$_{HOCO}$ = 16 MHz, f$_{IH}$ = 16 MHz Note 4	V$_{DD}$ = 5.0 V		0.4	1.38	
					V$_{DD}$ = 3.0 V		0.4	1.38	
			LS (low-speed main) mode Note 7	f$_{HOCO}$ = 8 MHz, f$_{IH}$ = 8 MHz Note 4	V$_{DD}$ = 3.0 V		260	790	µA
					V$_{DD}$ = 2.0 V		260	790	
			LV (low-voltage main) mode Note 7	f$_{HOCO}$ = 4 MHz, f$_{IH}$ = 4 MHz Note 4	V$_{DD}$ = 3.0 V		420	830	µA
					V$_{DD}$ = 2.0 V		420	830	
			HS (high-speed main) mode Note 7	f$_{MX}$ = 20 MHz Note 3, V$_{DD}$ = 5.0 V	Square wave input		0.28	1.55	mA
					Resonator connection		0.49	1.74	
				f$_{MX}$ = 20 MHz Note 3, V$_{DD}$ = 3.0 V	Square wave input		0.28	1.55	
					Resonator connection		0.49	1.74	
				f$_{MX}$ = 10 MHz Note 3, V$_{DD}$ = 5.0 V	Square wave input		0.19	0.86	
					Resonator connection		0.3	0.93	
				f$_{MX}$ = 10 MHz Note 3, V$_{DD}$ = 3.0 V	Square wave input		0.19	0.86	
					Resonator connection		0.3	0.93	
			LS (low-speed main) mode Note 7	f$_{MX}$ = 8 MHz Note 3, V$_{DD}$ = 3.0 V	Square wave input		95	640	µA
					Resonator connection		145	680	
				f$_{MX}$ = 8 MHz Note 3, V$_{DD}$ = 2.0 V	Square wave input		95	640	
					Resonator connection		145	680	
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz Note 5, T$_A$ = -40°C	Square wave input		0.25	0.57	µA
					Resonator connection		0.44	0.76	
				f$_{SUB}$ = 32.768 kHz Note 5, T$_A$ = 25°C	Square wave input		0.3	0.57	
					Resonator connection		0.49	0.76	
				f$_{SUB}$ = 32.768 kHz Note 5, T$_A$ = 50°C	Square wave input		0.36	1.17	
					Resonator connection		0.59	1.36	
				f$_{SUB}$ = 32.768 kHz Note 5, T$_A$ = 70°C	Square wave input		0.49	1.97	
					Resonator connection		0.72	2.16	
				f$_{SUB}$ = 32.768 kHz Note 5, T$_A$ = 85°C	Square wave input		0.97	3.37	
					Resonator connection		1.16	3.56	
	I$_{DD3}$ Note 6	STOP mode Note 8	T$_A$ = -40°C				0.18	0.51	µA
			T$_A$ = +25°C				0.24	0.51	
			T$_A$ = +50°C				0.29	1.1	
			T$_A$ = +70°C				0.41	1.9	
			T$_A$ = +85°C				0.9	3.3	

(**Notes** and **Remarks** are listed on the next page.)

(T_A = -40 to +85°C, 1.6 V $\leq$ EV$_{DD0}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = 0 V) (2/2)

| Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Timer RD input high-level width, low-level width	t_{TDIH}, t_{TDIL}	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1		$3/f_{CLK}$			ns
Timer RD forced cutoff signal input low-level width	t_{TDSIL}	P130/INTP0	2MHz < f_{CLK} $\leq$ 32 MHz	1			µs
			f_{CLK} $\leq$ 2 MHz	$1/f_{CLK}$ + 1			
Timer RG input high-level width, low-level width	t_{TGIH}, t_{TGIL}	TRGIOA, TRGIOB		$2.5/f_{CLK}$			ns
TO00 to TO03, TRJIO0, TRJO0, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRGIOA, TRGIOB output frequency	f_{TO}	HS (high-speed main) mode	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			16	MHz
			2.7 V $\leq$ EV$_{DD0}$ < 4.0 V			8	MHz
			1.8 V $\leq$ EV$_{DD0}$ < 2.7 V			4	MHz
			1.6 V $\leq$ EV$_{DD0}$ < 1.8 V			2	MHz
		LS (low-speed main) mode	1.8 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			4	MHz
			1.6 V $\leq$ EV$_{DD0}$ < 1.8 V			2	MHz
		LV (low-voltage main) mode	1.6 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			16	MHz
			2.7 V $\leq$ EV$_{DD0}$ < 4.0 V			8	MHz
			1.8 V $\leq$ EV$_{DD0}$ < 2.7 V			4	MHz
			1.6 V $\leq$ EV$_{DD0}$ < 1.8 V			2	MHz
		LS (low-speed main) mode	1.8 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			4	MHz
			1.6 V $\leq$ EV$_{DD0}$ < 1.8 V			2	MHz
		LV (low-voltage main) mode	1.8 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			4	MHz
			1.6 V $\leq$ EV$_{DD0}$ < 1.8 V			2	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0	1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	1			µs
		INTP1 to INTP11	1.6 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V	1			µs
Key interrupt input low-level width	t_{KR}	KR0 to KR7	1.8 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V	250			ns
			1.6 V $\leq$ EV$_{DD0}$ < 1.8 V	1			µs
$\overline{RESET}$ low-level width	t_{RSL}			10			µs

T$_{CY}$ vs V$_{DD}$ (LS (low-speed main) mode)
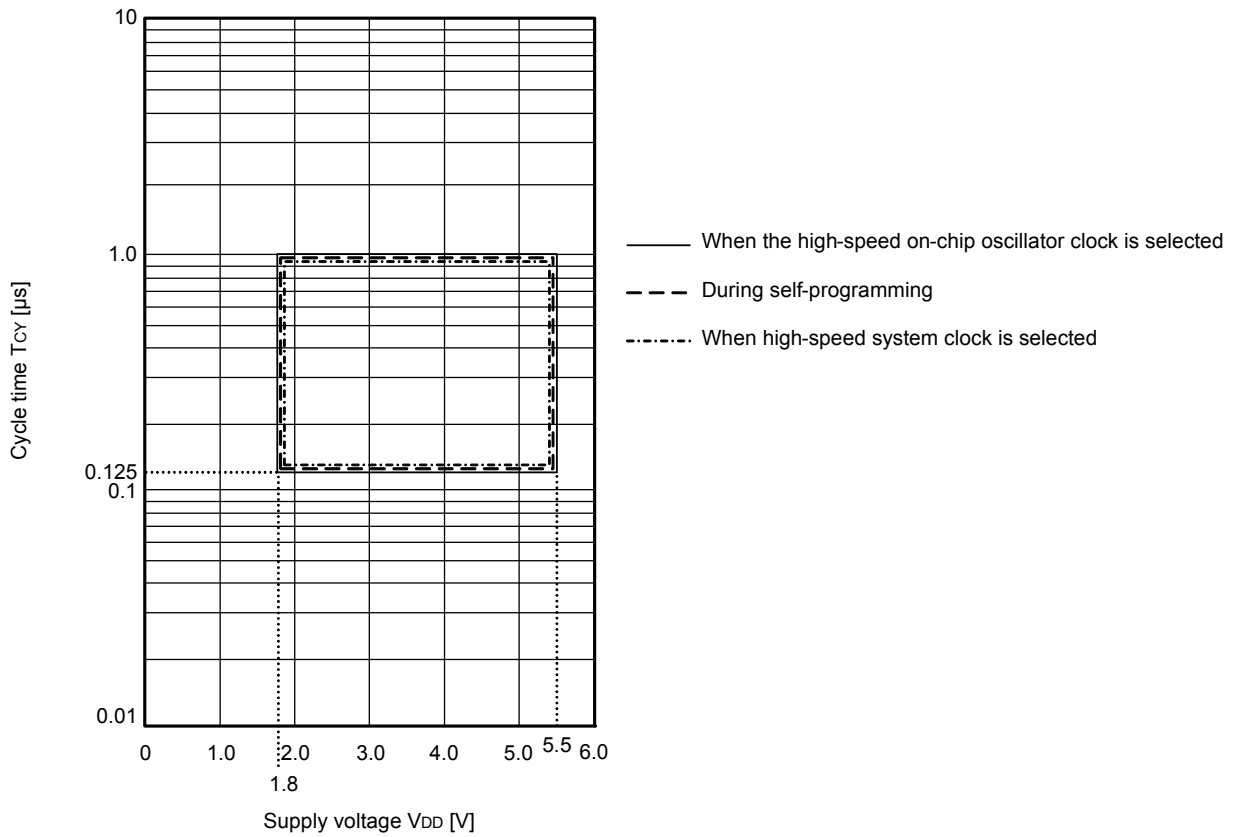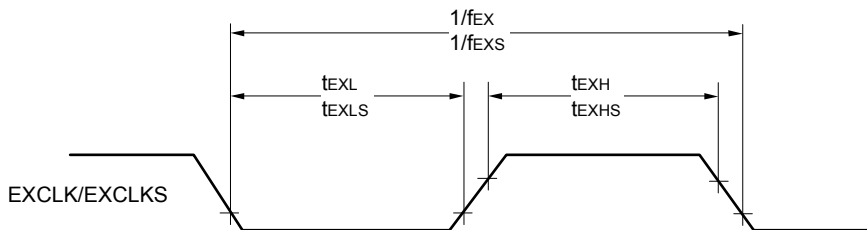

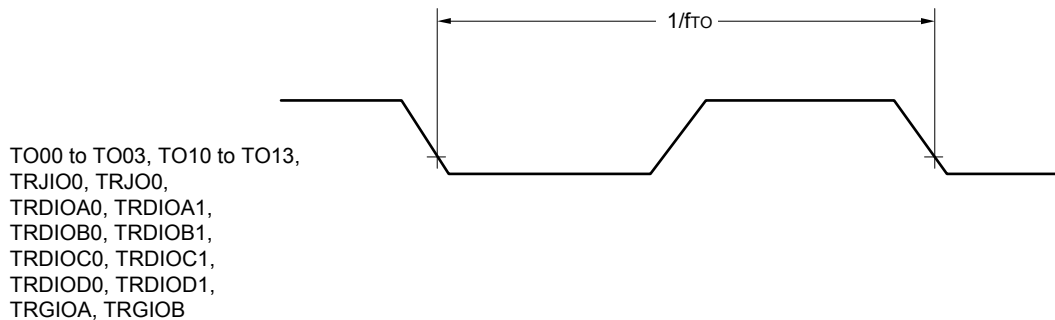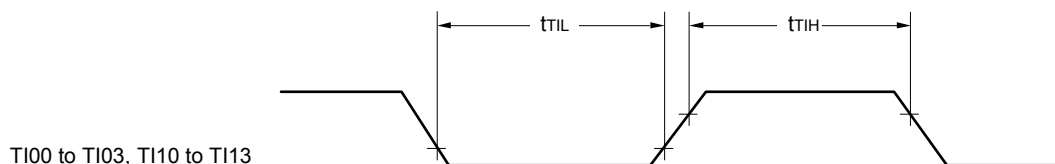T$_{CY}$ vs V$_{DD}$ (LV (low-voltage main) mode)
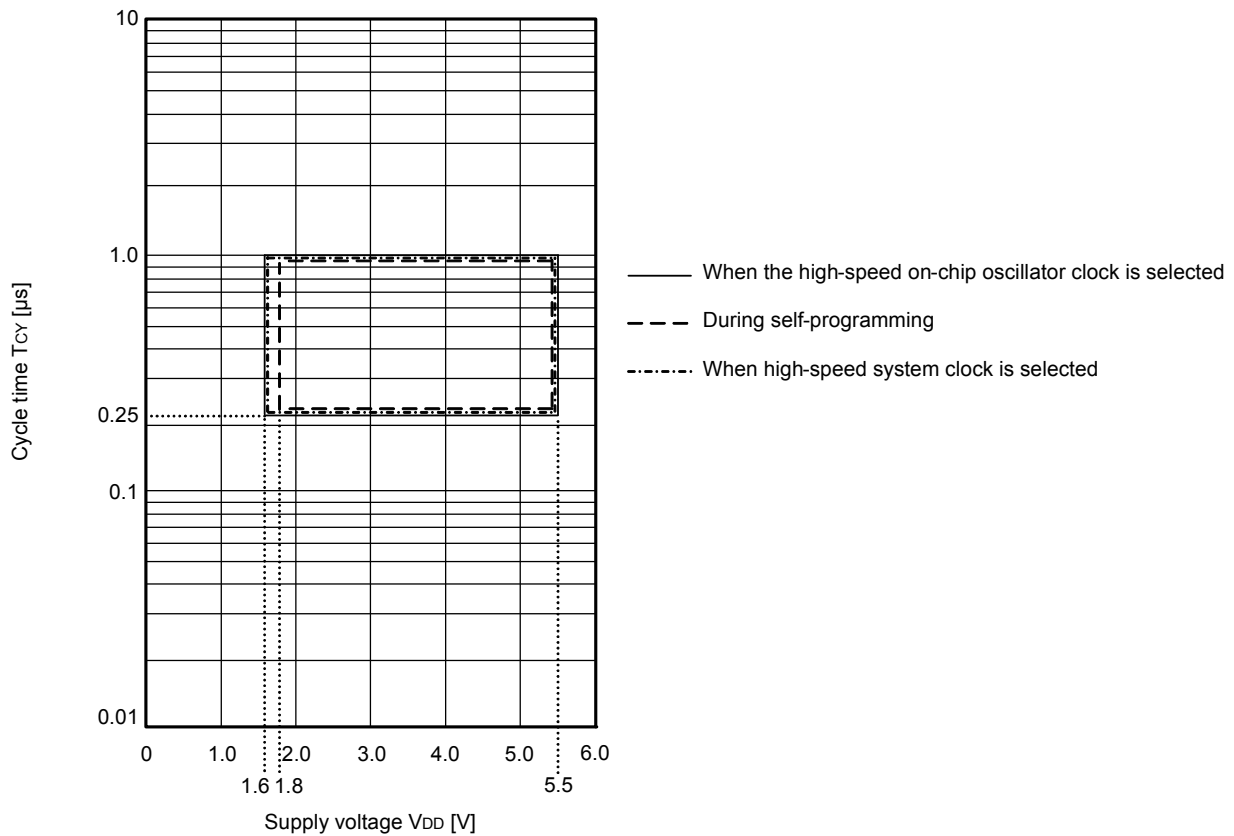
AC Timing Test Points
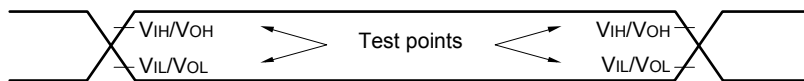
External System Clock Timing

TI/TO Timing

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)
(T$_A$ = -40 to +85°C, 1.6 V $\leq$ EV$_{DD0}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ $\geq$ 4/f$_{CLK}$	2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V	125		500		1000		ns
			2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V	250		500		1000		ns
			1.8 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V	500		500		1000		ns
			1.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V	1000		1000		1000		ns
			1.6 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V	—		1000		1000		ns
SCKp high-/low-level width	t$_{KH1}$, t$_{KL1}$	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		t$_{KCY1}$/2 - 12		t$_{KCY1}$/2 - 50		t$_{KCY1}$/2 - 50		ns
		2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		t$_{KCY1}$/2 - 18		t$_{KCY1}$/2 - 50		t$_{KCY1}$/2 - 50		ns
		2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		t$_{KCY1}$/2 - 38		t$_{KCY1}$/2 - 50		t$_{KCY1}$/2 - 50		ns
		1.8 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		t$_{KCY1}$/2 - 50		t$_{KCY1}$/2 - 50		t$_{KCY1}$/2 - 50		ns
		1.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		t$_{KCY1}$/2 - 100		t$_{KCY1}$/2 - 100		t$_{KCY1}$/2 - 100		ns
		1.6 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		—		t$_{KCY1}$/2 - 100		t$_{KCY1}$/2 - 100		ns
SIp setup time (to SCKp↑) Note 1	t$_{SIK1}$	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		44		110		110		ns
		2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		44		110		110		ns
		2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		75		110		110		ns
		1.8 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		110		110		110		ns
		1.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		220		220		220		ns
		1.6 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		—		220		220		ns
SIp hold time (from SCKp↑) Note 2	t$_{KSI1}$	1.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		19		19		19		ns
		1.6 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		—		19		19		ns
Delay time from SCKp↓ to SOp output Note 3	t$_{KSO1}$	1.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V C = 30 pF Note 4			25		25		25	ns
		1.6 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V C = 30 pF Note 4			—		25		25	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 , 5, 7)

Remark 2. f$_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T$_A$ = -40 to +85°C, 1.6 V ≤ EV$_{DD0}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode MIN.	HS MAX.	LS (low-speed main) mode MIN.	LS MAX.	LV (low-voltage main) mode MIN.	LV MAX.	Unit
SCKp cycle time Note 5	t$_{KCY2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V	20 MHz < f$_{MCK}$	8/f$_{MCK}$		—		—		ns
			f$_{MCK}$ ≤ 20 MHz	6/f$_{MCK}$		6/f$_{MCK}$		6/f$_{MCK}$		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V	16 MHz < f$_{MCK}$	8/f$_{MCK}$		—		—		ns
			f$_{MCK}$ ≤ 16 MHz	6/f$_{MCK}$		6/f$_{MCK}$		6/f$_{MCK}$		ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		6/f$_{MCK}$ and 500		6/f$_{MCK}$ and 500		6/f$_{MCK}$ and 500		ns
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		6/f$_{MCK}$ and 750		6/f$_{MCK}$ and 750		6/f$_{MCK}$ and 750		ns
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		6/f$_{MCK}$ and 1500		6/f$_{MCK}$ and 1500		6/f$_{MCK}$ and 1500		ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		6/f$_{MCK}$ and 1500		6/f$_{MCK}$ and 1500		ns
SCKp high-/ low-level width	t$_{KH2}$, t$_{KL2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY2}$/2 - 7		t$_{KCY2}$/2 - 7		t$_{KCY2}$/2 - 7		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY2}$/2 - 8		t$_{KCY2}$/2 - 8		t$_{KCY2}$/2 - 8		ns
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY2}$/2 - 18		t$_{KCY2}$/2 - 18		t$_{KCY2}$/2 - 18		ns
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY2}$/2 - 66		t$_{KCY2}$/2 - 66		t$_{KCY2}$/2 - 66		ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		t$_{KCY2}$/2 - 66		t$_{KCY2}$/2 - 66		ns
SIp setup time (to SCKp↑) Note 1	t$_{SIK2}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		1/f$_{MCK}$ + 20		1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		ns
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		ns
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		1/f$_{MCK}$ + 40		1/f$_{MCK}$ + 40		1/f$_{MCK}$ + 40		ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		1/f$_{MCK}$ + 40		1/f$_{MCK}$ + 40		ns
SIp hold time (from SCKp↑) Note 2	t$_{KSI2}$	1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		ns
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		1/f$_{MCK}$ + 250		1/f$_{MCK}$ + 250		1/f$_{MCK}$ + 250		ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		1/f$_{MCK}$ + 250		1/f$_{MCK}$ + 250		ns
Delay time from SCKp↓ to SOp output Note 3	t$_{KSO2}$	C = 30 pF Note 4	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		2/f$_{MCK}$ + 44		2/f$_{MCK}$ + 110		2/f$_{MCK}$ + 110	ns
			2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		2/f$_{MCK}$ + 75		2/f$_{MCK}$ + 110		2/f$_{MCK}$ + 110	ns
			1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		2/f$_{MCK}$ + 100		2/f$_{MCK}$ + 110		2/f$_{MCK}$ + 110	ns
			1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		2/f$_{MCK}$ + 220		2/f$_{MCK}$ + 220		2/f$_{MCK}$ + 220	ns
			1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		2/f$_{MCK}$ + 220		2/f$_{MCK}$ + 220	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution **Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(TA = -40 to +85°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V) **(2/2)**

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		transmission	$4.0 \text{ V} \leq \text{EV}_{DD0} \leq 5.5 \text{ V}$, $2.7 \text{ V} \leq V_b \leq 4.0 \text{ V}$		Note 1		Note 1		Note 1	bps
			Theoretical value of the maximum transfer rate $C_b = 50 \text{ pF}$, $R_b = 1.4 \text{ k}\Omega$, $V_b = 2.7 \text{ V}$		2.8 Note 2		2.8 Note 2		2.8 Note 2	Mbps
			$2.7 \text{ V} \leq \text{EV}_{DD0} < 4.0 \text{ V}$, $2.3 \text{ V} \leq V_b \leq 2.7 \text{ V}$		Note 3		Note 3		Note 3	bps
			Theoretical value of the maximum transfer rate $C_b = 50 \text{ pF}$, $R_b = 2.7 \text{ k}\Omega$, $V_b = 2.3 \text{ V}$		1.2 Note 4		1.2 Note 4		1.2 Note 4	Mbps
			$1.8 \text{ V} \leq \text{EV}_{DD0} < 3.3 \text{ V}$, $1.6 \text{ V} \leq V_b \leq 2.0 \text{ V}$		Notes 5, 6		Notes 5, 6		Notes 5, 6	bps
			Theoretical value of the maximum transfer rate $C_b = 50 \text{ pF}$, $R_b = 5.5 \text{ k}\Omega$, $V_b = 1.6 \text{ V}$		0.43 Note 7		0.43 Note 7		0.43 Note 7	Mbps

Note 1. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when $4.0 \text{ V} \leq \text{EV}_{DD0} \leq 5.5 \text{ V}$ and $2.7 \text{ V} \leq V_b \leq 4.0 \text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 2. This value as an example is calculated when the conditions described in the "Conditions" column are met.
Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Expression for calculating the transfer rate when $2.7 \text{ V} \leq \text{EV}_{DD0} < 4.0 \text{ V}$ and $2.3 \text{ V} \leq V_b \leq 2.7 \text{ V}$

Note 4. This value as an example is calculated when the conditions described in the "Conditions" column are met.
Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use it with $\text{EV}_{DD0} \geq V_b$.

Simplified I2C mode connection diagram (during communication at different potential)

Vb   Vb

Rb   Rb

SDAr   SDA

RL78 microcontroller   User's device

SCLr   SCL
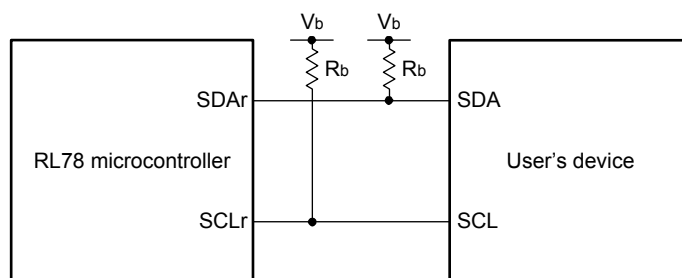
Simplified I2C mode serial transfer timing (during communication at different potential)

$1/f_{SCL}$

t_{LOW} t_{HIGH}

SCLr

SDAr

$t_{HD: DAT}$ $t_{SU: DAT}$
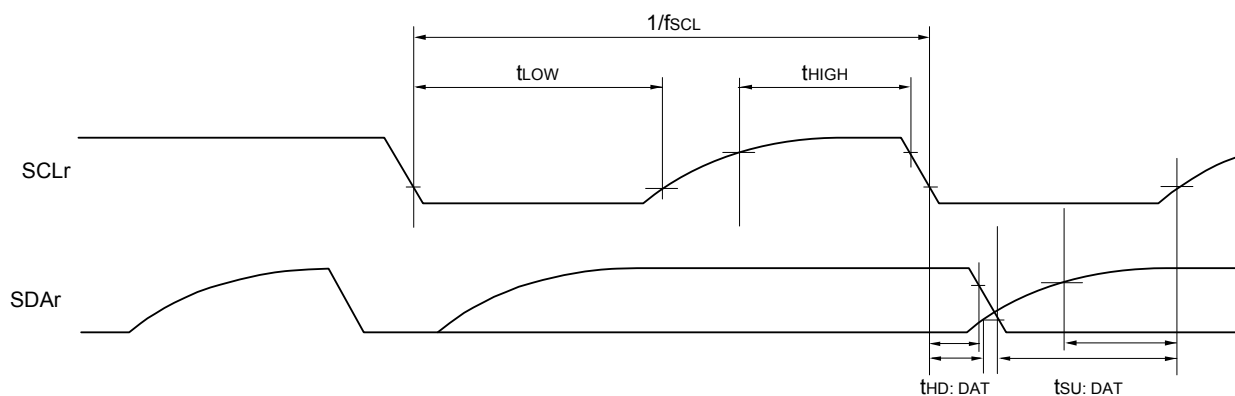
Remark 1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance,
$V_b[V]$: Communication line voltage
Remark 2. r: IIC number (r = 00, 01, 10, 11, 20), g: PIM, POM number (g = 0, 1, 3, 5, 7)
Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0, 2), mn = 00, 01, 02, 10)

3.3 DC Characteristics

3.3.1 Pin characteristics

(T_A = -40 to +105°C, 2.4 V $\leq$ EV_{DD0} $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = EV_{SS0} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147				-3.0 Note 2	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty $\leq$ 70% Note 3)	4.0 V $\leq$ EV_{DD0} $\leq$ 5.5 V			-30.0	mA
			2.7 V $\leq$ EV_{DD0} < 4.0 V			-10.0	mA
			2.4 V $\leq$ EV_{DD0} < 2.7 V			-5.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P53, P70 to P77, P146, P147 (When duty $\leq$ 70% Note 3)	4.0 V $\leq$ EV_{DD0} $\leq$ 5.5 V			-30.0	mA
			2.7 V $\leq$ EV_{DD0} < 4.0 V			-19.0	mA
			1.8 V $\leq$ EV_{DD0} < 2.7 V			-10.0	mA
		Total of all pins (When duty $\leq$ 70% Note 3)				-60.0	mA
	I_{OH2}	Per pin for P20 to P27				-0.1 Note 2	mA
		Total of all pins (When duty $\leq$ 70% Note 3)	2.4 V $\leq$ V_{DD} $\leq$ 5.5 V			-1.5	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0}, V_{DD} pins to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor $\leq$ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
  <Example>   Where n = 80% and I_{OH} = -10.0 mA
                Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) $\approx$ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Caution **P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43, P50 to P55, P71, P74 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T$_A$ = -40 to +105°C, 2.4 V $\leq$ EV$_{DD0}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = 0 V) **(2/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I$_{OL1}$	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77,P120, P130, P140, P141, P146, P147				8.5 Note 2	mA
		Per pin for P60 to P63				15.0 Note 2	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty $\leq$ 70% Note 3)	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			40.0	mA
			2.7 V $\leq$ EV$_{DD0}$ < 4.0 V			15.0	mA
			2.4 V $\leq$ EV$_{DD0}$ < 1.8 V			9.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P55, P60 to P63, P70 to P77, P146, P147 (When duty $\leq$ 70% Note 3)	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			40.0	mA
			2.7 V $\leq$ EV$_{DD0}$ < 4.0 V			35.0	mA
			2.4 V $\leq$ EV$_{DD0}$ < 1.8 V			20.0	mA
		Total of all pins (When duty $\leq$ 70% Note 3)				80.0	mA
	I$_{OL2}$	Per pin for P20 to P27				0.4 Note 2	mA
		Total of all pins (When duty $\leq$ 70% Note 3)	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			5.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV$_{SS0}$ and V$_{SS}$ pins.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor $\leq$ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

• Total output current of pins = (I$_{OL}$ × 0.7)/(n × 0.01)
  <Example>   Where n = 80% and I$_{OL}$ = 10.0 mA
                Total output current of pins = (10.0 × 0.7)/(80 × 0.01) $\approx$ 8.7 mA
  However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
  A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +105°C, 2.4 V $\leq$ EV$_{DD0}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = 0 V)   **(3/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH1}$	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147	Normal input buffer	0.8 EV$_{DD0}$		EV$_{DD0}$	V
	V$_{IH2}$	P01, P03, P04, P10, P14 to P17, P30, P43, P50, P53 to P55,	TTL input buffer 4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V	2.2		EV$_{DD0}$	V
			TTL input buffer 3.3 V $\leq$ EV$_{DD0}$ < 4.0 V	2.0		EV$_{DD0}$	V
			TTL input buffer 2.4 V $\leq$ EV$_{DD0}$ < 3.3 V	1.5		EV$_{DD0}$	V
	V$_{IH3}$	P20 to P27 (when P20 is used as a port pin)		0.7 V$_{DD}$		V$_{DD}$	V
	V$_{IH4}$	P60 to P63		0.7 EV$_{DD0}$		6.0	V
	V$_{IH5}$	P121 to P123, P137, EXCLK, EXCLKS, $\overline{RESET}$ (when P20 is used as INTP11 pin)		0.8 V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL1}$	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147	Normal input buffer	0		0.2 EV$_{DD0}$	V
	V$_{IL2}$	P01, P03, P04, P10, P14 to P17, P30, P43, P50, P53 to P55,	TTL input buffer 4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V $\leq$ EV$_{DD0}$ < 4.0 V	0		0.5	V
			TTL input buffer 2.4 V $\leq$ EV$_{DD0}$ < 3.3 V	0		0.32	V
	V$_{IL3}$	P20 to P27 (when P20 is used as a port pin)		0		0.3 V$_{DD}$	V
	V$_{IL4}$	P60 to P63		0		0.3 EV$_{DD0}$	V
	V$_{IL5}$	P121 to P124, P137, EXCLK, EXCLKS, $\overline{RESET}$ (when P20 is used as INTP11 pin)		0		0.2 V$_{DD}$	V

Caution   **The maximum value of V$_{IH}$ of pins P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43, P50 to P55, P71, P74 is EV$_{DD0}$, even in the N-ch open-drain mode.**

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)
(T$_A$ = -40 to +105°C, 2.4 V $\leq$ EV$_{DD0}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ $\geq$ 2/f$_{CLK}$	2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V	250		ns
			2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V	500		ns
SCKp high-/low-level width	t$_{KH1}$, t$_{KL1}$	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		t$_{KCY1}$/2 - 24		ns
		2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		t$_{KCY1}$/2 - 36		ns
		2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		t$_{KCY1}$/2 - 76		
SIp setup time (to SCKp↑) Note 1	t$_{SIK1}$	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		66		ns
		2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		66		ns
		2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		113		
SIp hold time (from SCKp↑) Note 2	t$_{KSI1}$	2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V		38		ns
Delay time from SCKp↓ to SOp output Note 3	t$_{KSO1}$	C = 20 pF Note 4			50	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM number (g = 0, 1, 3 , 5, 7)

Remark 2. f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(4) During communication at same potential (simplified I²C mode)

(T_A = -40 to +105°C, 2.4 V $\leq$ EV$_{DD0}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		400 Note 1	kHz
		2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		100 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Data setup time (reception)	$t_{SU: DAT}$	2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 220 Note 2		ns
		2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 580 Note 2		ns
Data hold time (transmission)	$t_{HD: DAT}$	2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	1420	ns

Note 1. The value must also be equal to or less than f_{MCK}/4.

Note 2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution   **Select the normal input buffer and the N-ch open drain output (V$_{DD}$ tolerance (for the 48-, 32-, 24-pin products)/EV$_{DD}$ tolerance (for the 64-, 36-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

(**Remarks** are listed on the next page.)

CSI mode connection diagram (during communication at different potential
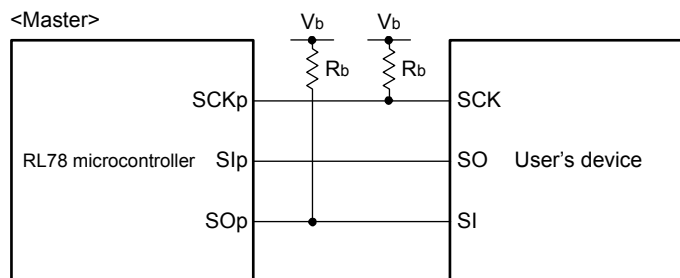
Remark 1. R$_b$[Ω]: Communication line (SCKp, SOp) pull-up resistance, C$_b$[F]: Communication line (SCKp, SOp) load capacitance, V$_b$[V]: Communication line voltage

Remark 2. p: CSI number (p = 00, 01, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 7)

Remark 3. f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

Remark 4. CSI01 of 48-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

3.10 Timing of Entry to Flash Memory Programming Modes

(T$_A$ = -40 to +105°C, 2.4 V $\leq$ EV$_{DD0}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t$_{SUINIT}$	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t$_{SU}$	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	t$_{HD}$	POR and LVD reset must end before the external reset ends.	1			ms
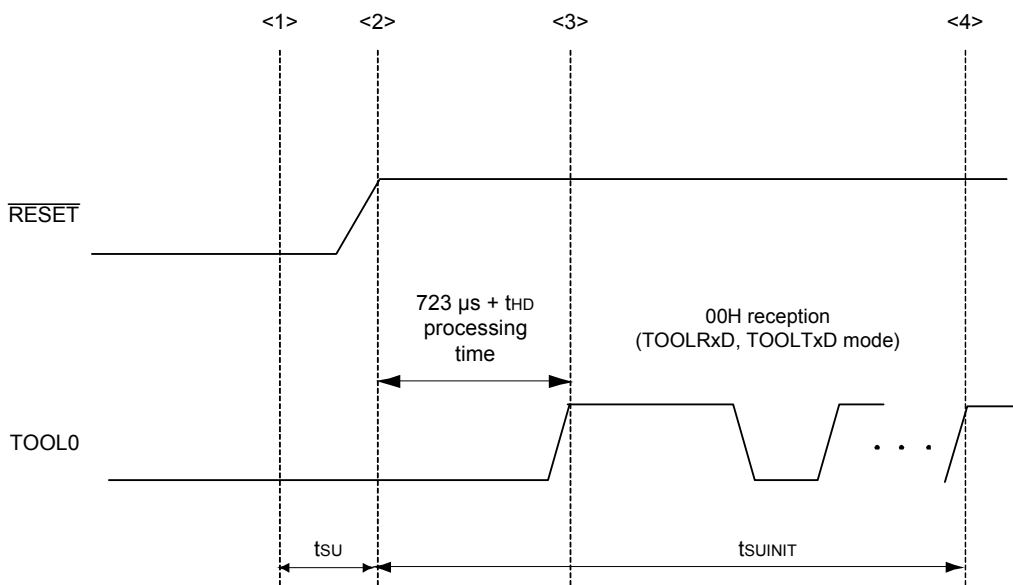
<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t$_{SUINIT}$: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

t$_{SU}$: How long from when the TOOL0 pin is placed at the low level until a pin reset ends

t$_{HD}$: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)