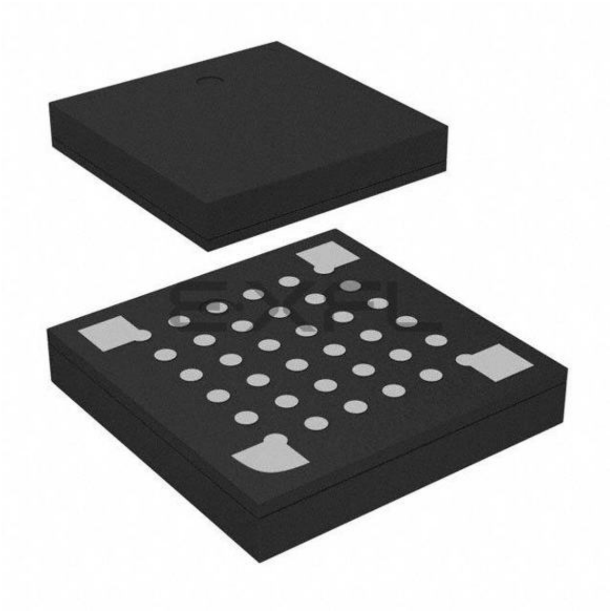

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, IrDA, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-WFLGA
Supplier Device Package	36-WFLGA (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f11bccala-u0

Pin count	Package	Fields of Application[Note]	Ordering Part Number
24 pins	24-pin plastic HWQFN (4 × 4, 0.5 mm pitch)	A	R5F11B7CANA#U0, R5F11B7EANA#U0, R5F11B7CANA#W0, R5F11B7EANA#W0
		G	R5F11B7CGNA#U0, R5F11B7EGNA#U0, R5F11B7CGNA#W0, R5F11B7EGNA#W0
32 pins	32-pin plastic LQFP (7 × 7, 0.8 mm pitch)	A	R5F11BBCAFP#30, R5F11BBEAFP#30, R5F11BBCAFP#50, R5F11BBEAFP#50
		G	R5F11BBCGFP#30, R5F11BBEGFP#30, R5F11BBCGFP#50, R5F11BBEGFP#50
36 pins	36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)	A	R5F11BCCALA#U0, R5F11BCEALA#U0, R5F11BCCALA#W0, R5F11BCEALA#W0
		G	R5F11BCCGLA#U0, R5F11BCEGLA#U0, R5F11BCCGLA#W0, R5F11BCEGLA#W0
48 pins	48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)	A	R5F11BGCAFB#30, R5F11BGEAFB#30, R5F11BGCAFB#50, R5F11BGEAFB#50
		G	R5F11BGCGFB#30, R5F11BGEGFB#30, R5F11BGCGFB#50, R5F11BGEGFB#50
64 pins	64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)	A	R5F11BLCAFB#30, R5F11BLEAFB#30, R5F11BLCAFB#50, R5F11BLEAFB#50
		G	R5F11BLCGFB#30, R5F11BLEGFB#30, R5F11BLCGFB#50, R5F11BLEGFB#50

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G1F**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 characteristics

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
		1.8 V ≤ V_{DD} < 2.4 V	1.0		8.0	
		1.6 V ≤ V_{DD} < 1.8 V	1.0		4.0	
XT1 clock oscillation frequency (f_{XT}) Note	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G1F User's Manual.

2.2.2 On-chip oscillator characteristics

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}	2.7 V ≤ V_{DD} ≤ 5.5 V		1		32	MHz
		2.4 V ≤ V_{DD} < 2.7 V		1		16	MHz
		1.8 V ≤ V_{DD} < 2.4 V		1		8	MHz
		1.6 V ≤ V_{DD} < 1.8 V		1		4	MHz
High-speed on-chip oscillator clock frequency accuracy		T_A = -20 to +85°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1		1	%
			1.6 V ≤ V_{DD} < 1.8 V	-5		5	%
		T_A = -40 to -20°C	1.8 V ≤ V_{DD} < 5.5 V	-1.5		1.5	%
			1.6 V ≤ V_{DD} < 1.8 V	-5.5		5.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

(T_A = -40 to +85°C, 1.6 V $\le EV_{DD0} \le V_{DD} \le$ 5.5 V, $V_{SS} = EV_{SS0}$ = 0 V) **(2/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low [Note 1]	I_{OL1}	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77,P120, P130, P140, P141, P146, P147				20.0 Note 2	mA
		Per pin for P60 to P63				15.0 Note 2	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty ≤ 70% [Note 3])	4.0 V $\le EV_{DD0} \le$ 5.5 V			70.0	mA
			2.7 V $\le EV_{DD0} <$ 4.0 V			15.0	mA
			1.8 V $\le EV_{DD0} <$ 2.7 V			9.0	mA
			1.6 V $\le EV_{DD0} <$ 1.8 V			4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P55, P60 to P63, P70 to P77, P146, P147 (When duty ≤ 70% [Note 3])	4.0 V $\le EV_{DD0} \le$ 5.5 V			80.0	mA
			2.7 V $\le EV_{DD0} <$ 4.0 V			35.0	mA
			1.8 V $\le EV_{DD0} <$ 2.7 V			20.0	mA
			1.6 V $\le EV_{DD0} <$ 1.8 V			10.0	mA
		Total of all pins (When duty ≤ 70% [Note 3])				150.0	mA
	I_{OL2}	Per pin for P20 to P27				0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% [Note 3])	1.6 V $\le V_{DD} \le$ 5.5 V			5.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0} and V_{SS} pins.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

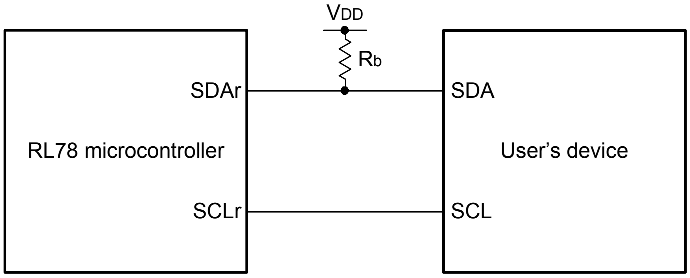
(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (4/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -10.0 mA	EV_{DD0} - 1.5			V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -3.0 mA	EV_{DD0} - 0.7			V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -2.0 mA	EV_{DD0} - 0.6			V
			1.8 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -1.5 mA	EV_{DD0} - 0.5			V
			1.6 V ≤ EV_{DD0} < 1.8 V, I_{OH1} = -1.0 mA	EV_{DD0} - 0.5			V
	V_{OH2}	P20 to P27	1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OH2} = -100 μA	V_{DD} - 0.5			V
Output voltage, low	V_{OL1}	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 20.0 mA			1.3	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			1.8 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
			1.6 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 0.3 mA			0.4	V
	V_{OL2}	P20 to P27	1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 15.0 mA			2.0	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 5.0 mA			0.4	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 3.0 mA			0.4	V
			1.8 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 2.0 mA			0.4	V
			1.6 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 1.0 mA			0.4	V

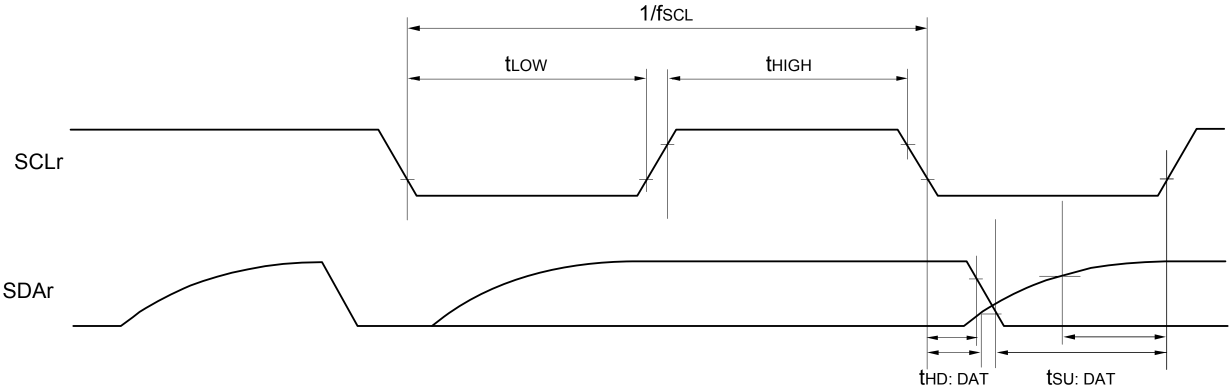
Caution **P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43, P50 to P55, P71, P74 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remark 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 01, 10, 11, 20, 21), g: PIM number (g = 0, 1, 3, 5, 7),
h: POM number (h = 0, 1, 3, 5, 7)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(T_A = -40 to +85°C, 1.8 V $\le EV_{DD0} \le V_{DD} \le$ 5.5 V, $V_{SS} = EV_{SS0}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		reception	4.0 V $\le EV_{DD0} \le$ 5.5 V, 2.7 V $\le V_b \le$ 4.0 V		$f_{MCK}/6$ Note 1		$f_{MCK}/6$ Note 1		$f_{MCK}/6$ Note 1	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 4		5.3		1.3		0.6	Mbps
			2.7 V $\le EV_{DD0} <$ 4.0 V, 2.3 V $\le V_b \le$ 2.7 V		$f_{MCK}/6$ Note 1		$f_{MCK}/6$ Note 1		$f_{MCK}/6$ Note 1	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 4		5.3		1.3		0.6	Mbps
			1.8 V $\le EV_{DD0} <$ 3.3 V, 1.6 V $\le V_b \le$ 2.0 V		$f_{MCK}/6$ Notes 1, 2, 3		$f_{MCK}/6$ Notes 1, 2		$f_{MCK}/6$ Notes 1, 2	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 4		5.3		1.3		0.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

Note 2. Use it with $EV_{DD0} \ge V_b$.

Note 3. The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$.
2.4 V $\le EV_{DD0} <$ 2.7 V: MAX. 2.6 Mbps
1.8 V $\le EV_{DD0} <$ 2.4 V: MAX. 1.3 Mbps

Note 4. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode:	32 MHz (2.7 V $\le V_{DD} \le$ 5.5 V) 16 MHz (2.4 V $\le V_{DD} \le$ 5.5 V)
LS (low-speed main) mode:	8 MHz (1.8 V $\le V_{DD} \le$ 5.5 V)
LV (low-voltage main) mode:	4 MHz (1.6 V $\le V_{DD} \le$ 5.5 V)

Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 48-, 32-, 24-pin products)/EV_{DD} tolerance (for the 64-, 36-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remark 1. V_b [V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1, 5, 7)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10, 11)

Remark 4. UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

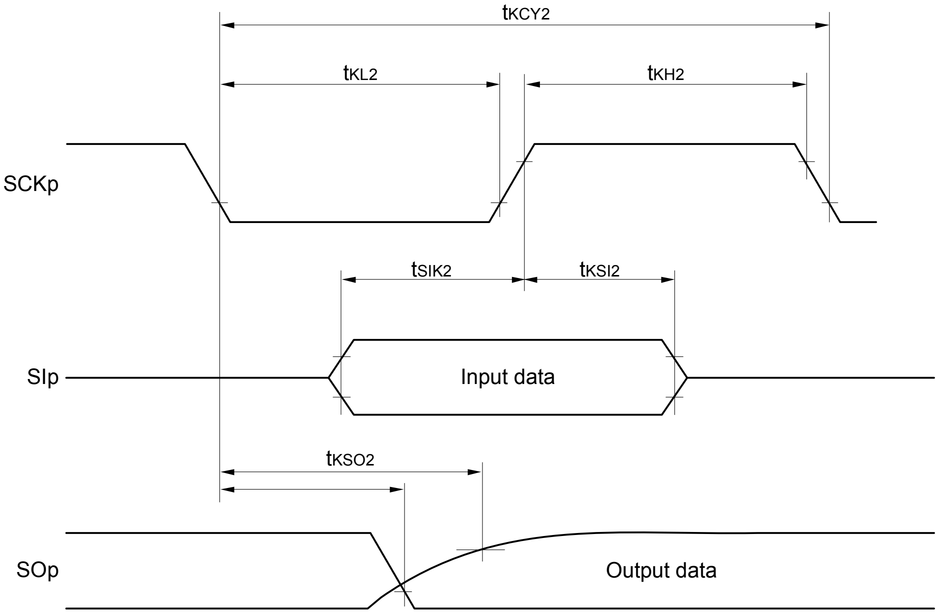
(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V)

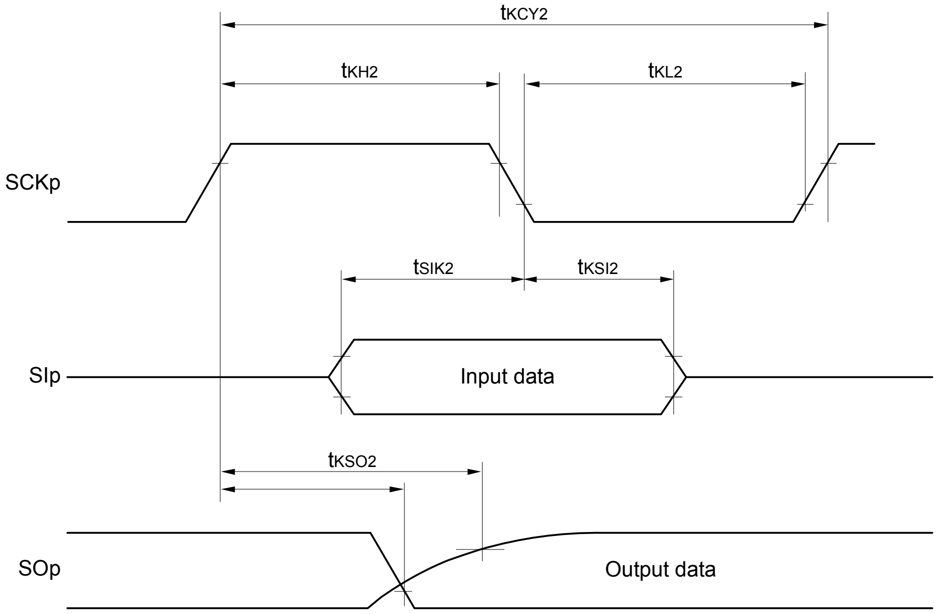
Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	24 MHz < f_{MCK}	$14/f_{MCK}$		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	$12/f_{MCK}$		—		—		ns
			8 MHz < f_{MCK} ≤ 20 MHz	$10/f_{MCK}$		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	$8/f_{MCK}$		$16/f_{MCK}$		—		ns
			f_{MCK} ≤ 4 MHz	$6/f_{MCK}$		$10/f_{MCK}$		$10/f_{MCK}$		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	24 MHz < f_{MCK}	$20/f_{MCK}$		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	$16/f_{MCK}$		—		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	$14/f_{MCK}$		—		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	$12/f_{MCK}$		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	$8/f_{MCK}$		$16/f_{MCK}$		—		ns
			f_{MCK} ≤ 4 MHz	$6/f_{MCK}$		$10/f_{MCK}$		$10/f_{MCK}$		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	24 MHz < f_{MCK}	$48/f_{MCK}$		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	$36/f_{MCK}$		—		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	$32/f_{MCK}$		—		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	$26/f_{MCK}$		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	$16/f_{MCK}$		$16/f_{MCK}$		—		ns
			f_{MCK} ≤ 4 MHz	$10/f_{MCK}$		$10/f_{MCK}$		$10/f_{MCK}$		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		$t_{KCY2}/2 - 12$		$t_{KCY2}/2 - 50$		$t_{KCY2}/2 - 50$		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		$t_{KCY2}/2 - 18$		$t_{KCY2}/2 - 50$		$t_{KCY2}/2 - 50$		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		$t_{KCY2}/2 - 50$		$t_{KCY2}/2 - 50$		$t_{KCY2}/2 - 50$		ns
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		$1/f_{MCK} + 20$		$1/f_{MCK} + 30$		$1/f_{MCK} + 30$		ns
		2.7 V ≤ EV_{DD0} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		$1/f_{MCK} + 20$		$1/f_{MCK} + 30$		$1/f_{MCK} + 30$		ns
		1.8 V ≤ EV_{DD0} ≤ 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		$1/f_{MCK} + 30$		$1/f_{MCK} + 30$		$1/f_{MCK} + 30$		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI2}			$1/f_{MCK} + 31$		$1/f_{MCK} + 31$		$1/f_{MCK} + 31$		ns
Delay time from SCKp↓ to SOp output Note 5	t_{KSO2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			$2/f_{MCK} + 120$		$2/f_{MCK} + 573$		$2/f_{MCK} + 573$	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			$2/f_{MCK} + 214$		$2/f_{MCK} + 573$		$2/f_{MCK} + 573$	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_v = 5.5 kΩ			$2/f_{MCK} + 573$		$2/f_{MCK} + 573$		$2/f_{MCK} + 573$	ns

(**Notes**, **Cautions**, and **Remarks** are listed on the next page.)

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



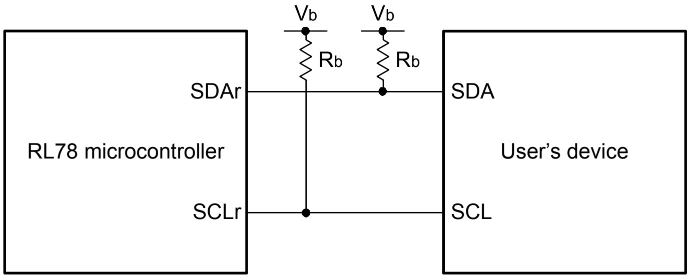
CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



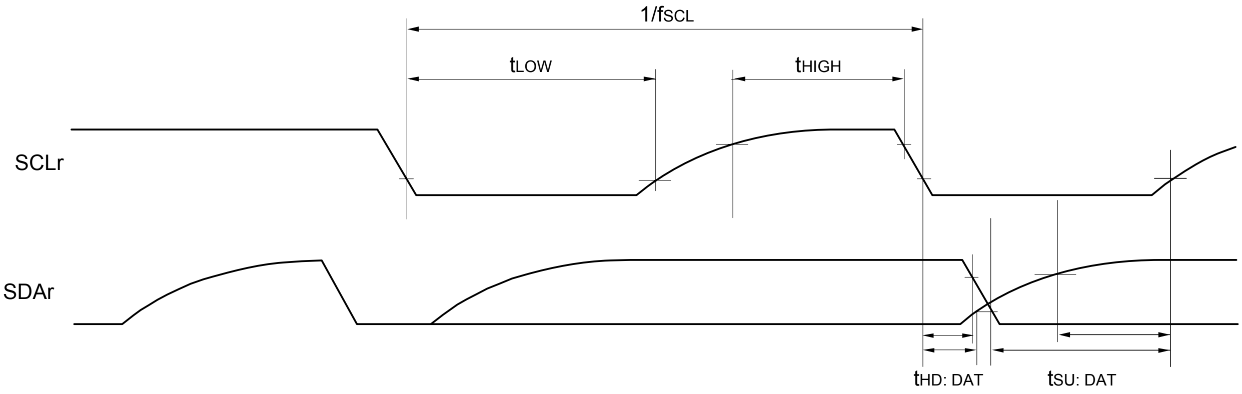
Remark 1. p: CSI number (p = 00, 01, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 7)

Remark 2. CSI01 of 48-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remark 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

Remark 2. r: IIC number (r = 00, 01, 10, 11, 20), g: PIM, POM number (g = 0, 1, 3, 5, 7)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0, 2), mn = 00, 01, 02, 10)

(1) I²C standard mode

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (2/2)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V	250		250		250		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V	250		250		250		ns
		1.7 V ≤ EV_{DD0} ≤ 5.5 V	250		250		250		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V	—		250		250		ns
Data hold time (transmission) Note 2	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
		1.7 V ≤ EV_{DD0} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
		1.6 V ≤ EV_{DD0} ≤ 5.5 V	—		0	3.45	0	3.45	μs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs
		1.7 V ≤ EV_{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs
		1.6 V ≤ EV_{DD0} ≤ 5.5 V	—		4.0		4.0		μs
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs
		1.7 V ≤ EV_{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs
		1.6 V ≤ EV_{DD0} ≤ 5.5 V	—		4.7		4.7		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I^2C fast mode

(T_A = -40 to +85°C, 1.6 V $\le EV_{DD0} \le V_{DD} \le$ 5.5 V, $V_{SS} = EV_{SS0}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: $f_{CLK} \ge$ 3.5 MHz	2.7 V $\le EV_{DD0} \le$ 5.5 V	0	400	0	400	0	400	kHz
			1.8 V $\le EV_{DD0} \le$ 5.5 V	0	400	0	400	0	400	kHz
Setup time of restart condition	$t_{SU:\ STA}$	2.7 V $\le EV_{DD0} \le$ 5.5 V		0.6		0.6		0.6		μs
		1.8 V $\le EV_{DD0} \le$ 5.5 V		0.6		0.6		0.6		μs
Hold time Note 1	$t_{HD:\ STA}$	2.7 V $\le EV_{DD0} \le$ 5.5 V		0.6		0.6		0.6		μs
		1.8 V $\le EV_{DD0} \le$ 5.5 V		0.6		0.6		0.6		μs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V $\le EV_{DD0} \le$ 5.5 V		1.3		1.3		1.3		μs
		1.8 V $\le EV_{DD0} \le$ 5.5 V		1.3		1.3		1.3		μs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V $\le EV_{DD0} \le$ 5.5 V		0.6		0.6		0.6		μs
		1.8 V $\le EV_{DD0} \le$ 5.5 V		0.6		0.6		0.6		μs
Data setup time (reception)	$t_{SU:\ DAT}$	2.7 V $\le EV_{DD0} \le$ 5.5 V		100		100		100		ns
		1.8 V $\le EV_{DD0} \le$ 5.5 V		100		100		100		ns
Data hold time (transmission) Note 2	$t_{HD:\ DAT}$	2.7 V $\le EV_{DD0} \le$ 5.5 V		0	0.9	0	0.9	0	0.9	μs
		1.8 V $\le EV_{DD0} \le$ 5.5 V		0	0.9	0	0.9	0	0.9	μs
Setup time of stop condition	$t_{SU:\ STO}$	2.7 V $\le EV_{DD0} \le$ 5.5 V		0.6		0.6		0.6		μs
		1.8 V $\le EV_{DD0} \le$ 5.5 V		0.6		0.6		0.6		μs
Bus-free time	t_{BUF}	2.7 V $\le EV_{DD0} \le$ 5.5 V		1.3		1.3		1.3		μs
		1.8 V $\le EV_{DD0} \le$ 5.5 V		1.3		1.3		1.3		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD:\ DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

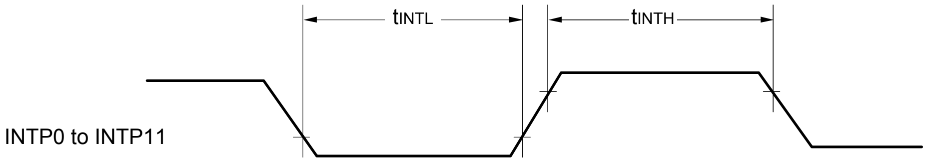
2.6.7 LVD circuit characteristics

(1) Reset Mode and Interrupt Mode

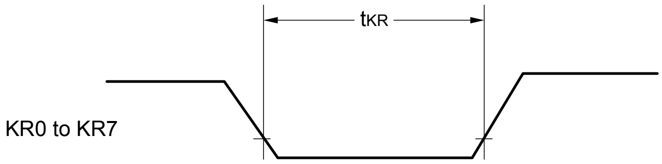
(T_A = -40 to +85°C, $V_{PDR} \leq EV_{DD0} \leq V_{DD} \leq$ 5.5 V, $V_{SS} = EV_{SS0}$ = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	Supply voltage level	V_{LVD0}	Rising edge	3.98	4.06	4.14	V
			Falling edge	3.90	3.98	4.06	V
		V_{LVD1}	Rising edge	3.68	3.75	3.82	V
			Falling edge	3.60	3.67	3.74	V
		V_{LVD2}	Rising edge	3.07	3.13	3.19	V
			Falling edge	3.00	3.06	3.12	V
		V_{LVD3}	Rising edge	2.96	3.02	3.08	V
			Falling edge	2.90	2.96	3.02	V
		V_{LVD4}	Rising edge	2.86	2.92	2.97	V
			Falling edge	2.80	2.86	2.91	V
		V_{LVD5}	Rising edge	2.76	2.81	2.87	V
			Falling edge	2.70	2.75	2.81	V
		V_{LVD6}	Rising edge	2.66	2.71	2.76	V
			Falling edge	2.60	2.65	2.70	V
		V_{LVD7}	Rising edge	2.56	2.61	2.66	V
			Falling edge	2.50	2.55	2.60	V
		V_{LVD8}	Rising edge	2.45	2.50	2.55	V
			Falling edge	2.40	2.45	2.50	V
		V_{LVD9}	Rising edge	2.05	2.09	2.13	V
			Falling edge	2.00	2.04	2.08	V
		V_{LVD10}	Rising edge	1.94	1.98	2.02	V
			Falling edge	1.90	1.94	1.98	V
		V_{LVD11}	Rising edge	1.84	1.88	1.91	V
			Falling edge	1.80	1.84	1.87	V
		V_{LVD12}	Rising edge	1.74	1.77	1.81	V
			Falling edge	1.70	1.73	1.77	V
		V_{LVD13}	Rising edge	1.64	1.67	1.70	V
			Falling edge	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

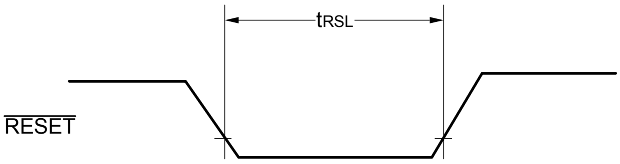
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



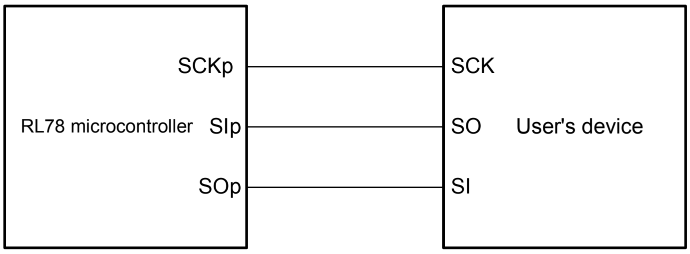
(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V)(2/2)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
$\overline{SSI00}$ setup time	t_{SSIK}	DAPmn = 0	2.7 V ≤ EV_{DD0} ≤ 5.5 V	240		ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V	400		ns
		DAPmn = 1	2.7 V ≤ EV_{DD0} ≤ 5.5 V	1/f_{MCK} + 240		ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V	1/f_{MCK} + 400		ns
$\overline{SSI00}$ hold time	t_{KSSI}	DAPmn = 0	2.7 V ≤ EV_{DD0} ≤ 5.5 V	1/f_{MCK} + 240		ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V	1/f_{MCK} + 400		ns
		DAPmn = 1	2.7 V ≤ EV_{DD0} ≤ 5.5 V	240		ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V	400		ns

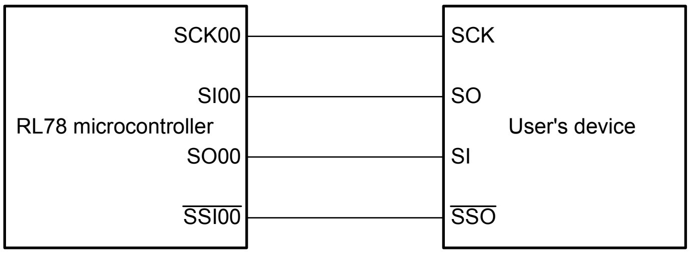
Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

CSI mode connection diagram (during communication at same potential)



CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))



Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21)
Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (1/2)

Parameter	Symbol	Conditions			HS (high-speed main) mode		Unit
					MIN.	MAX.	
Transfer rate		reception	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			$f_{MCK}/12$ Note 1	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3		2.6	Mbps
			2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			$f_{MCK}/12$ Note 1	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3		2.6	Mbps
			2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			$f_{MCK}/12$ Notes 1, 2	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3		1.3	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

Note 2. The following conditions are required for low voltage interface when EV_{DD0} < V_{DD}.
2.4 V ≤ EV_{DD0} < 2.7 V: MAX. 2.6 Mbps
1.8 V ≤ EV_{DD0} < 2.4 V: MAX. 1.3 Mbps

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 48-, 32-, 24-pin products)/EV_{DD} tolerance (for the 64-, 36-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remark 1. V_b [V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1, 5, 7)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

Remark 4. UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	24 MHz < f_{MCK}	28/f_{MCK}		ns
			20 MHz < f_{MCK} ≤ 24 MHz	24/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 20 MHz	20/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	24 MHz < f_{MCK}	40/f_{MCK}		ns
			20 MHz < f_{MCK} ≤ 24 MHz	32/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	28/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	24/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	24 MHz < f_{MCK}	96/f_{MCK}		ns
			20 MHz < f_{MCK} ≤ 24 MHz	72/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	64/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	52/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	32/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	20/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 - 24		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 - 36		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		t_{KCY2}/2 - 100		ns
SIp setup time (to SCKp↑) Note 2	t_{SIK2}	2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 40		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		1/f_{MCK} + 60		ns
SIp hold time (from SCKp↑) Note 3	t_{KSI2}			1/f_{MCK} + 62		ns
Delay time from SCKp↓ to SOp output Note 4	t_{KSO2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			2/f_{MCK} + 240	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 428	ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_v = 5.5 kΩ			2/f_{MCK} + 1146	ns

(**Notes** and **Remarks** are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) **(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 340 Note 2		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 340 Note 2		ns
		4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	$1/f_{MCK}$ + 760 Note 2		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 760 Note 2		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	$1/f_{MCK}$ + 570 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	1420	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	1420	ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	0	1215	ns

Note 1. The value must also be equal to or less than $f_{MCK}/4$.

Note 2. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Caution **Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 48-, 32-, 24-pin products)/EV_{DD} tolerance (for the 64-, 36-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 48-, 32-, 24-pin products)/EV_{DD} tolerance (for the 64-, 36-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

(2) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI16 to ANI24

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V,
V_{SS} = EV_{SS0} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error [Note 1]	AINL	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} [Notes 3, 4]	2.4 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±5.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target ANI pin: ANI16 to ANI20	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	µs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
Zero-scale error [Notes 1, 2]	E_{ZS}	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} [Notes 3, 4]	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
Full-scale error [Notes 1, 2]	E_{FS}	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} [Notes 3, 4]	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
Integral linearity error [Note 1]	ILE	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} [Notes 3, 4]	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±3.5	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} [Notes 3, 4]	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI24		0		AV_{REFP} and EV_{DD0}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When EV_{DD0} ≤ AV_{REFP} ≤ V_{DD}, the MAX. values are as follows.

Overall error:	Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.
Zero-scale error/Full-scale error:	Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.
Integral linearity error/ Differential linearity error:	Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Note 4. When AV_{REFP} < EV_{DD0} ≤ V_{DD}, the MAX. values are as follows.

Overall error:	Add ±4.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.
Zero-scale error/Full-scale error:	Add ±0.20%FSR to the MAX. value when AV_{REFP} = V_{DD}.
Integral linearity error/ Differential linearity error:	Add ±2.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

3.6.4 Comparator

(T_A = -40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOCMP}				±5	±40	mV
Input voltage range	V_{ICMP}			0		V_{DD}	V
Internal reference voltage deviation	ΔV_{IREF}	CmRVM register value : 7FH to 80H (m = 0, 1)				±2	LSB
		Other than above				±1	LSB
Response Time	t_{CR}, t_{CF}	Input amplitude±100mV			70	150	ns
Operation stabilization time[Note 1]	t_{CMP}	CMPn = 0→1	V_{DD} = 3.3 to 5.5 V			1	μs
			V_{DD} = 2.7 to 3.3 V			3	μs
Reference voltage stabilization wait time	t_{VR}	CVRE : 0→1[Note 2]				20	μs
Operation current	I_{CMPDD}	Separately, it is defined as the operation current of peripheral functions.					

Note 1. Time taken until the comparator satisfies the DC/AC characteristics after the comparator operation enable signal is switched (CMPnEN = 0 → 1).

Note 2. Enable comparator output (CnOE bit = 1; n = 0 to 1) after enabling operation of the internal reference voltage generator (by setting the CVREm bit to 1; m = 0 to 1) and waiting for the operation stabilization time to elapse.

3.6.5 PGA

(T_A = -40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOPGA}					±10	mV
Input voltage range	V_{IPGA}			0		0.9 × V_{DD}/ Gain	V
Output voltage range	V_{IOHPGA}			0.93 × V_{DD}			V
	V_{IOLPGA}					0.07 × V_{DD}	V
Gain error		x4, x8				±1	%
		x16				±1.5	%
		x32				±2	%
Slew rate	SR_{RPGA}	Rising When Vin= 0.1V_{DD}/gain to 0.9V_{DD}/gain. 10 to 90% of output voltage amplitude	4.0 V ≤ V_{DD} ≤ 5.5 V (Other than x32)	3.5			V/μs
			4.0 V ≤ V_{DD} ≤ 5.5 V (x32)	3.0			
			2.7 V ≤ V_{DD} ≤ 4.0V	0.5			
	SR_{FPGA}	Falling When Vin= 0.1V_{DD}/gain to 0.9V_{DD}/gain. 90 to 10% of output voltage amplitude	4.0 V ≤ V_{DD} ≤ 5.5 V (Other than x32)	3.5			
			4.0 V ≤ V_{DD} ≤ 5.5 V (x32)	3.0			
			2.7 V ≤ V_{DD} ≤ 4.0V	0.5			
Reference voltage stabilization wait time[Note 1]	t_{PGA}	x4, x8				5	μs
		x16, x32				10	μs
Operation current	I_{PGADD}	Separately, it is defined as the operation current of peripheral functions.					

Note 1. Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled (PGAEN = 1).

(2) Interrupt & Reset Mode

(T_A = -40 to +105°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Voltage detection threshold	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage			2.64	2.75	2.86	V
	V_{LVDD1}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
				Falling interrupt voltage	2.75	2.86	2.97	V
	V_{LVDD2}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
				Falling interrupt voltage	2.85	2.96	3.07	V
	V_{LVDD3}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
				Falling interrupt voltage	3.83	3.98	4.13	V

3.6.8 Power supply voltage rising slope characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SV_{DD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 3.4 AC Characteristics.

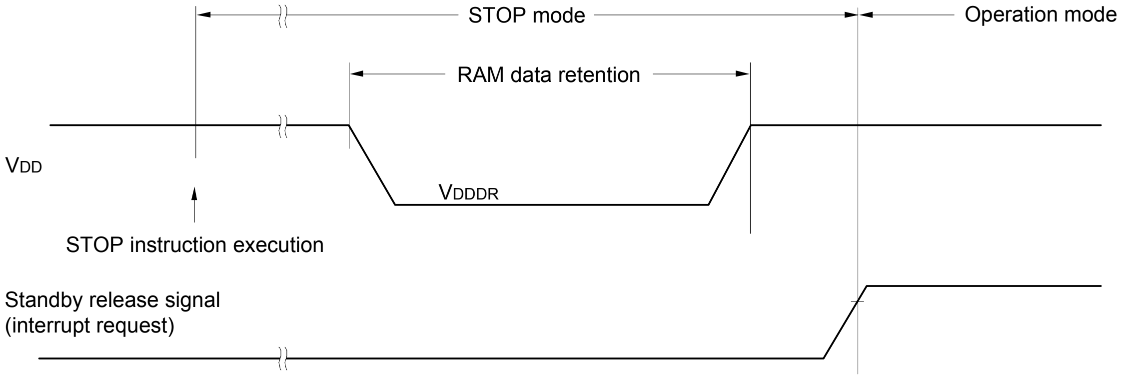
3.7 RAM Data Retention Characteristics

(T_A = -40 to +105°C, V_{SS} = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Notes 1, 2		5.5	V

Note 1. The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.

Note 2. Enter STOP mode before the supply voltage falls below the recommended operating voltage.



3.8 Flash Memory Programming Characteristics

(T_A = -40 to +105°C, 2.4 V $\leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	2.4 V $\leq V_{DD} \leq$ 5.5 V	1		32	MHz