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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	36MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.55V ~ 1.8V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam7l128-au

6. I/O Line Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are schmitt trigger inputs. TMS, TDI and TCK do not integrate a pull-up resistor.

TDO is an output, driven at up to VDDIO, and has no pull-up resistor.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. The JTAGSEL pin integrates a permanent pull-down resistor of about 15 k to GND, so that it can be left unconnected for normal operations.

6.2 Test Pin

The TST pin is used for manufacturing test or fast programming mode of the AT91SAM7L128/64 when asserted high. The TST pin integrates a permanent pull-down resistor of about 15 k to GND, so that it can be left unconnected for normal operations.

To enter fast programming mode, the TST and CLKIN pins must be tied high while FWUP is tied low.

6.3 NRST Pin

The NRST pin is bidirectional. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. There is no constraint on the length of the reset pulse and the reset controller can guarantee a minimum pulse length.

The NRST pin integrates a permanent pull-up resistor to VDDIO1 of about 100 k.

6.4 NRSTB Pin

The NRSTB pin is input only and enables asynchronous reset of the AT91SAM7L128/64 when asserted low. The NRSTB pin integrates a permanent pull-up resistor of about 15 k . This allows connection of a simple push button on the NRBST pin as a system-user reset.

In all modes, this pin will reset the chip. It can be used as an external system reset source.

In harsh environments, it is recommended to add an external capacitor (10 nF) between NRSTB and VDDIO1.

NRSTB pin must not be connected to VDDIO1. There must not be an external pull-up on NRSTB.

6.5 ERASE Pin

The ERASE pin is used to reinitialize the Flash content and some of its NVM bits. It integrates a permanent pull-down resistor of about 15 k to GND, so that it can be left unconnected for normal operations.

This pin is debounced by SCLK to improve the glitch tolerance. When the ERASE pin is tied high during less than 100 ms, it is not taken into account. The pin must be tied high during more than 220 ms to perform the reinitialization of the Flash.

6.6 PIO Controller Lines

All the I/O lines; PA0 to PA25, PB0 to PB23, PC0 to PC29 integrate a programmable pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the PIO controllers. All I/Os have input schmitt triggers.

Typical pull-up value is 100 k .

Maximum frequency is:

36 MHz under 25 pF of load on PIOC

36 MHz under 25 pF of load on PIOA and PIOB

10.4 PIO Controller A Multiplexing

Table 10-2. Multiplexing on PIO Controller A

PIO Controller A				Application Usage	
I/O Line	Peripheral A	Peripheral B	Extra Function	Function	Comments
PA0			COM0		
PA1			COM1		
PA2			COM2		
PA3			COM3		
PA4			COM4		
PA5			COM5		
PA6			SEG0		
PA7			SEG1		
PA8			SEG2		
PA9			SEG3		
PA10			SEG4		
PA11			SEG5		
PA12			SEG6		
PA13			SEG7		
PA14			SEG8		
PA15			SEG9		
PA16			SEG10		
PA17			SEG11		
PA18			SEG12		
PA19			SEG13		
PA20			SEG14		
PA21			SEG15		
PA22			SEG16		
PA23			SEG17		
PA24			SEG18		
PA25			SEG19		

13.4.1 Reset Controller Control Register

Name: RSTC_CR

Access Type: Write-only

31	30	29	28	27	26	25	24
KEY							
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
				EXTRST	PERRST		PROCRST

PROCRST: Processor Reset

0 = No effect.

1 = If KEY is correct, resets the processor.

PERRST: Peripheral Reset

0 = No effect.

1 = If KEY is correct, resets the peripherals.

EXTRST: External Reset

0 = No effect.

1 = If KEY is correct, asserts the NRST pin.

KEY: Password

Should be written at value 0xA5. Writing any other value in this field aborts the write operation.

the source of the access leading to the last abort (bits MST_EMAC, MST_PDC and MST_ARM)

whether or not an abort occurred for each master since the last read of the register (bits SVMST_EMAC, SVMST_PDC and SVMST_ARM) unless this information is loaded in MST bits

In the case of a Data Abort from the processor, the address of the data access is stored. This is useful, as searching for which address generated the abort would require disassembling the instructions and full knowledge of the processor context.

In the case of a Prefetch Abort, the address may have changed, as the prefetch abort is pipelined in the ARM processor. The ARM processor takes the prefetch abort into account only if the read instruction is executed and it is

Figure 25-2. Fast Startup Circuitry

Each wake-up input pin can be enabled to generate a Fast Startup event by writing at 1 the corresponding bit in the Fast Startup Mode Register SUPC_FSMR. Only a low level on the enabled wake-up input pins generates a Fast Startup.

The user interface does not provide any status for Fast Startup, but the user can easily recover this information by reading the PIO Controller.

25.7 Programming Sequence

1. Checking the Main Oscillator Frequency (Optional):

26.5.11 Debug Unit Chip ID Extension Register

Name: DBGU_EXID

Access Type: Read-only

31	30	29	28	27	26	25	24
EXID							
23	22	21	20	19	18	17	16
EXID							
15	14	13	12	11	10	9	8
EXID							
7	6	5	4	3	2	1	0
EXID							

EXID: Chip ID Extension

Reads 0 if the bit EXT in DBGU_CIDR is 0.

26.5.12 Debug Unit Force NTRST Register

Name: DBGU_FNR

Access Type: Read-write

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
							FNTRST

FNTRST: Force NTRST

0 = NTRST of the ARM processor s TAP controller is driven by the power_on_reset signal.

1 = NTRST of the ARM processor s TAP controller is held low.

27.6.17 PIO Controller Interrupt Status Register

Name: PIO_ISR

Access Type: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

P0-P31: Input Change Interrupt Status

0 = No Input Change has been detected on the I/O line since PIO_ISR was last read or since reset.

1 = At least one Input Change has been detected on the I/O line since PIO_ISR was last read or since reset.

27.6.18 PIO Multi-driver Enable Register

Name: PIO_MDER

Access Type: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

P0-P31: Multi Drive Enable.

0 = No effect.

1 = Enables Multi Drive on the I/O line.

1 = It indicates that the TWI_THR is empty and that data has been transmitted and acknowledged.

If TXRDY is high and if a NACK has been detected, the transmission will be stopped. Thus when TRDY = NACK = 1, the programmer must not fill TWI_THR to avoid losing it.

TXRDY behavior in Slave mode can be seen in Figure 29-24 on page 331, Figure 29-27 on page 333, Figure 29-29 on page 335 and Figure 29-30 on page 335.

SVREAD: Slave Read (automatically set / reset)

This bit is only used in Slave mode. When SVACC is low (no Slave access has been detected) SVREAD is irrelevant.

0 = Indicates that a write access is performed by a Master.

1 = Indicates that a read access is performed by a Master.

SVREAD behavior can be seen in Figure 29-24 on page 331, Figure 29-25 on page 331, Figure 29-29 on page 335 and Figure 29-30 on page 335.

SVACC: Slave Access (automatically set / reset)

This bit is only used in Slave mode.

0 = TWI is not addressed. SVACC is automatically cleared after a NACK or a STOP condition is detected.

1 = Indicates that the address decoding sequence has matched (A Master has sent SADR). SVACC remains high until a NACK or a STOP condition is detected.

SVACC behavior can be seen in Figure 29-24 on page 331, Figure 29-25 on page 331, Figure 29-29 on page 335 and Figure 29-30 on page 335.

GACC: General Call Access (clear on read)

This bit is only used in Slave mode.

0 = No General Call has been detected.

1 = A General Call has been detected. After the detection of General Call, the programmer decoded the commands that follow and the programming sequence.

GACC behavior can be seen in Figure 29-26 on page 332.

OVRE: Overrun Error (clear on read)

This bit is only used in Master mode.

0 = TWI_RHR has not been loaded while RXRDY was set

1 = TWI_RHR has been loaded while RXRDY was set. Reset by read in TWI_SR when TXCOMP is set.

NACK: Not Acknowledged (clear on read)

NACK used in Master mode:

0 = Each data byte has been correctly received by the far-end side TWI slave component.

1 = A data byte has not been acknowledged by the slave component. Set at the same time as TXCOMP.

NACK used in Slave Read mode:

0 = Each data byte has been correctly received by the Master.

1 = In read mode, a data byte has not been acknowledged by the Master. When NACK is set the programmer must not fill TWI_THR even if TXRDY is set, because it means that the Master will stop the data transfer or re initiate it.

Note that in Slave Write mode all data are acknowledged by the TWI.

32.3 I/O Lines Description

Each channel outputs one waveform on one external I/O line.

Table 32-1. I/O Line Description

Name	Description	Type
PWMx	PWM Waveform Output for channel x	Output

32.4 Product Dependencies

32.4.1 I/O Lines

The pins used for interfacing the PWM may be multiplexed with PIO lines. The programmer must first program the PIO controller to assign the desired PWM pins to their peripheral function. If I/O lines of the PWM are not used by the application, they can be used for other purposes by the PIO controller.

All of the PWM outputs may or may not be enabled. If an application requires only four channels, then only four PIO lines will be assigned to PWM outputs.

32.4.2 Power Management

The PWM is not continuously clocked. The programmer must first enable the PWM clock in the Power Management Controller (PMC) before using the PWM. However, if the application does not require PWM operations, the PWM clock can be stopped when not needed and be restarted later. In this case, the PWM will resume its operations where it left off.

Configuring the PWM does not require the PWM clock to be enabled.

32.4.3 Interrupt Sources

The PWM interrupt line is connected on one of the internal sources of the Advanced Interrupt Controller. Using the PWM interrupt requires the AIC to be programmed first. Note that it is not recommended to use the PWM interrupt line in edge sensitive mode.

32.5 Functional Description

The PWM macrocell is primarily composed of a clock generator module and channels.

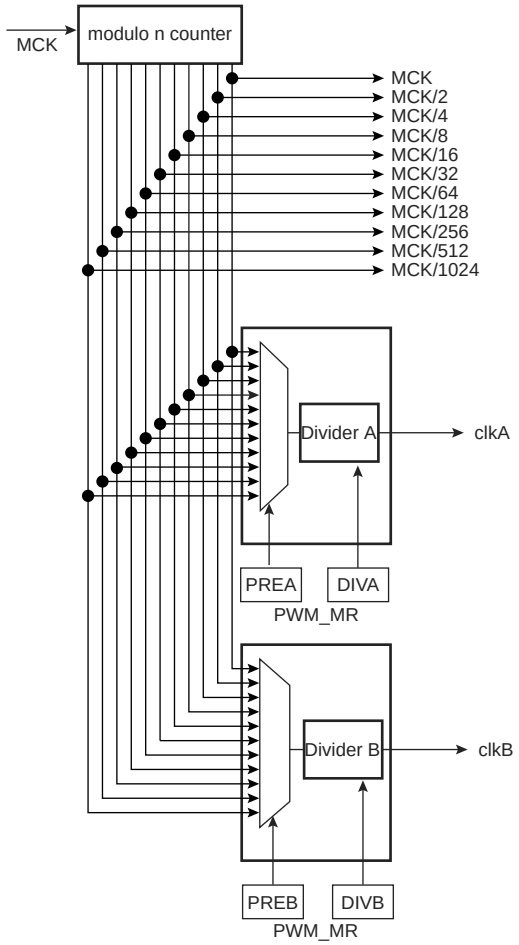
Clocked by the system clock, MCK, the clock generator module provides 13 clocks.

Each channel can independently choose one of the clock generator outputs.

Each channel generates an output waveform with attributes that can be defined independently for each channel through the user interface registers.

32.5.1 PWM Clock Generator

Figure 32-2. Functional View of the Clock Generator Block Diagram



Caution: Before using the PWM macrocell, the programmer must first enable the PWM clock in the Power Management Controller (PMC).

The PWM macrocell master clock, MCK, is divided in the clock generator module to provide different clocks available for all channels. Each channel can independently select one of the divided clocks.

The clock generator is divided in three blocks:

- a modulo n counter which provides 11 clocks: F_{MCK}, $F_{MCK}/2$, $F_{MCK}/4$, $F_{MCK}/8$, $F_{MCK}/16$, $F_{MCK}/32$, $F_{MCK}/64$, $F_{MCK}/128$, $F_{MCK}/256$, $F_{MCK}/512$, $F_{MCK}/1024$
- two linear dividers (1, 1/2, 1/3, ... 1/255) that provide two separate clocks: clkA and clkB

Each linear divider can independently divide one of the clocks of the modulo n counter. The selection of the clock to be divided is made according to the PREA (PREB) field of the PWM Mode register (PWM_MR). The resulting clock clkA (clkB) is the clock selected divided by DIVA (DIVB) field value in the PWM Mode register (PWM_MR).

After a reset of the PWM controller, DIVA (DIVB) and PREA (PREB) in the PWM Mode register are set to 0. This implies that after reset clkA (clkB) are turned off.

At reset, all clocks provided by the modulo n counter are turned off except clock clk . This situation is also true when the PWM master clock is turned off through the Power Management Controller.

35.3.2.2 High Frequency

Table 35-10. High-range Frequencies, Active Mode (Peripheral Activated)

Mode	Conditions	VDDIO1 Consumption	Condition	Unit
Active (AT91SAM7L128/64) (See Figure 35-8)	Voltage regulator in Normal Mode VDDOUT = 1.80V RTC ON Programmable BOD ON (Continuous) Charge pump ON LCD Regulator ON Flash is read ADC ON All peripheral clocks activated RC 2MHz OFF PLL ON		VDDI01= 3V @ 25°C	mA
		3.346	ARM core clock = 4 MHz	
		5.37	ARM core clock = 8 MHz	
		10.37	ARM core clock = 16 MHz	
		11.16	ARM core clock = 18 MHz	
		12.13	ARM core clock = 20 MHz	
		14.24	ARM core clock = 24 MHz	
		19.55	ARM core clock = 30 MHz	
		22.63	ARM core clock = 36 MHz	
			VDDI01= 3V @ 85°C	
		3.34	ARM core clock = 4 MHz	
		5.39	ARM core clock = 8 MHz	
		10.39	ARM core clock = 16 MHz	
		11.22	ARM core clock = 18 MHz	
		12.21	ARM core clock = 20 MHz	
		14.35	ARM core clock = 24 MHz	
		19.55	ARM core clock = 30 MHz	
		22.66	ARM core clock = 36 MHz	
Active (AT91SAM7L128/64) (See Figure 35-9)	Voltage regulator in Normal Mode VDDOUT = 1.55V RTC ON Programmable BOD ON (Continuous) Charge pump ON LCD Regulator ON Flash is read ADC ON All peripheral clocks activated RC 2MHz OFF PLL ON		VDDI01= 3V @ 25°C	mA
		2.73	ARM core clock = 4 MHz	
		4.47	ARM core clock = 8 MHz	
		8.55	ARM core clock = 16 MHz	
		9.23	ARM core clock = 18 MHz	
		10.1	ARM core clock = 20 MHz	
		11.9	ARM core clock = 24 MHz	
		16	ARM core clock = 30 MHz	
		18.6	ARM core clock = 36 MHz	
			VDDI01= 3V @ 85°C	
		2.76	ARM core clock = 4 MHz	
		4.52	ARM core clock = 8 MHz	
		8.62	ARM core clock = 16 MHz	
		9.33	ARM core clock = 18 MHz	
		10.21	ARM core clock = 20 MHz	
		12.04	ARM core clock = 24 MHz	
		16.07	ARM core clock = 30 MHz	
		18.75	ARM core clock = 36 MHz	

35.10.5.2 JTAG Interface Signals

Table 35-38. JTAG Interface Timing specification

Symbol	Parameter	Conditions	Min	Max	Units
$JTAG_0$	TCK Low Half-period	(1)	6.5		ns
$JTAG_1$	TCK High Half-period	(1)	5.5		ns
$JTAG_2$	TCK Period	(1)	12		ns
$JTAG_3$	TDI, TMS Setup before TCK High	(1)	2		ns
$JTAG_4$	TDI, TMS Hold after TCK High	(1)	3		ns
$JTAG_5$	TDO Hold Time	(1)	4		ns
$JTAG_6$	TCK Low to TDO Valid	(1)		16	ns
$JTAG_7$	Device Inputs Setup Time	(1)	0		ns
$JTAG_8$	Device Inputs Hold Time	(1)	3		ns
$JTAG_9$	Device Outputs Hold Time	(1)	6		ns
$JTAG_{10}$	TCK to Device Outputs Valid	(1)		18	ns

Note: 1. V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF.

Figure 35-18. JTAG Interface Signals