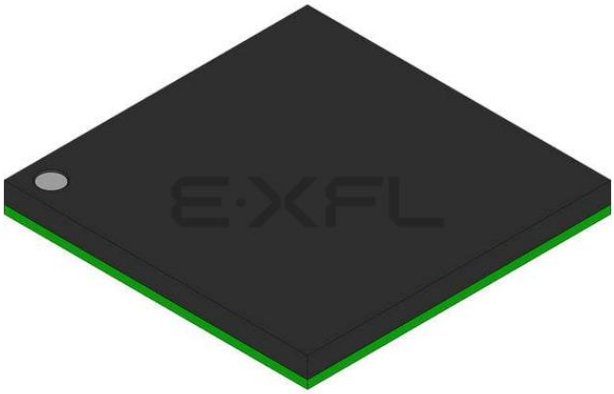

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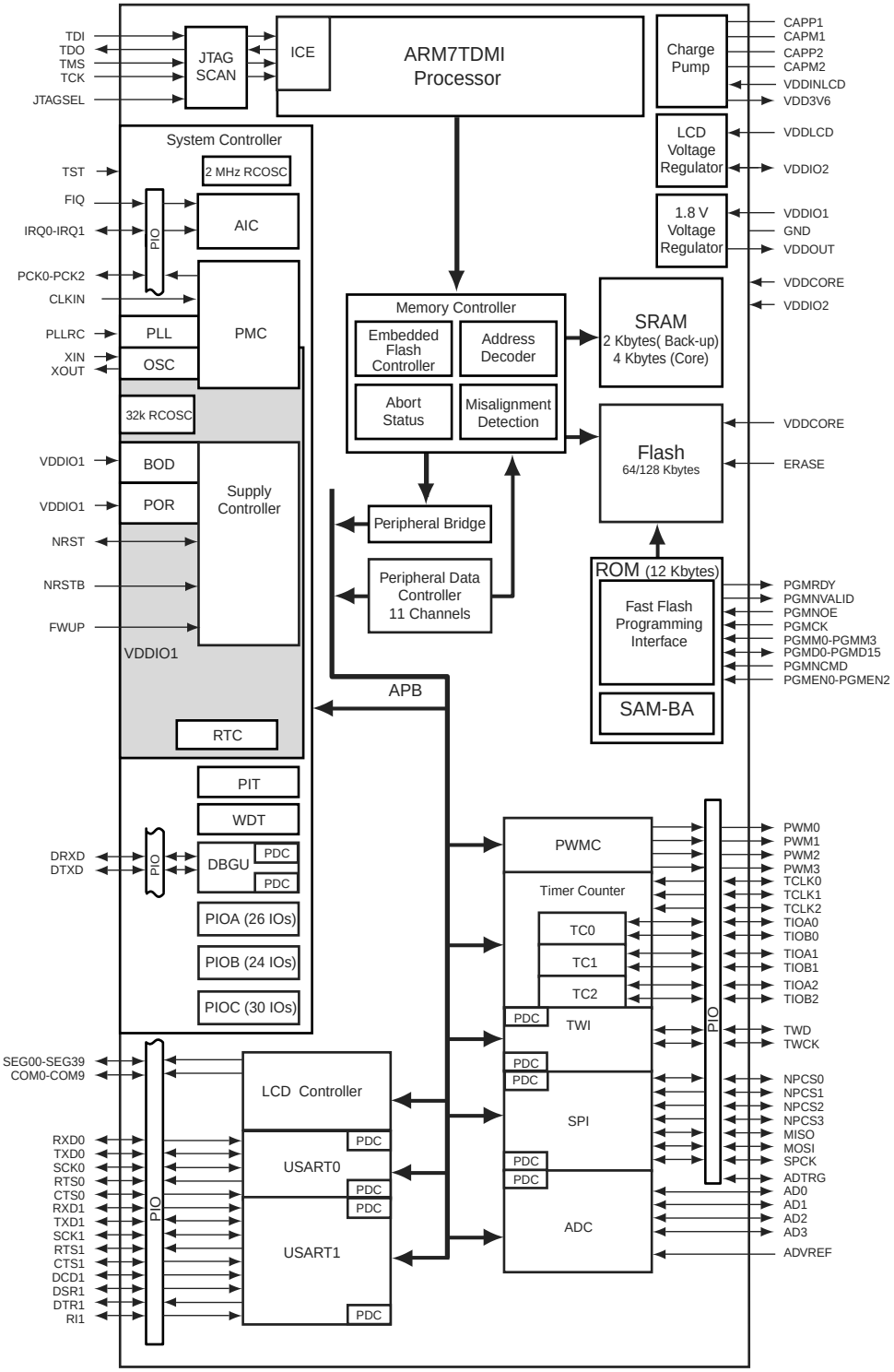
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	36MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.55V ~ 1.8V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-BGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at91sam7l64-cu

2. Block Diagram

Figure 2-1. AT91SAM7L128/64 Block Diagram



Adequate input supply decoupling is mandatory for VDDIO1 in order to improve startup stability and reduce source voltage drop. The input decoupling capacitor should be placed close to the chip. For example, two capacitors can be used in parallel, 100 nF NPO and 4.7 µF X7R.

5.6 LCD Power Supply

The AT91SAM7L128/64 embeds an on-chip LCD power supply comprising a regulated charge pump and an adjustable voltage regulator.

The regulated charge pump output delivers 3.6V as long as its input is supplied between 1.8V and 3.6V. The regulated charge pump only requires two external flying capacitors and one external tank capacitor to operate.

Adequate input supply decoupling is mandatory for VDDINLCD in order to improve startup stability and reduce source voltage drop. The input decoupling capacitor should be placed close to the chip.

Current consumption of the charge pump and LCD bias when active is 350 µA (max case).

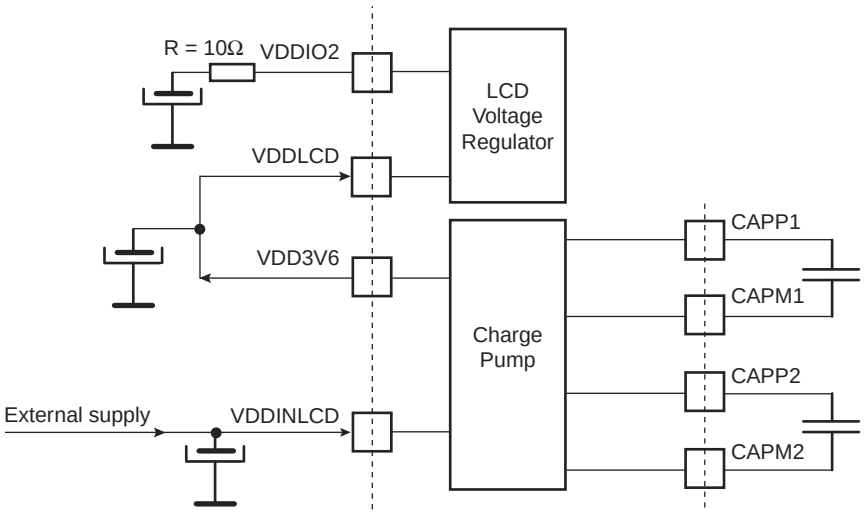
The regulated charge pump can be used to supply the LCD voltage regulator or as a 3.6V voltage reference delivering up to 4 mA.

The LCD voltage regulator output voltage is software selectable from 2.4V to 3.4V with 16 levels. Its input should be supplied in the range of 2.5 to 3.6V. The LCD voltage regulator can be supplied by the regulated charge pump output or by an external supply.

When the LCD voltage regulator is not used, its output must be connected to an external source in order to supply the PIOA and PIOB I/O lines.

Figure 5-3 below shows the typical schematics needed:

Figure 5-3. The Charge Pump Supplies the LCD Regulator



6. I/O Line Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are schmitt trigger inputs. TMS, TDI and TCK do not integrate a pull-up resistor.

TDO is an output, driven at up to VDDIO, and has no pull-up resistor.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. The JTAGSEL pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

6.2 Test Pin

The TST pin is used for manufacturing test or fast programming mode of the AT91SAM7L128/64 when asserted high. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

To enter fast programming mode, the TST and CLKIN pins must be tied high while FWUP is tied low.

6.3 NRST Pin

The NRST pin is bidirectional. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. There is no constraint on the length of the reset pulse and the reset controller can guarantee a minimum pulse length.

The NRST pin integrates a permanent pull-up resistor to VDDIO1 of about 100 kΩ.

6.4 NRSTB Pin

The NRSTB pin is input only and enables asynchronous reset of the AT91SAM7L128/64 when asserted low. The NRSTB pin integrates a permanent pull-up resistor of about 15 kΩ. This allows connection of a simple push button on the NRBST pin as a system-user reset.

In all modes, this pin will reset the chip. It can be used as an external system reset source.

In harsh environments, it is recommended to add an external capacitor (10 nF) between NRSTB and VDDIO1.

NRSTB pin must not be connected to VDDIO1. There must not be an external pull-up on NRSTB.

6.5 ERASE Pin

The ERASE pin is used to reinitialize the Flash content and some of its NVM bits. It integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

This pin is debounced by SCLK to improve the glitch tolerance. When the ERASE pin is tied high during less than 100 ms, it is not taken into account. The pin must be tied high during more than 220 ms to perform the reinitialization of the Flash.

6.6 PIO Controller Lines

All the I/O lines; PA0 to PA25, PB0 to PB23, PC0 to PC29 integrate a programmable pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the PIO controllers. All I/Os have input schmitt triggers.

Typical pull-up value is 100 kΩ.

Maximum frequency is:

- 36 MHz under 25 pF of load on PIOC
- 36 MHz under 25 pF of load on PIOA and PIOB

14.5.3 RTC Time Register

Name: RTC_TIMR

Access Type: Read-write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	AMPM	HOUR					

15	14	13	12	11	10	9	8
–	MIN						

7	6	5	4	3	2	1	0
–	SEC						

- **SEC: Current Second**

The range that can be set is 0 - 59 (BCD).

The lowest four bits encode the units. The higher bits encode the tens.

- **MIN: Current Minute**

The range that can be set is 0 - 59 (BCD).

The lowest four bits encode the units. The higher bits encode the tens.

- **HOUR: Current Hour**

The range that can be set is 1 - 12 (BCD) in 12-hour mode or 0 - 23 (BCD) in 24-hour mode.

- **AMPM: Ante Meridiem Post Meridiem Indicator**

This bit is the AM/PM indicator in 12-hour mode.

0 = AM.

1 = PM.

All non-significant bits read zero.

14.5.10 RTC Interrupt Disable Register

Name: RTC_IDR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	CALDIS	TIMDIS	SECDIS	ALRDIS	ACKDIS

- **ACKDIS: Acknowledge Update Interrupt Disable**

0 = No effect.

1 = The acknowledge for update interrupt is disabled.

- **ALRDIS: Alarm Interrupt Disable**

0 = No effect.

1 = The alarm interrupt is disabled.

- **SECDIS: Second Event Interrupt Disable**

0 = No effect.

1 = The second periodic interrupt is disabled.

- **TIMDIS: Time Event Interrupt Disable**

0 = No effect.

1 = The selected time event interrupt is disabled.

- **CALDIS: Calendar Event Interrupt Disable**

0 = No effect.

1 = The selected calendar event interrupt is disabled.

16.4.3 Watchdog Timer Status Register

Register Name: WDT_SR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	WDERR	WDUNF

- **WDUNF: Watchdog Underflow**

0: No Watchdog underflow occurred since the last read of WDT_SR.

1: At least one Watchdog underflow occurred since the last read of WDT_SR.

- **WDERR: Watchdog Error**

0: No Watchdog error occurred since the last read of WDT_SR.

1: At least one Watchdog error occurred since the last read of WDT_SR.

20. Fast Flash Programming Interface (FFPI)

20.1 Overview

The Fast Flash Programming Interface provides two solutions - parallel or serial - for high-volume programming using a standard gang programmer. The parallel interface is fully handshaked and the device is considered to be a standard EEPROM. Additionally, the parallel protocol offers an optimized access to all the embedded Flash functionalities. The serial interface uses the standard IEEE 1149.1 JTAG protocol. It offers an optimized access to all the embedded Flash functionalities.

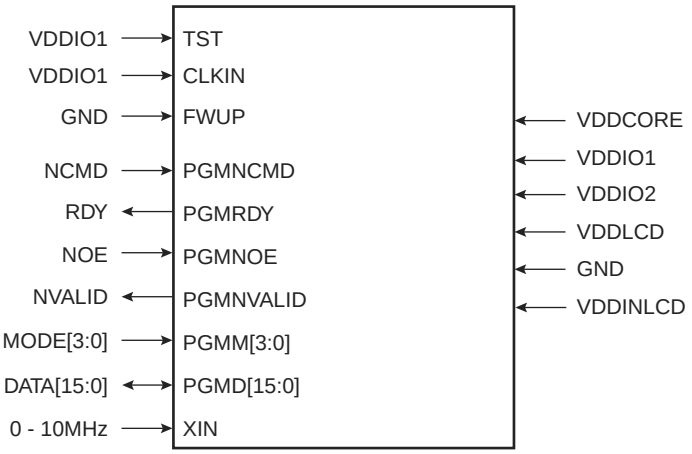
Although the Fast Flash Programming Mode is a dedicated mode for high volume programming, this mode is not designed for in-situ programming.

20.2 Parallel Fast Flash Programming

20.2.1 Device Configuration

In Fast Flash Programming Mode, the device is in a specific test mode. Only a certain set of pins is significant. Other pins must be left unconnected.

Figure 20-1. Parallel Programming Interface



The Master Clock is main clock divided by 16.

The Processor Clock is the Master Clock.

4. Selection of Programmable clocks

Programmable clocks are controlled via registers; PMC_SCER, PMC_SCDR and PMC_SCSR.

Programmable clocks can be enabled and/or disabled via the PMC_SCER and PMC_SCDR registers. 3 Programmable clocks can be enabled or disabled. The PMC_SCSR provides a clear indication as to which Programmable clock is enabled. By default all Programmable clocks are disabled.

PMC_PCKx registers are used to configure Programmable clocks.

The CSS field is used to select the Programmable clock divider source. Three clock options are available: main clock, slow clock, PLLCK. By default, the clock source selected is slow clock.

The PRES field is used to control the Programmable clock prescaler. It is possible to choose between different values (1, 2, 4, 8, 16, 32, 64). Programmable clock output is prescaler input divided by PRES parameter. By default, the PRES parameter is set to 0 which means that master clock is equal to slow clock.

Once the PMC_PCKx register has been programmed, The corresponding Programmable clock must be enabled and the user is constrained to wait for the PCKRDYx bit to be set in the PMC_SR register. This can be done either by polling the status register or by waiting the interrupt line to be raised if the associated interrupt to PCKRDYx has been enabled in the PMC_IER register. All parameters in PMC_PCKx can be programmed in a single write operation.

If the CSS and PRES parameters are to be modified, the corresponding Programmable clock must be disabled first. The parameters can then be modified. Once this has been done, the user must re-enable the Programmable clock and wait for the PCKRDYx bit to be set.

Code Example:

```
write_register(PMC_PCK0,0x00000015)
```

Programmable clock 0 is main clock divided by 32.

5. Enabling Peripheral Clocks

Once all of the previous steps have been completed, the peripheral clocks can be enabled and/or disabled via registers PMC_PCER and PMC_PCDR.

15 peripheral clocks can be enabled or disabled. The PMC_PCSR provides a clear view as to which peripheral clock is enabled.

Note: Each enabled peripheral clock corresponds to Master Clock.

Code Examples:

```
write_register(PMC_PCER,0x00000110)
```

Peripheral clocks 4 and 8 are enabled.

```
write_register(PMC_PCDR,0x00000010)
```

Peripheral clock 4 is disabled.

26.4.2 Receiver

26.4.2.1 Receiver Reset, Enable and Disable

After device reset, the Debug Unit receiver is disabled and must be enabled before being used. The receiver can be enabled by writing the control register DBGU_CR with the bit RXEN at 1. At this command, the receiver starts looking for a start bit.

The programmer can disable the receiver by writing DBGU_CR with the bit RXDIS at 1. If the receiver is waiting for a start bit, it is immediately stopped. However, if the receiver has already detected a start bit and is receiving the data, it waits for the stop bit before actually stopping its operation.

The programmer can also put the receiver in its reset state by writing DBGU_CR with the bit RSTRX at 1. In doing so, the receiver immediately stops its current operations and is disabled, whatever its current state. If RSTRX is applied when data is being processed, this data is lost.

26.4.2.2 Start Detection and Data Sampling

The Debug Unit only supports asynchronous operations, and this affects only its receiver. The Debug Unit receiver detects the start of a received character by sampling the DRXD signal until it detects a valid start bit. A low level (space) on DRXD is interpreted as a valid start bit if it is detected for more than 7 cycles of the sampling clock, which is 16 times the baud rate. Hence, a space that is longer than 7/16 of the bit period is detected as a valid start bit. A space which is 7/16 of a bit period or shorter is ignored and the receiver continues to wait for a valid start bit.

When a valid start bit has been detected, the receiver samples the DRXD at the theoretical midpoint of each bit. It is assumed that each bit lasts 16 cycles of the sampling clock (1-bit period) so the bit sampling point is eight cycles (0.5-bit period) after the start of the bit. The first sampling point is therefore 24 cycles (1.5-bit periods) after the falling edge of the start bit was detected.

Each subsequent bit is sampled 16 cycles (1-bit period) after the previous one.

Figure 26-4. Start Bit Detection

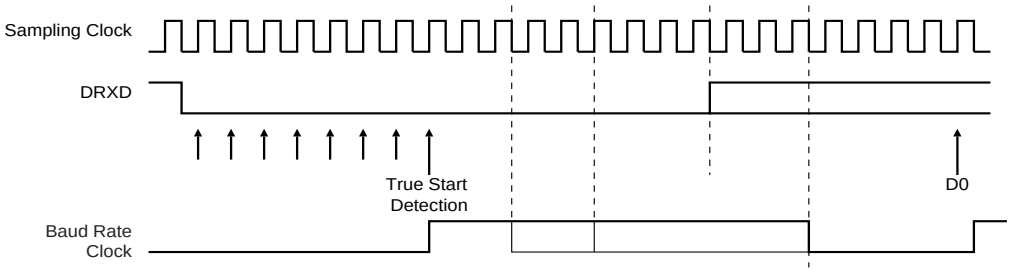
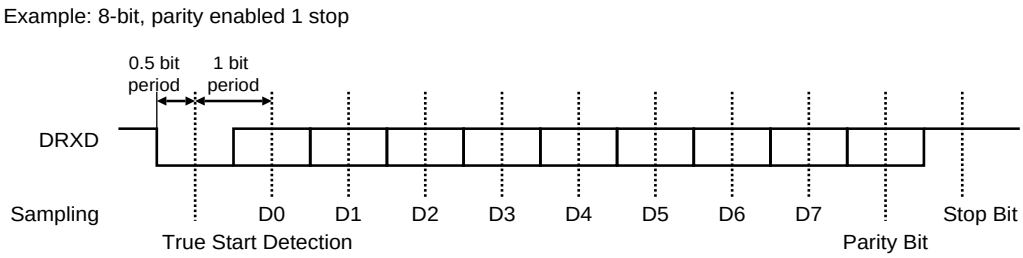


Figure 26-5. Character Reception



26.4.2.3 Receiver Ready

When a complete character is received, it is transferred to the DBGU_RHR and the RXRDY status bit in DBGU_SR (Status Register) is set. The bit RXRDY is automatically cleared when the receive holding register DBGU_RHR is read.

27.4 Functional Description

The PIO Controller features up to 32 fully-programmable I/O lines. Most of the control logic associated to each I/O is represented in Figure 27-3. In this description each signal shown represents but one of up to 32 possible indexes.

Figure 27-3. I/O Line Control Logic

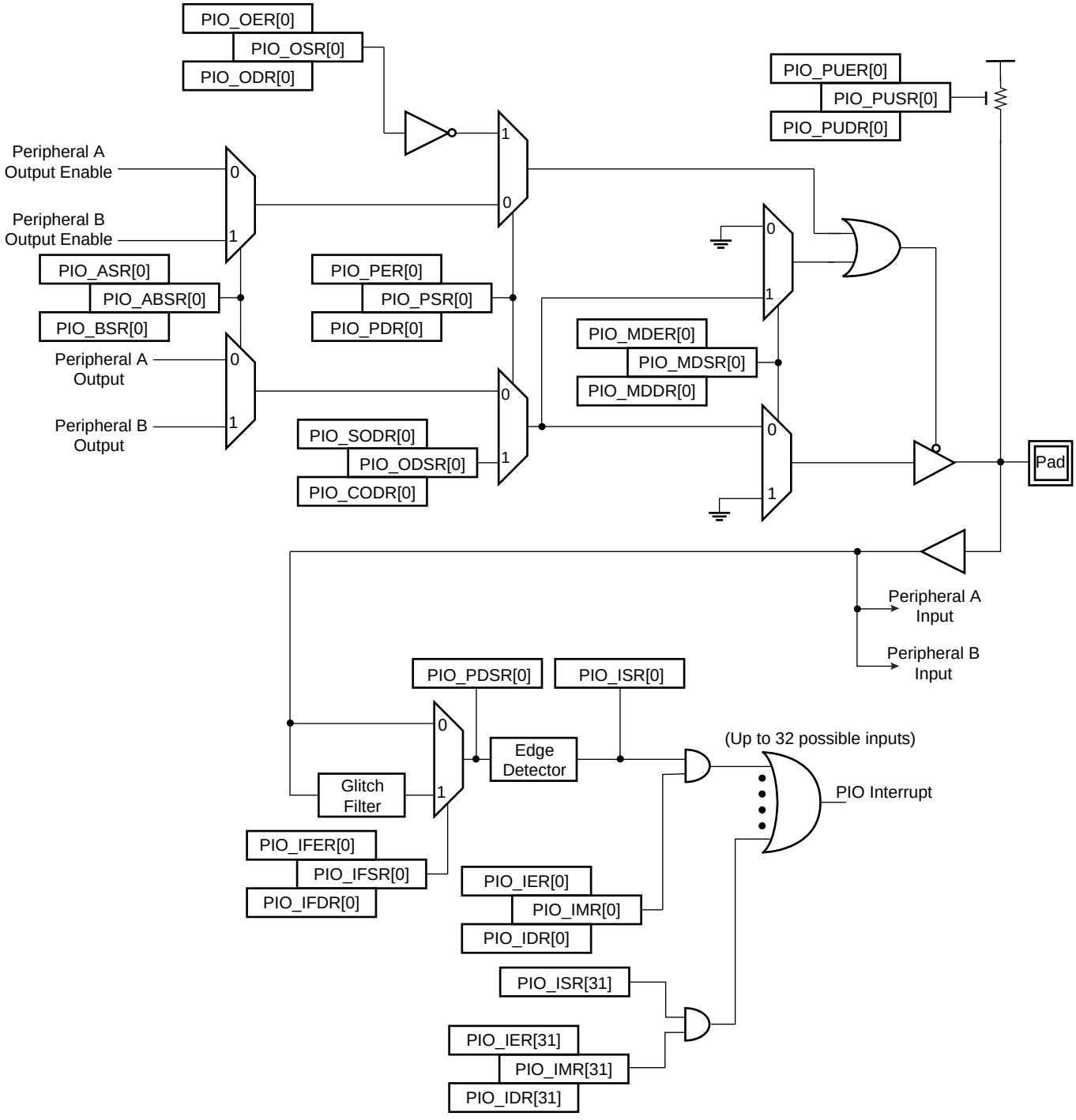
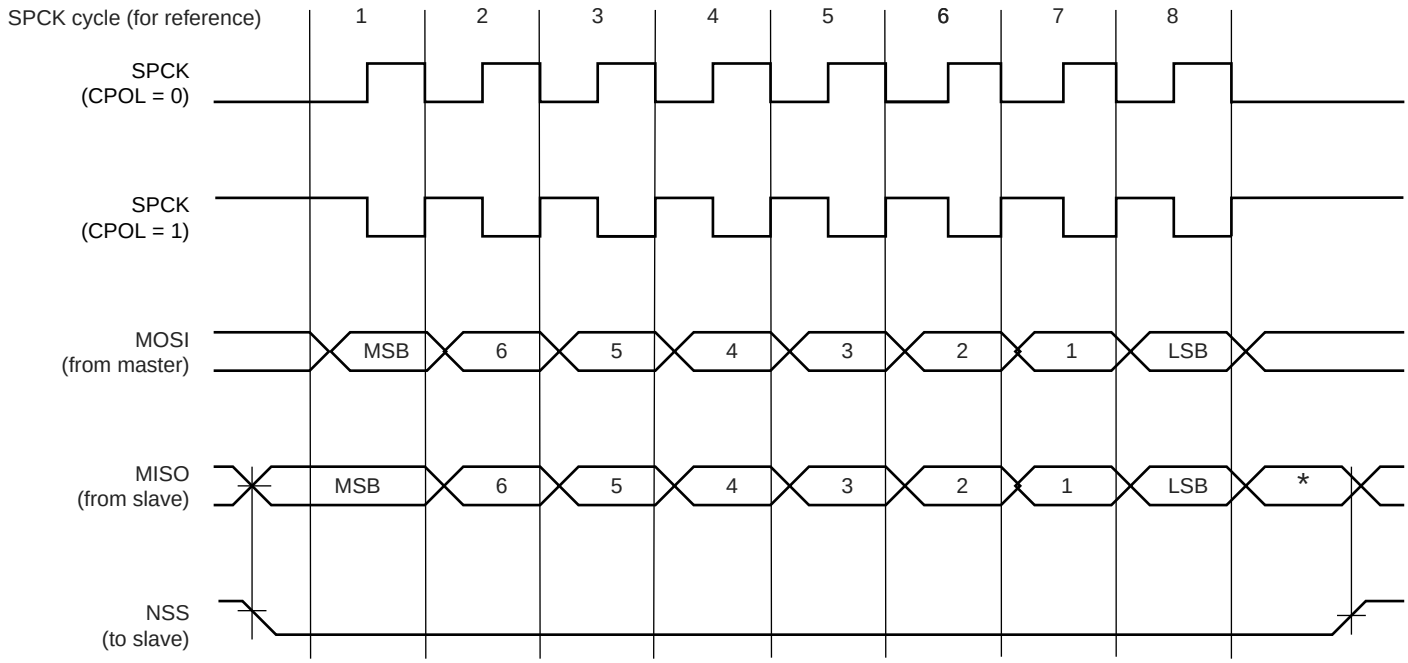
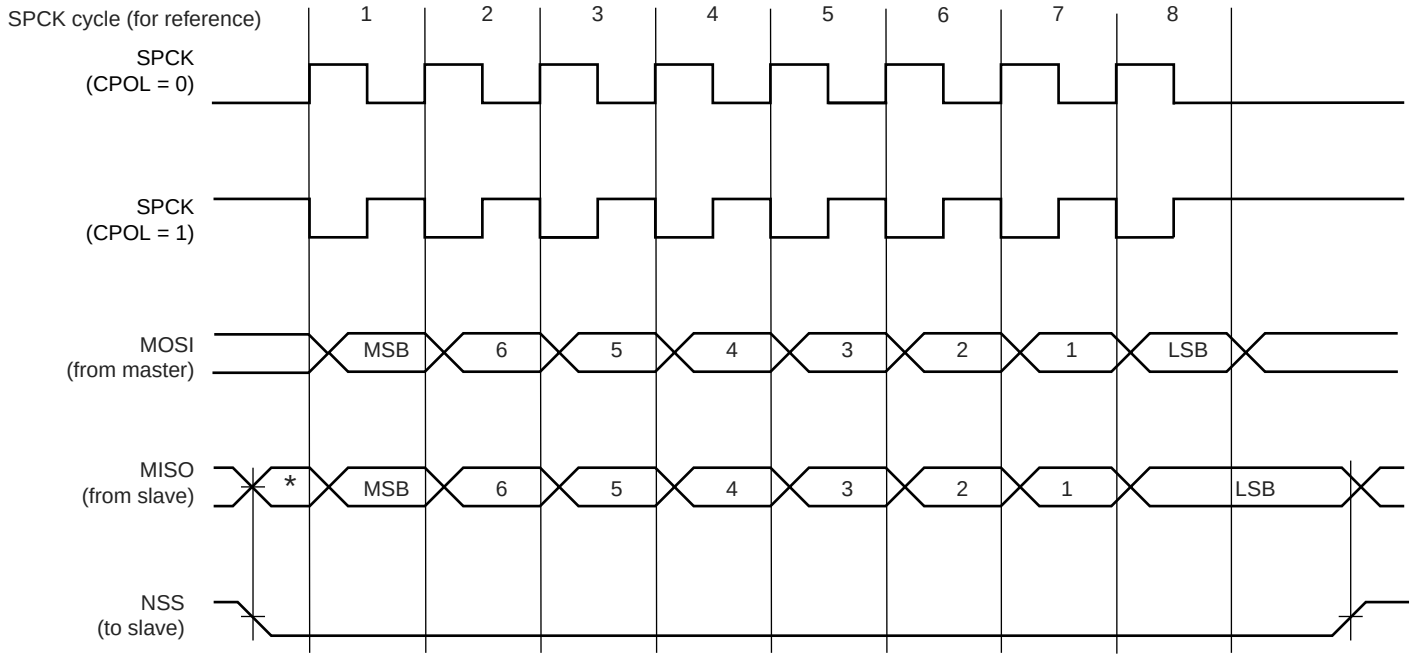


Figure 28-3. SPI Transfer Format (NCPHA = 1, 8 bits per transfer)



* Not defined, but normally MSB of previous character received.

Figure 28-4. SPI Transfer Format (NCPHA = 0, 8 bits per transfer)



* Not defined but normally LSB of previous character transmitted.

BITS	Bits Per Transfer
1101	Reserved
1110	Reserved
1111	Reserved

- **SCBR: Serial Clock Baud Rate**

In Master Mode, the SPI Interface uses a modulus counter to derive the SPCK baud rate from the Master Clock MCK. The Baud rate is selected by writing a value from 1 to 255 in the SCBR field. The following equations determine the SPCK baud rate:

$$\text{SPCK Baudrate} = \frac{MCK}{SCBR}$$

Programming the SCBR field at 0 is forbidden. Triggering a transfer while SCBR is at 0 can lead to unpredictable results.

At reset, SCBR is 0 and the user has to program it at a valid value before performing the first transfer.

- **DLYBS: Delay Before SPCK**

This field defines the delay from NPCS valid to the first valid SPCK transition.

When DLYBS equals zero, the NPCS valid to SPCK transition is 1/2 the SPCK clock period.

Otherwise, the following equations determine the delay:

$$\text{Delay Before SPCK} = \frac{DLYBS}{MCK}$$

- **DLYBCT: Delay Between Consecutive Transfers**

This field defines the delay between two consecutive transfers with the same peripheral without removing the chip select. The delay is always inserted after each transfer and before removing the chip select if needed.

When DLYBCT equals zero, no delay between consecutive transfers is inserted and the clock keeps its duty cycle over the character transfers.

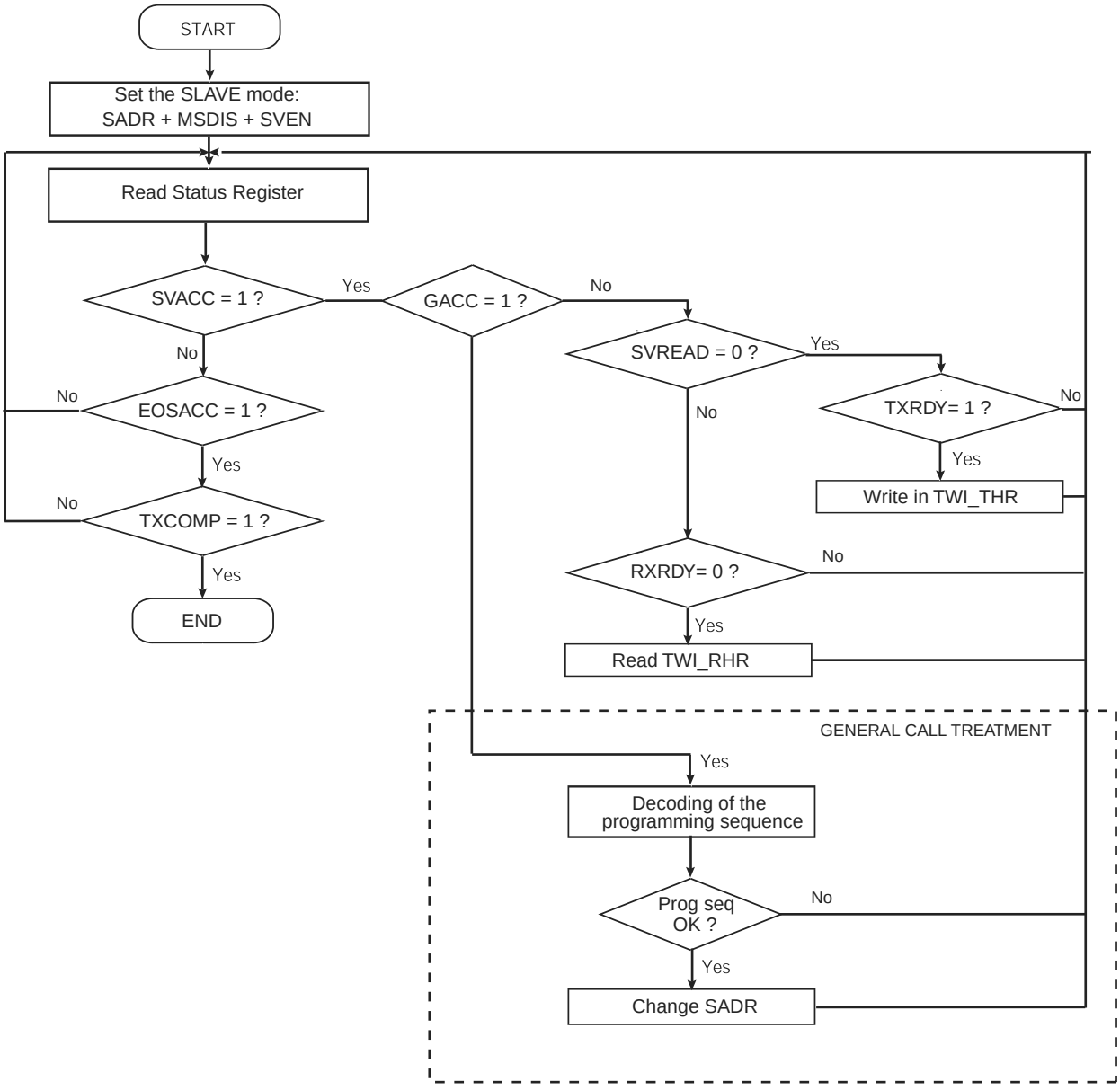
Otherwise, the following equation determines the delay:

$$\text{Delay Between Consecutive Transfers} = \frac{32 \times DLYBCT}{MCK}$$

29.9.6 Read Write Flowcharts

The flowchart shown in Figure 29-31 on page 336 gives an example of read and write operations in Slave mode. A polling or interrupt method can be used to check the status bits. The interrupt method requires that the interrupt enable register (TWI_IER) be configured first.

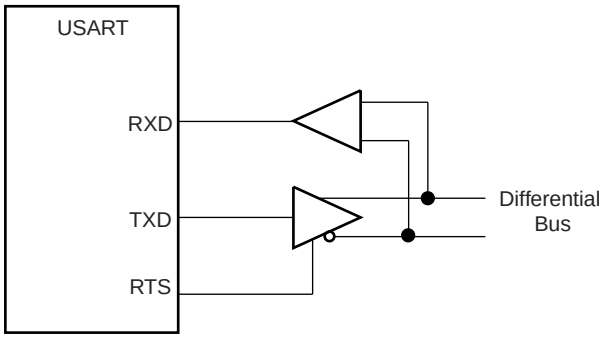
Figure 29-31. Read Write Flowchart in Slave Mode



30.6.6 RS485 Mode

The USART features the RS485 mode to enable line driver control. While operating in RS485 mode, the USART behaves as though in asynchronous or synchronous mode and configuration of all the parameters is possible. The difference is that the RTS pin is driven high when the transmitter is operating. The behavior of the RTS pin is controlled by the TXEMPTY bit. A typical connection of the USART to a RS485 bus is shown in Figure 30-36.

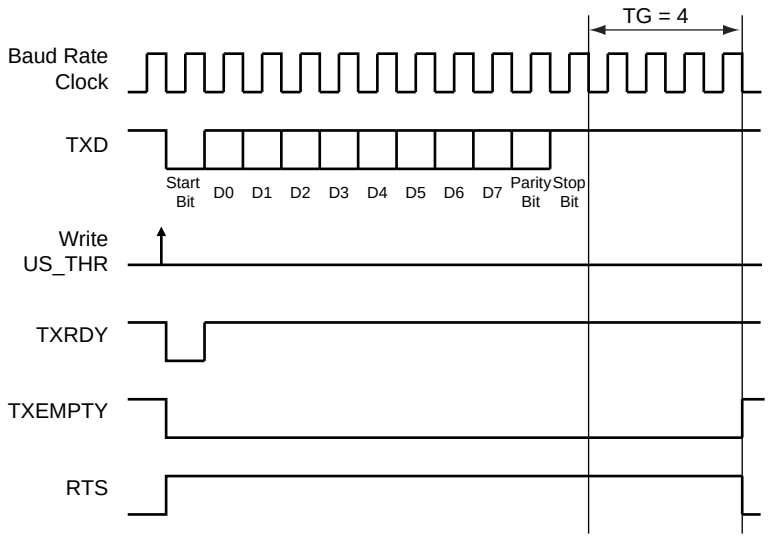
Figure 30-36. Typical Connection to a RS485 Bus



The USART is set in RS485 mode by programming the USART_MODE field in the Mode Register (US_MR) to the value 0x1.

The RTS pin is at a level inverse to the TXEMPTY bit. Significantly, the RTS pin remains high when a timeguard is programmed so that the line can remain driven after the last character completion. Figure 30-37 gives an example of the RTS waveform during a character transmission when the timeguard is enabled.

Figure 30-37. Example of RTS Drive with Timeguard



30.7.7 USART Receive Holding Register

Name: US_RHR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
RXSYNH	–	–	–	–	–	–	RXCHR
7	6	5	4	3	2	1	0
RXCHR							

- **RXCHR: Received Character**

Last character received if RXRDY is set.

- **RXSYNH: Received Sync**

0: Last Character received is a Data.

1: Last Character received is a Command.

Figure 31-2. Clock Chaining Selection

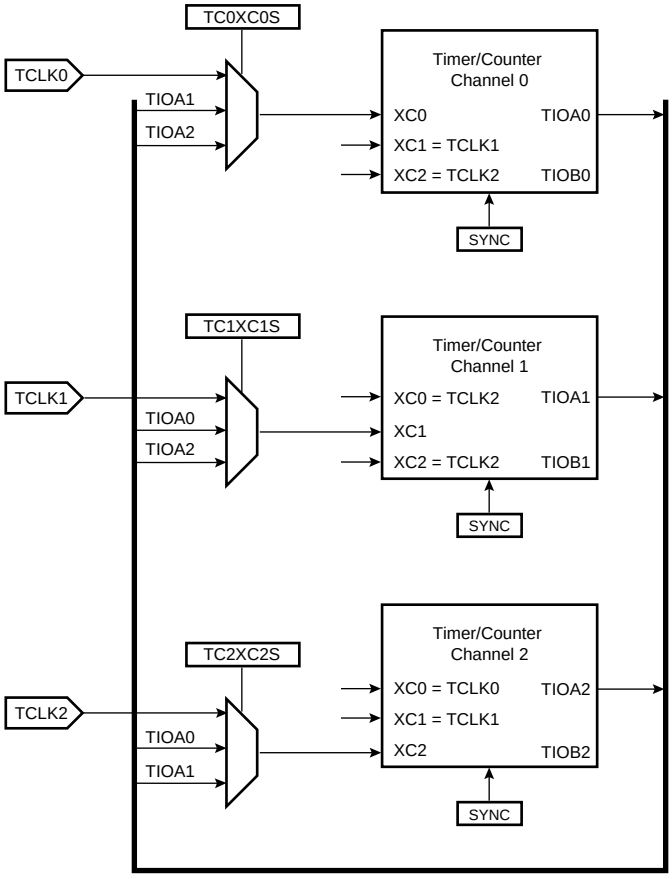
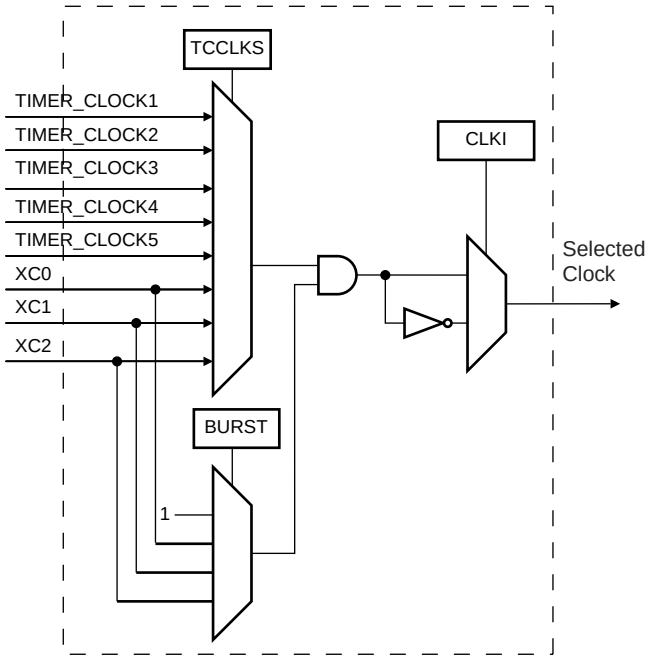


Figure 31-3. Clock Selection



31.6.1 TC Block Control Register

Register Name: TC_BCR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	SYNC

- **SYNC: Synchro Command**

0 = No effect.

1 = Asserts the SYNC signal which generates a software trigger simultaneously for each of the channels.

35.2 DC Characteristics

The following characteristics are applicable to the operating temperature range: T_A = -40°C to 85°C, unless otherwise specified.

Table 35-2. DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DDCORE}	DC Supply Core	Depends on VDDOUT (externally connected to VDDOUT)		VDDOUT		V
V_{VDDIO1}	DC Supply I/Os		1.8		3.6	V
V_{VDDIO2}	DC Supply I/Os	Adjustable	1.8		3.6	V
$V_{VDDINLCD}$	DC Supply Charge Pump		1.8		3.6	V
V_{VDDLCD}	DC Supply LCD Regulator		2.5		3.6	V
V_{IL}	Input Low-level Voltage	V_{VDDIO1} from 1.8V to 3.6V PC0-PC29, NRST, NRSTB, CLKIN	-0.3		0.3 x V_{VDDIO1}	V
		V_{VDDIO2} from 1.8V to 3.6V PA0-PA25, PB0-PB23	-0.3		0.3 x V_{VDDIO2}	V
V_{IH}	Input High-level Voltage	V_{VDDIO1} from 1.8V to 3.6V PC0-PC29, NRST, NRSTB, CLKIN	0.7 x V_{VDDIO1}		V_{VDDIO1} +0.3V	V
		V_{VDDIO2} from 1.8V to 3.6V PA0-PA25, PB0-PB23	0.7 x V_{VDDIO2}		V_{VDDIO2} +0.3V	V
V_{Hys}	Hysteresis Voltage	V_{VDDIO1} from 1.8V to 3.6V PC0-PC29, NRST, NRSTB, CLKIN	0.25		0.65	V
		V_{VDDIO2} from 1.8V to 3.6V PA0-PA25, PB0-PB23	0.25		0.7	V
V_{OL}	Output Low-level Voltage	I_O max, V_{VDDIO1} from 1.8V to 3.6V PC0-PC29, NRST			0.4	V
		I_O max, V_{VDDIO2} from 1.8V to 3.6V PA0-PA25, PB0-PB23			0.4	
V_{OH}	Output High-level Voltage	I_O max, V_{VDDIO1} from 1.8V to 3.6V PC0-PC29, NRST	V_{VDDIO1} - 0.4			V
		I_O max, V_{VDDIO2} from 1.8V to 3.6V PA0-PA25, PB0-PB23	V_{VDDIO2} - 0.4			V
I_O	Output current	V_{VDDIO1} from 1.8V to 3.6V PC0-PC6, PC11-PC29, NRST V_{VDDIO2} from 1.8V to 3.6V PA0-PA25, PB0-PB23,			2	mA
		V_{VDDIO1} from 1.8V to 3.6V PC7-PC10			4	

Table 35-26. Transfer Characteristics (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Offset Error				±3	LSB
Gain Error				±2	LSB
Absolute accuracy				±4.2	LSB

35.7 Regulated Charge Pump Characteristics

Table 35-27. Regulated Charge Pump Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{VDDINLCD}$	Charge Pump Supply Voltage		1.8	2.7	3.6	V
V_{VDD3V6}	Output Voltage	I_O = 4 mA max			3.6	V
$I_{VDDINLCD}$	Current consumption	Active, No load, with clock, CL = 4.7µF, ESR = 1Ω				µA
		Onto VDDIO1 = 1.8V			50	
		Onto VDDINLCD = 1.8V			250	
		Onto VDDIO1 = 3.6V			50	
		Onto VDDINLCD = 3.6V			65	
T_{START}	Startup Time				4	mS
	External charge capacitor	Between CAPP1 and CAPM1 (Tolerance +/- 10%)		220		nF
	External charge capacitor	Between CAPP2 and CAPM2 (Tolerance +/- 10%)		220		nF
	External storage capacitor	On VDD3V6 (Tolerance +/- 10%,ESR =<1Ω)		4.7		µF

Figure 35-12. Charge Pump Schematics