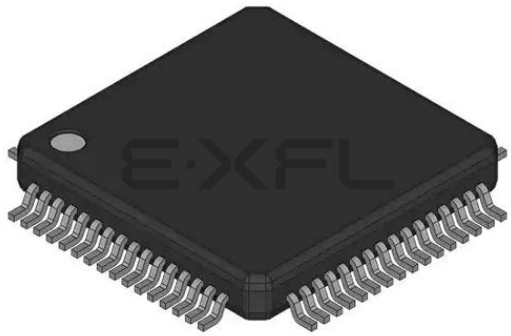

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM® Cortex®-M4F |
| Core Size | 32-Bit Single-Core |
| Speed | 160MHz |
| Connectivity | CANbus, CSIO, I²C, LINbus, UART/USART, USB |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 48 |
| Program Memory Size | 288KB (288K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 15x12b; D/A 2x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/rochester-electronics/mb9bf564lpmc-g-jne2 |

### Multi-function Serial Interface (Max 6 channels)

- 64 bytes with FIFO (the FIFO step numbers are variable depending on the settings of the communication mode or bit length.)
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - LIN
  - $I^2C$
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Hardware Flow control : Automatically control the transmission by CTS/RTS (only ch.4)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
  - Serial chip select function (ch.6 only)
  - Supports high-speed SPI (ch.0 and ch.6 only)
  - Data length 5 to 16-bit
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/Slave mode supported
  - LIN break field generation (can change to 13 to 16-bit length)
  - LIN break delimiter generation (can change to 1 to 4-bit length)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- $I^2C$
  - Standard mode (Max 100 kbps) / High-speed mode (Max 400 kbps) supported
  - Fast mode Plus (Fm+) (Max 1000 kbps, only for ch.3=ch.A and ch.4=ch.B) supported

### DMA Controller (8 channels)

DMA Controller has an independent bus for CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 Gbytes)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

### DSTC (Descriptor System data Transfer Controller) (128 channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the Descriptor system and, following the specified contents of the Descriptor which has already been constructed on the memory, can access directly the memory /peripheral device and performs the data transfer operation.

It supports the software activation, the hardware activation and the chain activation functions.

### A/D Converter (Max 15 channels) [12-bit A/D Converter]

- Successive Approximation type
- Built-in 2 units
- Conversion time: 0.5 µs @ 5 V
- Priority conversion available (priority at 2levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16steps, for Priority conversion: 4steps)

### DA Converter (Max 2 channels)

- R-2R type
- 12-bit resolution

### Base Timer (Max 8 channels)

Operation mode is selectable from the followings for each channel.

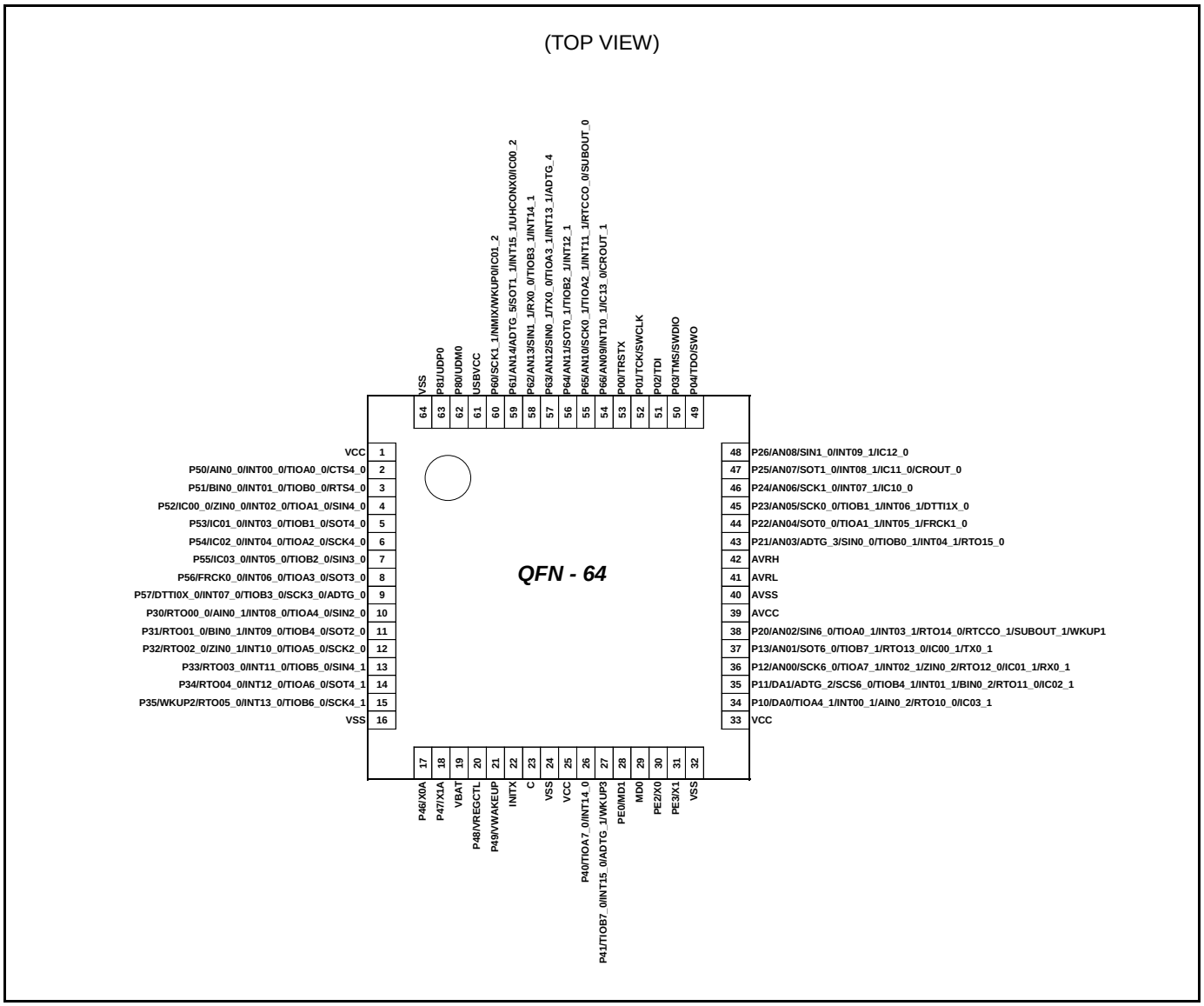
- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

### General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 48 high-speed general-purpose I/O ports @ 64 pin Package
- Some pin is 5 V tolerant I/O.
  See 4. Pin Description and 5. I/O Circuit Type for the corresponding pins.

**LCC-64P-M24**




***Note:***

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

# 4. Pin Description

## 4.1 List of Pin Numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

| Pin No | | Pin Name | I/O circuit type | Pin state type |
|---|---|---|---|---|
| LQFP64 QFN64 | LQFP48 QFN48 | | | |
| 1 | 1 | VCC | - | - |
| 2 | - | P50 | E | K |
| | | AIN0_0 | | |
| | | INT00_0 | | |
| | | TIOA0_0 | | |
| | | CTS4_0 | | |
| 3 | - | P51 | E | K |
| | | BIN0_0 | | |
| | | INT01_0 | | |
| | | TIOB0_0 | | |
| | | RTS4_0 | | |
| 4 | - | P52 | I | K |
| | | IC00_0 | | |
| | | ZIN0_0 | | |
| | | INT02_0 | | |
| | | TIOA1_0 | | |
| | | SIN4_0 | | |
| 5 | - | P53 | N | K |
| | | IC01_0 | | |
| | | INT03_0 | | |
| | | TIOB1_0 | | |
| | | SOT4_0 (SDA4_0) | | |
| 6 | 2 | P54 | N | K |
| | | IC02_0 | | |
| | | INT04_0 | | |
| | | TIOA2_0 | | |
| | - | SCK4_0 (SCL4_0) | | |
| 7 | 3 | P55 | I | K |
| | | IC03_0 | | |
| | | INT05_0 | | |
| | | TIOB2_0 | | |
| | | SIN3_0 | | |
| 8 | 4 | P56 | N | K |
| | | FRCK0_0 | | |
| | | INT06_0 | | |
| | | TIOA3_0 | | |
| | | SOT3_0 (SDA3_0) | | |

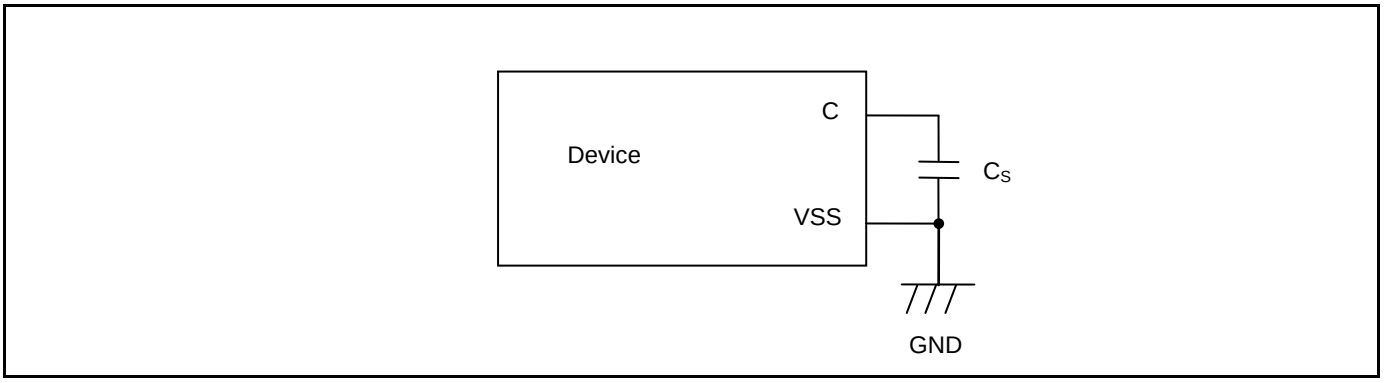
| Pin function | Pin name | Function description | Pin No | |
|---|---|---|---|---|
| | | | LQFP64 QFN64 | LQFP48 QFN48 |
| Multi-function Serial 0 | SIN0_0 | Multi-function serial interface ch.0 input pin | 43 | 34 |
| | SIN0_1 | | 57 | - |
| | SOT0_0 (SDA0_0) | Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an $I^2C$ (operation mode 4). | 44 | 35 |
| | SOT0_1 (SDA0_1) | | 56 | - |
| | SCK0_0 (SCL0_0) | Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a CSIO (operation modes 2) and as SCL0 when it is used in an $I^2C$ (operation mode 4). | 45 | 36 |
| | SCK0_1 (SCL0_1) | | 55 | - |
| Multi-function Serial 1 | SIN1_0 | Multi-function serial interface ch.1 input pin | 48 | - |
| | SIN1_1 | | 58 | - |
| | SOT1_0 (SDA1_0) | Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an $I^2C$ (operation mode 4). | 47 | - |
| | SOT1_1 (SDA1_1) | | 59 | 43 |
| | SCK1_0 (SCL1_0) | Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation modes 2) and as SCL1 when it is used in an $I^2C$ (operation mode 4). | 46 | - |
| | SCK1_1 (SCL1_1) | | 60 | 44 |
| Multi-function Serial 2 | SIN2_0 | Multi-function serial interface ch.2 input pin | 10 | 6 |
| | SOT2_0 (SDA2_0) | Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an $I^2C$ (operation mode 4). | 11 | 7 |
| | SCK2_0 (SCL2_0) | Multi-function serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a CSIO (operation modes 2) and as SCL2 when it is used in an $I^2C$ (operation mode 4). | 12 | 8 |

### Handling when Using Multi-function Serial Pin as I²C Pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled.
However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

### C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor ($C_S$) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7 µF would be recommended for this series.




### Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

### Notes on Power-on

Turn power on/off in the following order or at the same time.
If not using the A/D converter and D/A converter, connect AVCC = VCC and AVSS = VSS.

| | |
|---|---|
| Turning on: | VBAT → VCC → USBVCC |
| | VCC → AVCC → AVRH |
| Turning off: | USBVCC → VCC → VBAT |
| | AVRH → AVCC → VCC |

### Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data.

### Differences in Features among the Products with Different Memory Sizes and between Flash Products and MASK Products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.
If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

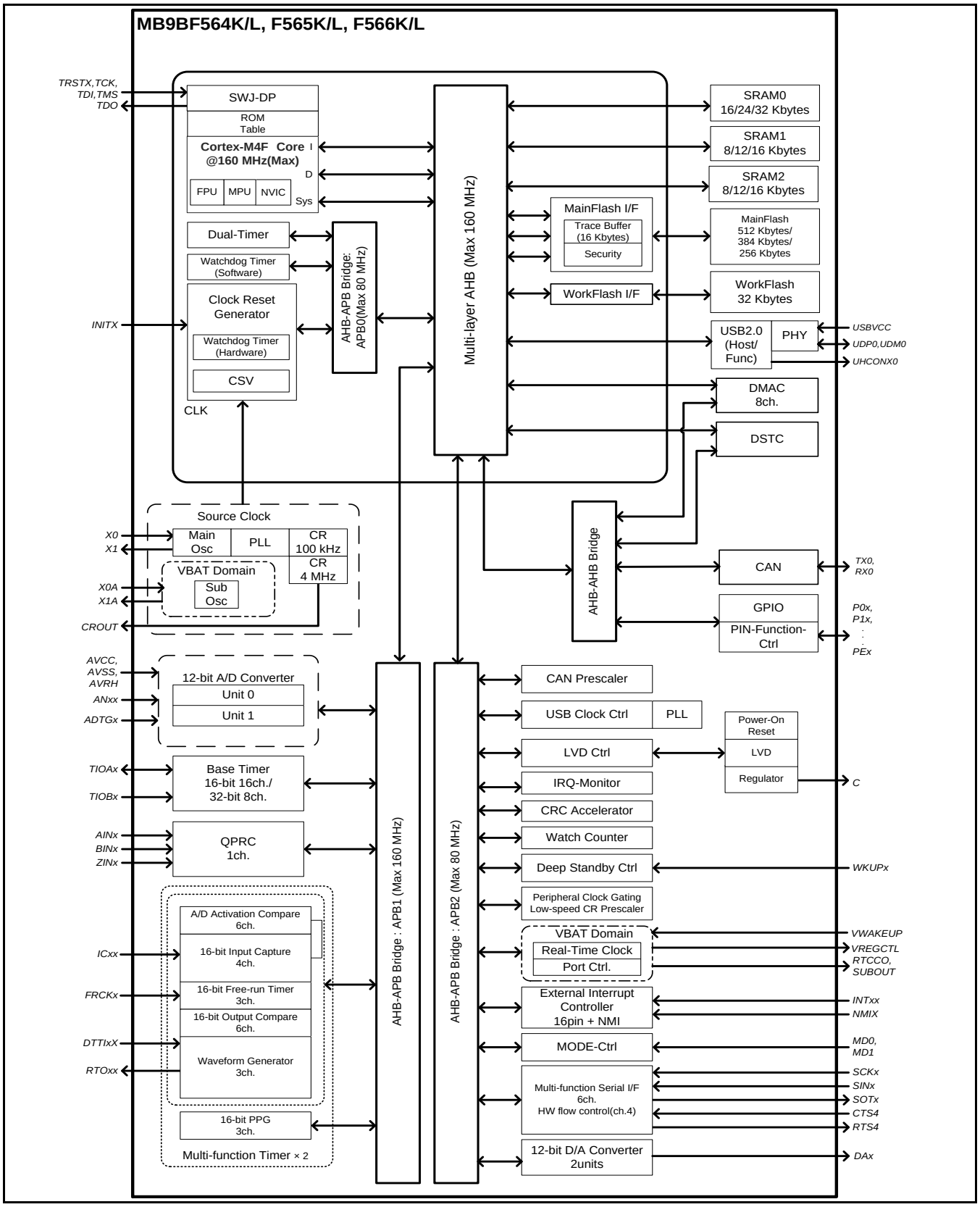
### Pull-Up Function of 5 V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of pull-up function use of 5V tolerant I/O.

### Handling when Using Debug Pins

When debug pins (TDO/TMS/TDI/TCK/TRSTX or SWO/SWDIO/SWCLK) are set to GPIO or other peripheral functions, only set them as output, do not set them as input.

## 8. Block Diagram



## Peripheral Address Map

| Start address | End address | Bus | Peripherals |
|---|---|---|---|
| 0x4000_0000 | 0x4000_0FFF | AHB | MainFlash I/F register |
| 0x4000_1000 | 0x4000_FFFF | | Reserved |
| 0x4001_0000 | 0x4001_0FFF | APB0 | Clock/Reset Control |
| 0x4001_1000 | 0x4001_1FFF | | Hardware Watchdog timer |
| 0x4001_2000 | 0x4001_2FFF | | Software Watchdog timer |
| 0x4001_3000 | 0x4001_4FFF | | Reserved |
| 0x4001_5000 | 0x4001_5FFF | | Dual-Timer |
| 0x4001_6000 | 0x4001_FFFF | | Reserved |
| 0x4002_0000 | 0x4002_0FFF | APB1 | Multi-function timer unit0 |
| 0x4002_1000 | 0x4002_1FFF | | Multi-function timer unit1 |
| 0x4002_2000 | 0x4003_FFFF | | Reserved |
| 0x4002_4000 | 0x4002_4FFF | | PPG |
| 0x4002_5000 | 0x4002_5FFF | | Base Timer |
| 0x4002_6000 | 0x4002_6FFF | | Quadrature Position/Revolution Counter |
| 0x4002_7000 | 0x4002_7FFF | | A/D Converter |
| 0x4002_8000 | 0x4002_DFFF | | Reserved |
| 0x4002_E000 | 0x4002_EFFF | | Internal CR trimming |
| 0x4002_F000 | 0x4002_FFFF | | Reserved |
| 0x4003_0000 | 0x4003_0FFF | APB2 | External Interrupt Controller |
| 0x4003_1000 | 0x4003_1FFF | | Interrupt Request Batch-Read Function |
| 0x4003_2000 | 0x4003_4FFF | | Reserved |
| 0x4003_3000 | 0x4003_3FFF | | D/A Converter |
| 0x4003_4000 | 0x4003_4FFF | | Reserved |
| 0x4003_5000 | 0x4003_57FF | | Low Voltage Detector |
| 0x4003_5800 | 0x4003_5FFF | | Deep standby mode Controller |
| 0x4003_6000 | 0x4003_6FFF | | USB clock generator |
| 0x4003_7000 | 0x4003_7FFF | | CAN prescaler |
| 0x4003_8000 | 0x4003_8FFF | | Multi-function serial Interface |
| 0x4003_9000 | 0x4003_9FFF | | CRC |
| 0x4003_A000 | 0x4003_AFFF | | Watch Counter |
| 0x4003_B000 | 0x4003_BFFF | | RTC/Port Ctrl |
| 0x4003_C000 | 0x4003_C0FF | | Low-speed CR Prescaler |
| 0x4003_C100 | 0x4003_C7FF | | Peripheral Clock Gating |
| 0x4003_C800 | 0x4003_FFFF | | Reserved |
| 0x4004_0000 | 0x4004_FFFF | AHB | USB ch.0 |
| 0x4005_0000 | 0x4005_FFFF | | Reserved |
| 0x4006_0000 | 0x4006_0FFF | | DMAC register |
| 0x4006_1000 | 0x4006_1FFF | | DSTC register |
| 0x4006_2000 | 0x4006_2FFF | | CAN ch.0 |
| 0x4006_3000 | 0x4006_EFFF | | Reserved |
| 0x4006_F000 | 0x4006_FFFF | | GPIO |
| 0x4006_7000 | 0x41FF_FFFF | | Reserved |
| 0x200E_0000 | 0x200E_FFFF | | WorkFlash I/F register |

| Parameter | Symbol | Pin Name | Conditions | | Frequency*4 (MHz) | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Typ*1 | Max*2 | | |
| Power supply current | $I_{CC}$ | VCC | Normal operation (PLL) | *5 | 72 MHz | 41 | 75 | mA | *3 When all peripheral clocks are ON |
| | | | | | 60 MHz | 36 | 69 | | |
| | | | | | 48 MHz | 31 | 64 | | |
| | | | | | 36 MHz | 25 | 57 | | |
| | | | | | 24 MHz | 18 | 50 | | |
| | | | | | 12 MHz | 11 | 42 | | |
| | | | | | 8 MHz | 8.1 | 39 | | |
| | | | | | 4 MHz | 5.4 | 37 | | |
| | | | | | 72 MHz | 32 | 63 | mA | *3 When all peripheral clocks are OFF |
| | | | | | 60 MHz | 28 | 58 | | |
| | | | | | 48 MHz | 24 | 54 | | |
| | | | | | 36 MHz | 20 | 50 | | |
| | | | | | 24 MHz | 15 | 45 | | |
| | | | | | 12 MHz | 9.1 | 38 | | |
| | | | | | 8 MHz | 6.9 | 36 | | |
| | | | | | 4 MHz | 4.6 | 34 | | |

*1: $T_A$=+25 °C, $V_{CC}$=3.3 V

*2: Tj=+125 °C, $V_{CC}$=5.5 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK

*5: When 0 wait-cycle mode (FRWTR.RWT = 00, FSYNDN.SD = 00)

| Parameter | Symbol | Pin Name | Conditions | | Frequency*4 | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Typ*1 | Max*2 | | |
| Power supply current | $I_{CC}$ | VCC | Normal operation (built-in high-speed CR) | *5 | 4 MHz | 3.3 | 29 | mA | *3 When all peripheral clocks are ON |
| | | | | | | 2.8 | 29 | mA | *3 When all peripheral clocks are OFF |
| | | | Normal operation (sub oscillation) | *5 | 32 kHz | 0.51 | 27 | mA | *3 When all peripheral clocks are ON |
| | | | | | | 0.50 | 27 | mA | *3 When all peripheral clocks are OFF |
| | | | Normal operation (built-in low-speed CR) | *5 | 100 kHz | 0.54 | 27 | mA | *3 When all peripheral clocks are ON |
| | | | | | | 0.52 | 27 | mA | *3 When all peripheral clocks are OFF |

*1: $T_A$=+25 °C, $V_{CC}$=3.3 V

*2: Tj=+125 °C, $V_{CC}$=5.5 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

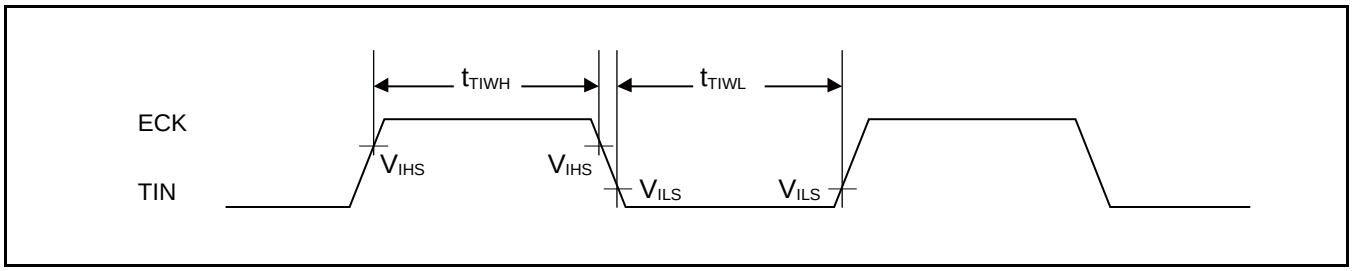
*5: When 0 wait-cycle mode (FRWTR.RWT = 00, FSYNDN.SD = 000)

### *12.4.10 Base Timer Input Timing*

#### Timer Input Timing

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

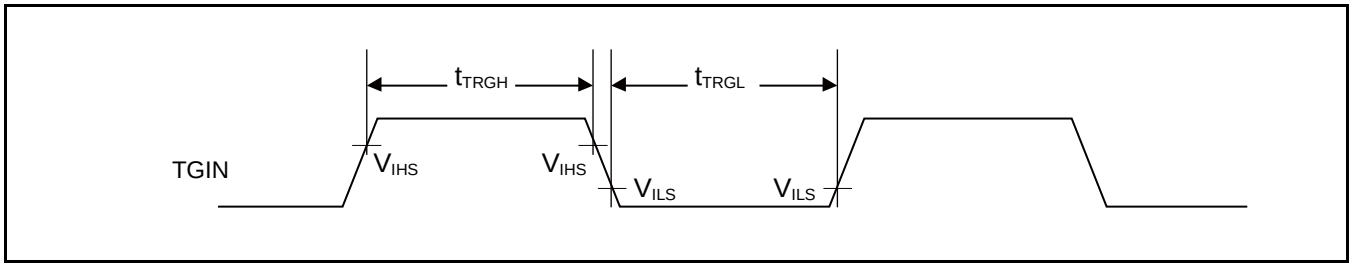
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TIWH}$, $t_{TIWL}$ | TIOAn/TIOBn (when using as ECK, TIN) | - | $2t_{CYCP}$ | - | ns | |




#### Trigger Input Timing

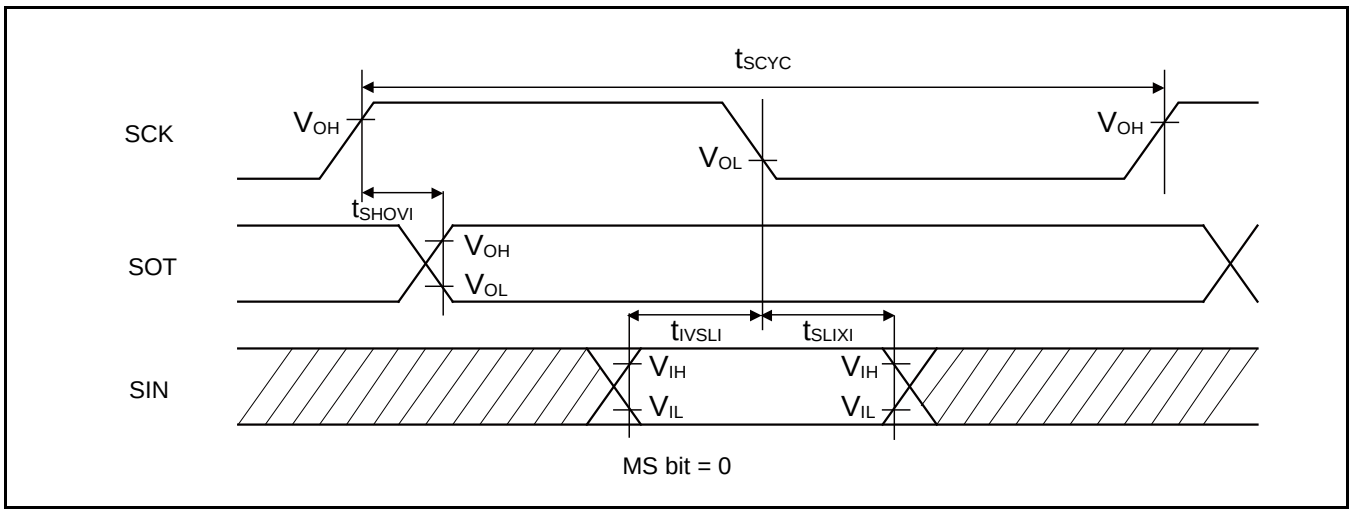
($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TRGH}$, $t_{TRGL}$ | TIOAn/TIOBn (when using as TGIN) | - | $2t_{CYCP}$ | - | ns | |

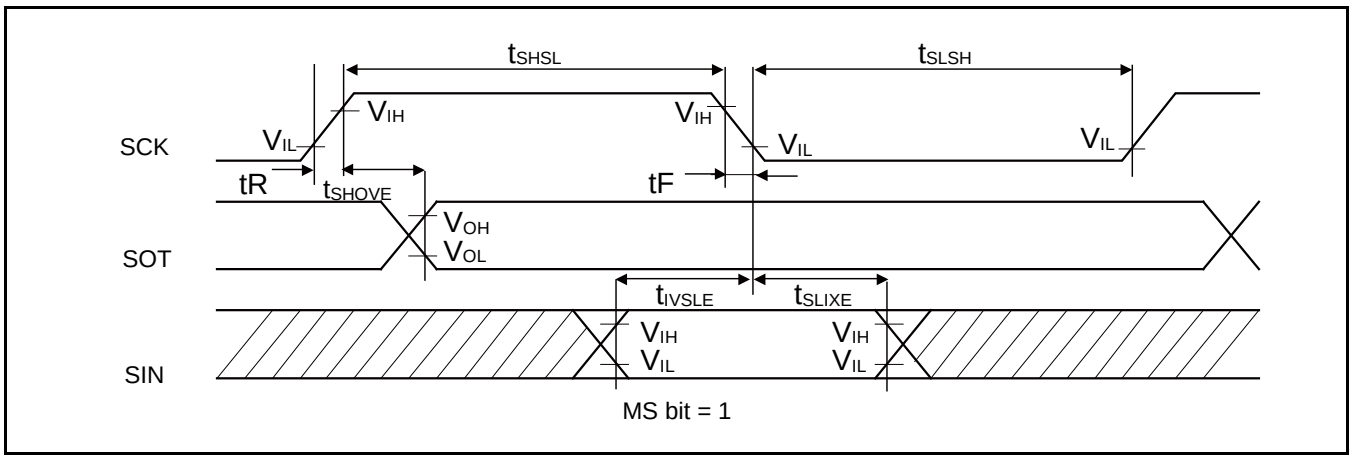



***Note:***

- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which the Base Timer is connected to, see 8. Block Diagram in this data sheet.*




MS bit = 0




MS bit = 1

### Synchronous Serial (SPI = 1, SCINV = 1)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin Name | Conditions | $V_{CC}$ < 4.5 V | | $V_{CC}$ ≥ 4.5 V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCKx | Internal shift clock operation | $4t_{CYCP}$ | - | $4t_{CYCP}$ | - | ns |
| SCK↓→SOT delay time | $t_{SLOVI}$ | SCKx, SOTx | | - 30 | + 30 | - 20 | + 20 | ns |
| SIN→SCK↑ setup time | $t_{IVSHI}$ | SCKx, SINx | | 50 | - | 30 | - | ns |
| SCK↑→SIN hold time | $t_{SHIXI}$ | SCKx, SINx | | 0 | - | 0 | - | ns |
| SOT→SCK↑ delay time | $t_{SOVHI}$ | SCKx, SOTx | | $2t_{CYCP}$ - 30 | - | $2tC_{YCP}$ - 30 | - | ns |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCKx | External shift clock operation | $2t_{CYCP}$ - 10 | - | $2t_{CYCP}$ - 10 | - | ns |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCKx | | $t_{CYCP}$ + 10 | - | $t_{CYCP}$ + 10 | - | ns |
| SCK↓→SOT delay time | $t_{SLOVE}$ | SCKx, SOTx | | - | 50 | - | 30 | ns |
| SIN→SCK↑ setup time | $t_{IVSHE}$ | SCKx, SINx | | 10 | - | 10 | - | ns |
| SCK↑→SIN hold time | $t_{SHIXE}$ | SCKx, SINx | | 20 | - | 20 | - | ns |
| SCK falling time | tF | SCKx | | - | 5 | - | 5 | ns |
| SCK rising time | tR | SCKx | | - | 5 | - | 5 | ns |

***Notes:***

- *The above characteristics apply to CLK synchronous mode.*
- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
  *For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance $C_L$ = 30 pF.*

### High-speed Synchronous Serial (SPI = 0, SCINV = 0)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin Name | Conditions | $V_{CC}$ < 4.5V | | $V_{CC}$ ≥ 4.5V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCKx | Internal shift clock operation | $4t_{CYCP}$ | - | $4t_{CYCP}$ | - | ns |
| SCK↓→SOT delay time | $t_{SLOVI}$ | SCKx, SOTx | | -10 | +10 | -10 | +10 | ns |
| SIN→SCK↑ setup time | $t_{IVSHI}$ | SCKx, SINx | | 14<br>12.5* | - | 12.5 | - | ns |
| SCK↑→SIN hold time | $t_{SHIXI}$ | SCKx, SINx | | 5 | - | 5 | - | ns |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCKx | External shift clock operation | $2t_{CYCP}$ – 5 | - | $2t_{CYCP}$ – 5 | - | ns |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCKx | | $t_{CYCP}$ + 10 | - | $t_{CYCP}$ + 10 | - | ns |
| SCK↓→SOT delay time | $t_{SLOVE}$ | SCKx, SOTx | | - | 15 | - | 15 | ns |
| SIN→SCK↑ setup time | $t_{IVSHE}$ | SCKx, SINx | | 5 | - | 5 | - | ns |
| SCK↑→SIN hold time | $t_{SHIXE}$ | SCKx,<br>SINx | | 5 | - | 5 | - | ns |
| SCK falling time | tF | SCKx | | - | 5 | - | 5 | ns |
| SCK rising time | tR | SCKx | | - | 5 | - | 5 | ns |

***Notes:***

- *The above characteristics apply to CLK synchronous mode.*
- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.*
- *These characteristics only guarantee the following pins.*
  - *No chip select: SIN0_1, SOT0_1, SCK0_1*
  - *Chip select: SIN6_0, SOT6_0, SCK6_0, SCS6_0*
- *When the external load capacitance $C_L$ = 30 pF. (For *, when $C_L$ = 10 pF)*

### When Using High-speed Synchronous Serial Chip Select (SPI = 1, SCINV = 0, MS=0, CSLVL=1)

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Conditions | $V_{CC}$ < 4.5 V | | $V_{CC}$ ≥ 4.5 V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| SCS↓→SCK↓setup time | $t_{CSSI}$ | Internal shift clock operation | (*1)-20 | (*1)+0 | (*1)-20 | (*1)+0 | ns |
| SCK↑→SCS↑ hold time | $t_{CSHI}$ | | (*2)+0 | (*2)+20 | (*2)+0 | (*2)+20 | ns |
| SCS deselect time | $t_{CSDI}$ | | (*3)-20+5$t_{CYCP}$ | (*3)+20+5$t_{CYCP}$ | (*3)-20+5$t_{CYCP}$ | (*3)+20+5$t_{CYCP}$ | ns |
| SCS↓→SCK↓setup time | $t_{CSSE}$ | External shift clock operation | 3$t_{CYCP}$+15 | - | 3$t_{CYCP}$+15 | - | ns |
| SCK↑→SCS↑ hold time | $t_{CSHE}$ | | 0 | - | 0 | - | ns |
| SCS deselect time | $t_{CSDE}$ | | 3$t_{CYCP}$+15 | - | 3$t_{CYCP}$+15 | - | ns |
| SCS↓→SOT delay time | $t_{DSE}$ | | - | 25 | - | 25 | ns |
| SCS↑→SOT delay time | $t_{DEE}$ | | 0 | - | 0 | - | ns |

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

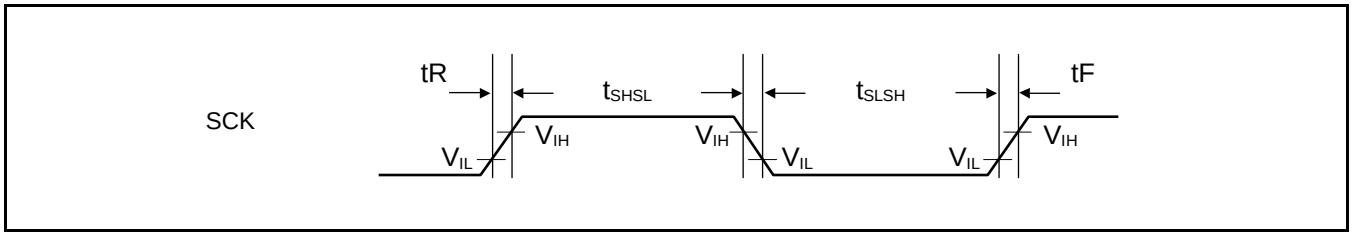
***Notes:***

- *$t_{CYCP}$ indicates the APB bus clock cycle time.*
  *About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.*
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual.*
- *When the external load capacitance $C_L$ = 30 pF.*

### External Clock (EXT = 1): when in Asynchronous Mode Only

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Serial clock "L" pulse width | $t_{SLSH}$ | $C_L$ = 30 pF | $t_{CYCP}$ + 10 | - | ns | |
| Serial clock "H" pulse width | $t_{SHSL}$ | | $t_{CYCP}$ + 10 | - | ns | |
| SCK falling time | tF | | - | 5 | ns | |
| SCK rising time | tR | | - | 5 | ns | |



### 12.4.14 $I^2C$ Timing

#### Typical Mode, High-speed Mode

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Conditions | Typical Mode | | High-speed Mode | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | | |
| SCL clock frequency | $F_{SCL}$ | $C_L$ = 30 pF, $R = (Vp/I_{OL})$*1 | 0 | 100 | 0 | 400 | kHz | |
| (Repeated) START condition hold time SDA ↓ → SCL ↓ | $t_{HDSTA}$ | | 4.0 | - | 0.6 | - | µs | |
| SCL clock "L" width | $t_{LOW}$ | | 4.7 | - | 1.3 | - | µs | |
| SCL clock "H" width | $t_{HIGH}$ | | 4.0 | - | 0.6 | - | µs | |
| (Repeated) START condition setup time SCL ↑ → SDA ↓ | $t_{SUSTA}$ | | 4.7 | - | 0.6 | - | µs | |
| Data hold time SCL ↓ → SDA ↓ ↑ | $t_{HDDAT}$ | | 0 | 3.45*2 | 0 | 0.9*3 | µs | |
| Data setup time SDA ↓ ↑ → SCL ↑ | $t_{SUDAT}$ | | 250 | - | 100 | - | ns | |
| STOP condition setup time SCL ↑ → SDA ↑ | $t_{SUSTO}$ | | 4.0 | - | 0.6 | - | µs | |
| Bus free time between "STOP condition" and "START condition" | $t_{BUF}$ | | 4.7 | - | 1.3 | - | µs | |
| Noise filter | $t_{SP}$ | 2 MHz ≤ $t_{CYCP}$<40 MHz | $2t_{CYCP}$*4 | - | $2t_{CYCP}$*4 | - | ns | *5 |
| | | 40 MHz ≤ $t_{CYCP}$<60 MHz | $4t_{CYCP}$*4 | - | $4t_{CYCP}$*4 | - | ns | |
| | | 60 MHz ≤ $t_{CYCP}$<80 MHz | $6t_{CYCP}$*4 | - | $6t_{CYCP}$*4 | - | ns | |
| | | 80 MHz ≤ $t_{CYCP}$<100 MHz | $8t_{CYCP}$*4 | - | $8t_{CYCP}$*4 | - | ns | |
| | | 100 MHz ≤ $t_{CYCP}$<120 MHz | $10t_{CYCP}$*4 | - | $10t_{CYCP}$*4 | - | ns | |
| | | 120 MHz ≤ $t_{CYCP}$<140 MHz | $12t_{CYCP}$*4 | - | $12t_{CYCP}$*4 | - | ns | |
| | | 140 MHz ≤ $t_{CYCP}$<160 MHz | $14t_{CYCP}$*4 | - | $14t_{CYCP}$*4 | - | ns | |
| | | 160 MHz ≤ $t_{CYCP}$<180 MHz | $16t_{CYCP}$*4 | - | $16t_{CYCP}$*4 | - | ns | |

*1: R and $C_L$ represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and $I_{OL}$ indicates $V_{OL}$ guaranteed current.

*2: The maximum $t_{HDDA}T$ must satisfy that it does not extend at least "L" period ($t_{LOW}$) of device's SCL signal.

*3: A high-speed mode $I^2C$ bus device can be used on a typical mode $I^2C$ bus system as long as the device satisfies the requirement of $t_{SUDAT}$ ≥ 250 ns.

*4: $t_{CYCP}$ is the APB bus clock cycle time.
About the APB bus number that $I^2C$ is connected to, see "8. Block Diagram" in this data sheet.

*5: The noise filter time can be changed by register settings.
Change the number of the noise filter steps according to APB bus clock frequency.

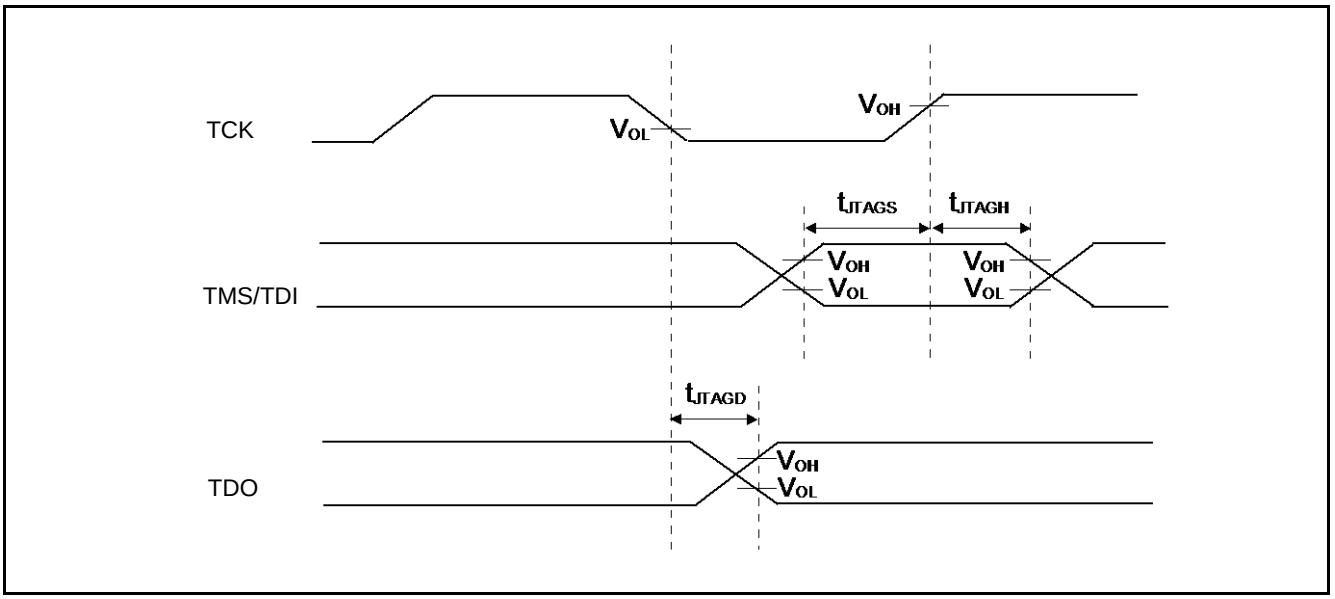
### 12.4.15 JTAG Timing

($V_{CC}$ = 2.7V to 5.5V, $V_{SS}$ = 0V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| TMS, TDI setup time | $t_{JTAGS}$ | TCK, TMS, TDI | $V_{CC} \geq 4.5$ V | 15 | - | ns | |
| | | | $V_{CC} < 4.5$ V | | | | |
| TMS, TDI hold time | $t_{JTAGH}$ | TCK, TMS, TDI | $V_{CC} \geq 4.5$ V | 15 | - | ns | |
| | | | $V_{CC} < 4.5$ V | | | | |
| TDO delay time | $t_{JTAGD}$ | TCK, TDO | $V_{CC} \geq 4.5$ V | - | 25 | ns | |
| | | | $V_{CC} < 4.5$ V | - | 45 | | |

***Note:***

- *When the external load capacitance $C_L$= 30 pF.*



## 12.8 Low-Voltage Detection Characteristics

### *12.8.1 Low-Voltage Detection Reset*

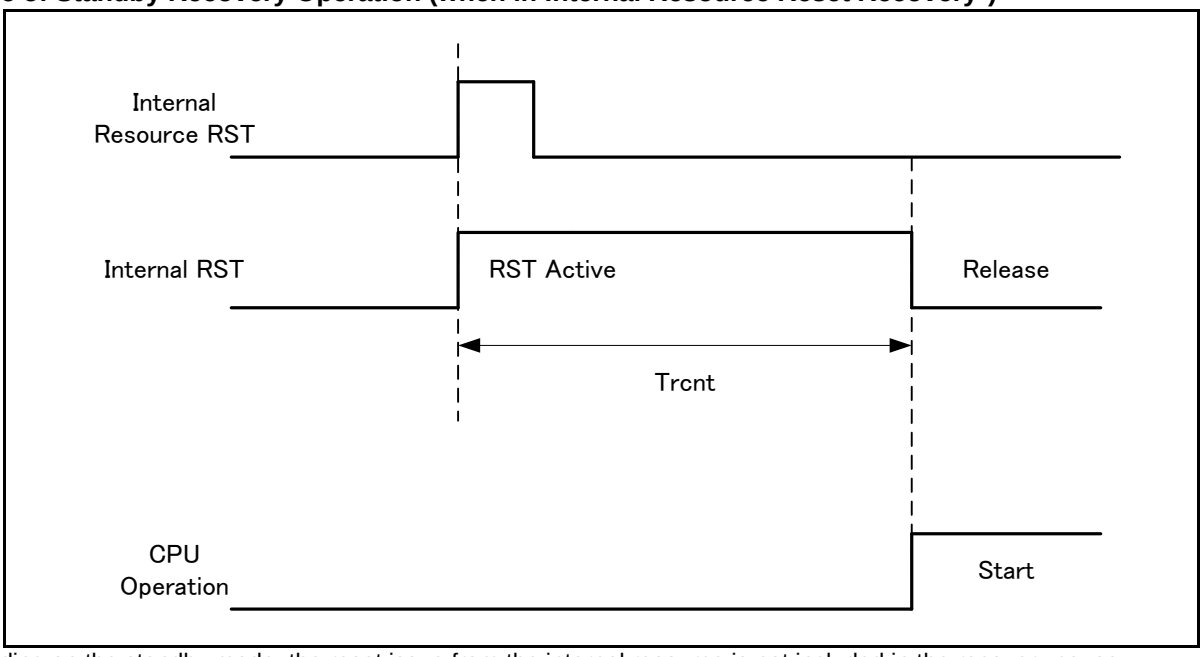
| Parameter | Symbol | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Detected voltage | VDL | - | 2.25 | 2.45 | 2.65 | V | When voltage drops |
| Released voltage | VDH | - | 2.30 | 2.50 | 2.70 | V | When voltage rises |

### *12.8.2 Interrupt of Low-Voltage Detection*

| Parameter | Symbol | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Detected voltage | VDL | SVHI = 00111 | 2.58 | 2.8 | 3.02 | V | When voltage drops |
| Released voltage | VDH | | 2.67 | 2.9 | 3.13 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 00100 | 2.76 | 3.0 | 3.24 | V | When voltage drops |
| Released voltage | VDH | | 2.85 | 3.1 | 3.34 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 01100 | 2.94 | 3.2 | 3.45 | V | When voltage drops |
| Released voltage | VDH | | 3.04 | 3.3 | 3.56 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 01111 | 3.31 | 3.6 | 3.88 | V | When voltage drops |
| Released voltage | VDH | | 3.40 | 3.7 | 3.99 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 01110 | 3.40 | 3.7 | 3.99 | V | When voltage drops |
| Released voltage | VDH | | 3.50 | 3.8 | 4.10 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 01001 | 3.68 | 4.0 | 4.32 | V | When voltage drops |
| Released voltage | VDH | | 3.77 | 4.1 | 4.42 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 01000 | 3.77 | 4.1 | 4.42 | V | When voltage drops |
| Released voltage | VDH | | 3.86 | 4.2 | 4.53 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 11000 | 3.86 | 4.2 | 4.53 | V | When voltage drops |
| Released voltage | VDH | | 3.96 | 4.3 | 4.64 | V | When voltage rises |
| LVD stabilization wait time | $T_{LVDW}$ | - | - | - | 4480× $t_{CYCP}$* | µs | |

*: $t_{CYCP}$ indicates the APB2 bus clock cycle time.

**Example of Standby Recovery Operation (when in Internal Resource Reset Recovery*)**

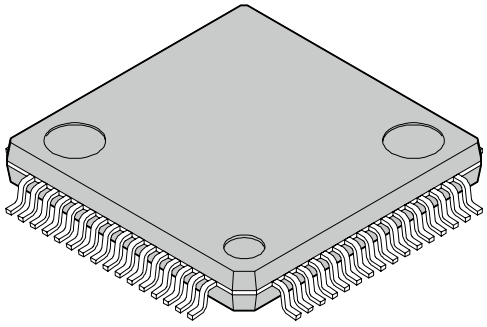



*: Depending on the standby mode, the reset issue from the internal resource is not included in the recovery cause.

***Notes:***

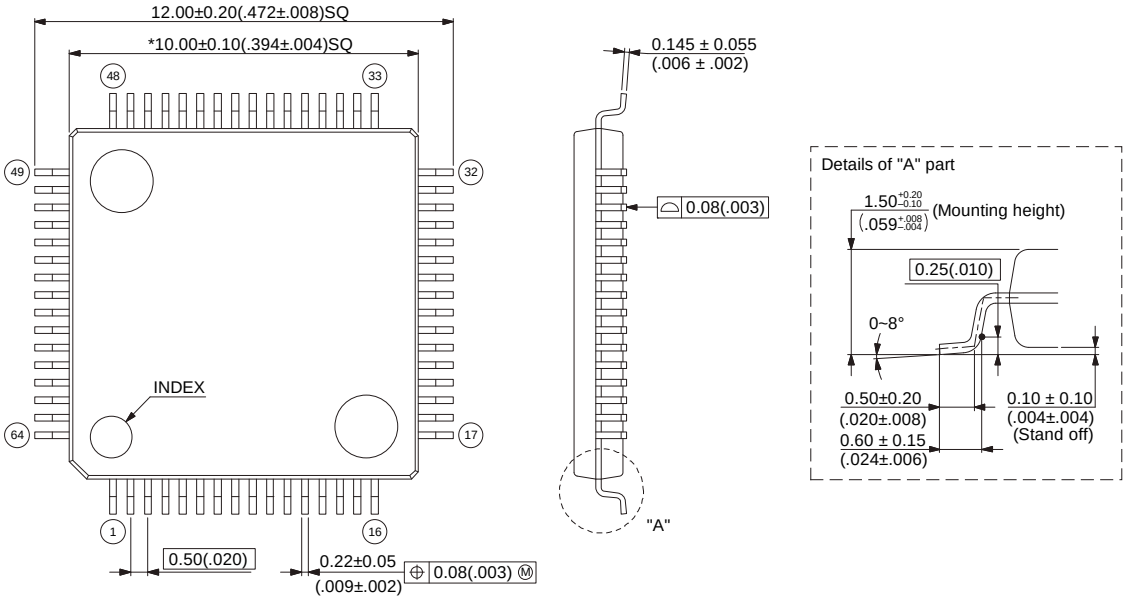
- *The return factor is different in each Low-Power consumption modes.*
  *See CHAPTER 6: Low Power Consumption Mode and Operations of Standby Modes in FM4 Family Peripheral Manual Main part (002-04856).*
- *The time during the power-on reset/low-voltage detection reset is excluded to the recovery source. See (6) Power-on Reset Timing in 12.4 AC Characteristics in 12. Electrical Characteristics for the detail on the time during the power-on reset/low-voltage detection reset.*
- *When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*

## 14. Package Dimensions

| 64-pin plastic LQFP | | |
|---|---|---|
|  (FPT-64P-M38) | Lead pitch | 0.50 mm |
| | Package width × package length | 10.00 mm × 10.00 mm |
| | Lead shape | Gullwing |
| | Lead bend direction | Normal bend |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.32 g |

64-pin plastic LQFP
(FPT-64P-M38)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.






Dimensions in mm (inches).
Note: The values in parentheses are reference values.