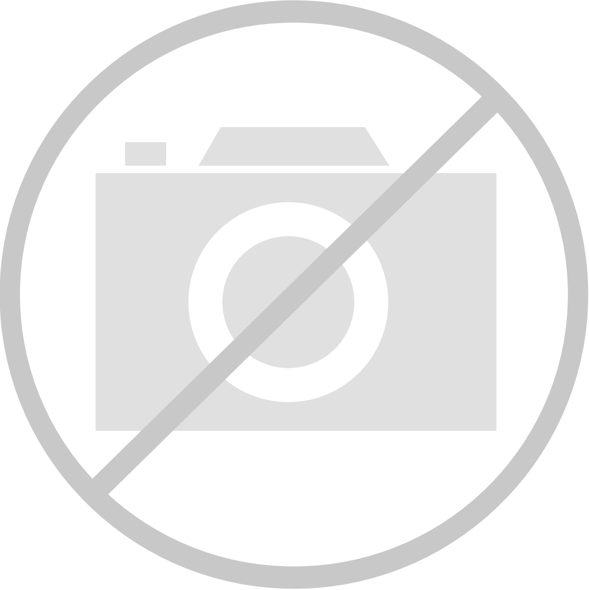
NXP Semiconductors - S912ZVHL64F1VLQ Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HCS12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	5.5V ~ 18V
Data Converters	A/D 8x10b SAR
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvhl64f1vlq

Chapter 19
Simple Sound Generator (SSGV1)

Chapter 20
ECC Generation module (SRAM_ECCV1)

1.7.2.32.3 API_EXTCLK

This signal is associated with the output of the API.

1.7.2.32.4 ECLK

This signal is associated with the output of the divided bus clock (ECLK).

NOTE

This feature is only intended for debug purposes at room temperature. It must not be used for clocking external devices in an application.

1.7.2.33 BDC and Debug Signals

1.7.2.33.1 BKGD — Background Debug signal

The BKGD signal is used as a pseudo-open-drain signal for the background debug communication. The BKGD signal has an internal pull-up device.

1.7.2.33.2 PDO — Profiling Data Output

This is the profiling data output signal used when the DBG module profiling feature is enabled. This signal is output only and provides a serial, encoded data stream that can be used by external development tools to reconstruct the internal CPUcode flow.

1.7.2.33.3 PDOCLK — Profiling Data Output Clock

This is the PDO clock signal used when the DBG module profiling feature is enabled. This signal is output only. During code profiling this is the clock signal that can be used by external development tools to sample the PDO signal.

1.7.2.33.4 DBGEEV — External Event Input

This signal is the DBG external event input. It is input only. Within the DBG module, it allows an external event to force a state sequencer transition, or trace buffer entry, or to gate trace buffer entries. A falling edge at the external event signal constitutes an event. Rising edges have no effect. The maximum frequency of events is half the internal core bus frequency.

1.7.2.34 LIN Physical Layer 0 Signals

1.7.2.34.1 LIN

This pad is connected to the single-wire LIN data bus.

1.7.2.34.2 LPTXD0

This is the LIN physical layer transmitter input signal.

Table 6-2. Glossary Of Terms

Term	Definition
BDM	Background Debug Mode. In this mode CPU application code execution is halted. Execution of BDC “active BDM” commands is possible.
BDC	Background Debug Controller
WORD	16-bit data entity
Data Line	64-bit data entity
CPU	S12Z CPU module
Trigger	A trace buffer input that triggers tracing start, end or mid point

6.1.2 Overview

The comparators monitor the bus activity of the CPU. A single comparator match or a series of matches can trigger bus tracing and/or generate breakpoints. A state sequencer determines if the correct series of matches occurs. Similarly an external event can trigger bus tracing and/or generate breakpoints.

The trace buffer is visible through a 2-byte window in the register address map and can be read out using standard 16-bit word reads.

6.1.3 Features

- Four comparators (A, B, C, and D)
  - Comparators A and C compare the full address bus and full 32-bit data bus
  - Comparators A and C feature a data bus mask register
  - Comparators B and D compare the full address bus only
  - Each comparator can be configured to monitor PC addresses or addresses of data accesses
  - Each comparator can select either read or write access cycles
  - Comparator matches can force state sequencer state transitions
- Three comparator modes
  - Simple address/data comparator match mode
  - Inside address range mode, Addmin ≤ Address ≤ Addmax
  - Outside address range match mode, Address < Addmin or Address > Addmax
- State sequencer control
  - State transitions forced by comparator matches
  - State transitions forced by software write to TRIG
  - State transitions forced by an external event
- The following types of breakpoints
  - CPU breakpoint entering active BDM on breakpoint (BDM)
  - CPU breakpoint executing SWI on breakpoint (SWI)
- Trace control

7.3.2.9 S12CPMU_UHV_V5 RTI Control Register (CPMURTI)

This register selects the time-out period for the Real Time Interrupt.

The clock source for the RTI is either IRCCLK or OSCCLK depending on the setting of the RTIOSCSEL bit. In Stop Mode with PSTP=1 (Pseudo Stop Mode) and RTIOSCSEL=1 the RTI continues to run, else the RTI counter halts in Stop Mode.

Module Base + 0x000B

	7	6	5	4	3	2	1	0
R W	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
Reset	0	0	0	0	0	0	0	0

Figure 7-12. S12CPMU_UHV_V5 RTI Control Register (CPMURTI)

Read: Anytime

Write: Anytime

NOTE

A write to this register starts the RTI time-out period. A change of the RTIOSCSEL bit (writing a different value or loosing UPOSC status) re-starts the RTI time-out period.

Table 7-11. CPMURTI Field Descriptions

Field	Description
7 RTDEC	**Decimal or Binary Divider Select Bit** — RTDEC selects decimal or binary based prescaler values. 0 Binary based divider value. See Table 7-12 1 Decimal based divider value. See Table 7-13
6–4 RTR[6:4]	**Real Time Interrupt Prescale Rate Select Bits** — These bits select the prescale rate for the RTI.See Table 7-12 and Table 7-13.
3–0 RTR[3:0]	**Real Time Interrupt Modulus Counter Select Bits** — These bits select the modulus counter target value to provide additional granularity.Table 7-12 and Table 7-13 show all possible divide values selectable by the CPMURTI register**.**

Chapter 8
Timer Module (TIM16B8CV3) Block Description

Table 8-1. Revision History

V03.00	Jan. 28, 2009		Initial version
V03.01	Aug. 26, 2009	8.1.2/8-296 8.3.2.15/8-312 8.3.2.2/8-302, 8.3.2.3/8-302, 8.3.2.4/8-303, 8.4.3/8-318	- Correct typo: TSCR ->TSCR1; - Correct typo: ECTxxx->TIMxxx - Correct reference: Figure 8-25 -> Figure 8-30 - Add description, "a counter overflow when TTOV[7] is set", to be the condition of channel 7 override event. - Phrase the description of OC7M to make it more explicit
V03.02	Apri,12,2010	8.3.2.8/8-306 8.3.2.11/8-309 8.4.3/8-318	-Add Table 8-10 -update TCRE bit description -add Figure 8-31
V03.03	Jan,14,2013		-single source generate different channel guide

8.1 Introduction

The basic scalable timer consists of a 16-bit, software-programmable counter driven by a flexible programmable prescaler.

This timer can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform. Pulse widths can vary from microseconds to many seconds.

This timer could contain up to 8 input capture/output compare channels with one pulse accumulator available only on channel 7. The input capture function is used to detect a selected transition edge and record the time. The output compare function is used for generating output signals or for timer software delays. The 16-bit pulse accumulator is used to operate as a simple event counter or a gated time accumulator. The pulse accumulator shares timer channel 7 when the channel is available and when in event mode.

A full access for the counter registers or the input capture/output compare registers should take place in one clock cycle. Accessing high byte and low byte separately for all of these registers may not yield the same result as accessing them in one word.

8.1.1 Features

The TIM16B8CV3 includes these distinctive features:

- Up to 8 channels available. (refer to device specification for exact number)
- All channels have same input capture/output compare functionality.

Write: Anytime.

Table 8-11. TCTL3/TCTL4 Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero.

Field	Description
7:0 EDGnB EDGnA	**Input Capture Edge Control** — These eight pairs of control bits configure the input capture edge detector circuits.

Table 8-12. Edge Detector Circuit Configuration

EDGnB	EDGnA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge (rising or falling)

8.3.2.10 Timer Interrupt Enable Register (TIE)

Module Base + 0x000C

	7	6	5	4	3	2	1	0
R W	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
Reset	0	0	0	0	0	0	0	0

Figure 8-18. Timer Interrupt Enable Register (TIE)

Read: Anytime

Write: Anytime.

Table 8-13. TIE Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero

Field	Description
7:0 C7I:C0I	**Input Capture/Output Compare "x" Interrupt Enable —** The bits in TIE correspond bit-for-bit with the bits in the TFLG1 status register. If cleared, the corresponding flag is disabled from causing a hardware interrupt. If set, the corresponding flag is enabled to cause a interrupt.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0006 PWMCLKAB[1]	R	PCLKAB7	PCLKAB6	PCLKAB5	PCLKAB4	PCLKAB3	PCLKAB2	PCLKAB1	PCLKAB0
	W								
0x0007 RESERVED	R	0	0	0	0	0	0	0	0
	W	▨	▨	▨	▨	▨	▨	▨	▨
0x0008 PWMSCLA	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x0009 PWMSCLB	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x000A RESERVED	R	0	0	0	0	0	0	0	0
	W	▨	▨	▨	▨	▨	▨	▨	▨
0x000B RESERVED	R	0	0	0	0	0	0	0	0
	W	▨	▨	▨	▨	▨	▨	▨	▨
0x000C PWMCNT0 (2)	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x000D PWMCNT1[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x000E PWMCNT2[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x000F PWMCNT3[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0010 PWMCNT4[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0011 PWMCNT5[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0012 PWMCNT6[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x0013 PWMCNT7[2]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0

▨ = Unimplemented or Reserved

Figure 9-2. The scalable PWM Register Summary (Sheet 2 of 4)

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0027	Reserved	R	Reserved							
		W								
0x0028	Reserved	R	Reserved						0	0
		W							▨	▨
0x0029	Reserved	R	Reserved	0	Reserved					
		W	▨	▨	▨					
0x002A- 0x003F	Reserved	R	0	0	0	0	0	0	0	0
		W	▨	▨	▨	▨	▨	▨	▨	▨

▨ = Unimplemented or Reserved

Figure 10-3. ADC12B_LBA Register Summary (Sheet 3 of 3)

Module Base + 0x000C

Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W	▨	▨	▨	▨	▨	▨	▨	▨
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 11-16. MSCAN Reserved Register

[1] Read: Always reads zero in normal system operation modes
Write: Unimplemented in normal system operation modes

NOTE

Writing to this register when in special system operating modes can alter the MSCAN functionality.

11.3.2.14 MSCAN Miscellaneous Register (CANMISC)

This register provides additional features.

Module Base + 0x000D

Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	BOHOLD
W	▨	▨	▨	▨	▨	▨	▨	
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 11-17. MSCAN Miscellaneous Register (CANMISC)

[1] Read: Anytime
Write: Anytime; write of '1' clears flag; write of '0' ignored

Table 11-20. CANMISC Register Field Descriptions

Field	Description
0 BOHOLD	**Bus-off State Hold Until User Request** — If BORM is set in MSCAN Control Register 1 (CANCTL1), this bit indicates whether the module has entered the bus-off state. Clearing this bit requests the recovery from bus-off. Refer to Section 11.5.2, "Bus-Off Recovery," for details. 0 Module is not bus-off or recovery has been requested by user in bus-off state 1 Module is bus-off and holds this state until user request

11.3.2.15 MSCAN Receive Error Counter (CANRXERR)

This register reflects the status of the MSCAN receive error counter.

Module Base + 0x00X2

	7	6	5	4	3	2	1	0
R W	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
Reset:	x	x	x	x	x	x	x	x

Figure 11-28. Identifier Register 2 (IDR2) — Extended Identifier Mapping

Table 11-28. IDR2 Register Field Descriptions — Extended

Field	Description
7-0 ID[14:7]	**Extended Format Identifier —** The identifiers consist of 29 bits (ID[28:0]) for the extended format. ID28 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number.

Module Base + 0x00X3

	7	6	5	4	3	2	1	0
R W	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
Reset:	x	x	x	x	x	x	x	x

Figure 11-29. Identifier Register 3 (IDR3) — Extended Identifier Mapping

Table 11-29. IDR3 Register Field Descriptions — Extended

Field	Description
7-1 ID[6:0]	**Extended Format Identifier —** The identifiers consist of 29 bits (ID[28:0]) for the extended format. ID28 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number.
0 RTR	**Remote Transmission Request** — This flag reflects the status of the remote transmission request bit in the CAN frame. In the case of a receive buffer, it indicates the status of the received frame and supports the transmission of an answering frame in software. In the case of a transmit buffer, this flag defines the setting of the RTR bit to be sent. 0 Data frame 1 Remote frame

Module Base + 0x00X2

	7	6	5	4	3	2	1	0
R W								
Reset:	x	x	x	x	x	x	x	x

▨ = Unused; always read ‘x’

Figure 11-32. Identifier Register 2 — Standard Mapping

Module Base + 0x00X3

	7	6	5	4	3	2	1	0
R W								
Reset:	x	x	x	x	x	x	x	x

▨ = Unused; always read ‘x’

Figure 11-33. Identifier Register 3 — Standard Mapping

11.3.3.2 Data Segment Registers (DSR0-7)

The eight data segment registers, each with bits DB[7:0], contain the data to be transmitted or received. The number of bytes to be transmitted or received is determined by the data length code in the corresponding DLR register.

Module Base + 0x00X4 to Module Base + 0x00XB

	7	6	5	4	3	2	1	0
R W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Reset:	x	x	x	x	x	x	x	x

Figure 11-34. Data Segment Registers (DSR0–DSR7) — Extended Identifier Mapping

Table 11-32. DSR0–DSR7 Register Field Descriptions

Field	Description
7-0 DB[7:0]	**Data bits 7-0**

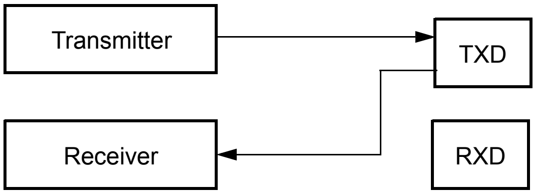

Figure 12-30. Single-Wire Operation (LOOPS = 1, RSRC = 1)

Enable single-wire operation by setting the LOOPS bit and the receiver source bit, RSRC, in SCI control register 1 (SCICR1). Setting the LOOPS bit disables the path from the RXD pin to the receiver. Setting the RSRC bit connects the TXD pin to the receiver. Both the transmitter and receiver must be enabled (TE = 1 and RE = 1).The TXDIR bit (SCISR2[1]) determines whether the TXD pin is going to be used as an input (TXDIR = 0) or an output (TXDIR = 1) in this mode of operation.

NOTE

In single-wire operation data from the TXD pin is inverted if RXPOL is set.

12.4.8 Loop Operation

In loop operation the transmitter output goes to the receiver input. The RXD pin is disconnected from the SCI.

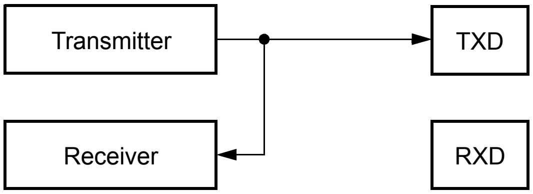

Figure 12-31. Loop Operation (LOOPS = 1, RSRC = 0)

Enable loop operation by setting the LOOPS bit and clearing the RSRC bit in SCI control register 1 (SCICR1). Setting the LOOPS bit disables the path from the RXD pin to the receiver. Clearing the RSRC bit connects the transmitter output to the receiver input. Both the transmitter and receiver must be enabled (TE = 1 and RE = 1).

NOTE

In loop operation data from the transmitter is not recognized by the receiver if RXPOL and TXPOL are not the same.

12.5 Initialization/Application Information

12.5.1 Reset Initialization

See Section 12.3.2, “Register Descriptions”.

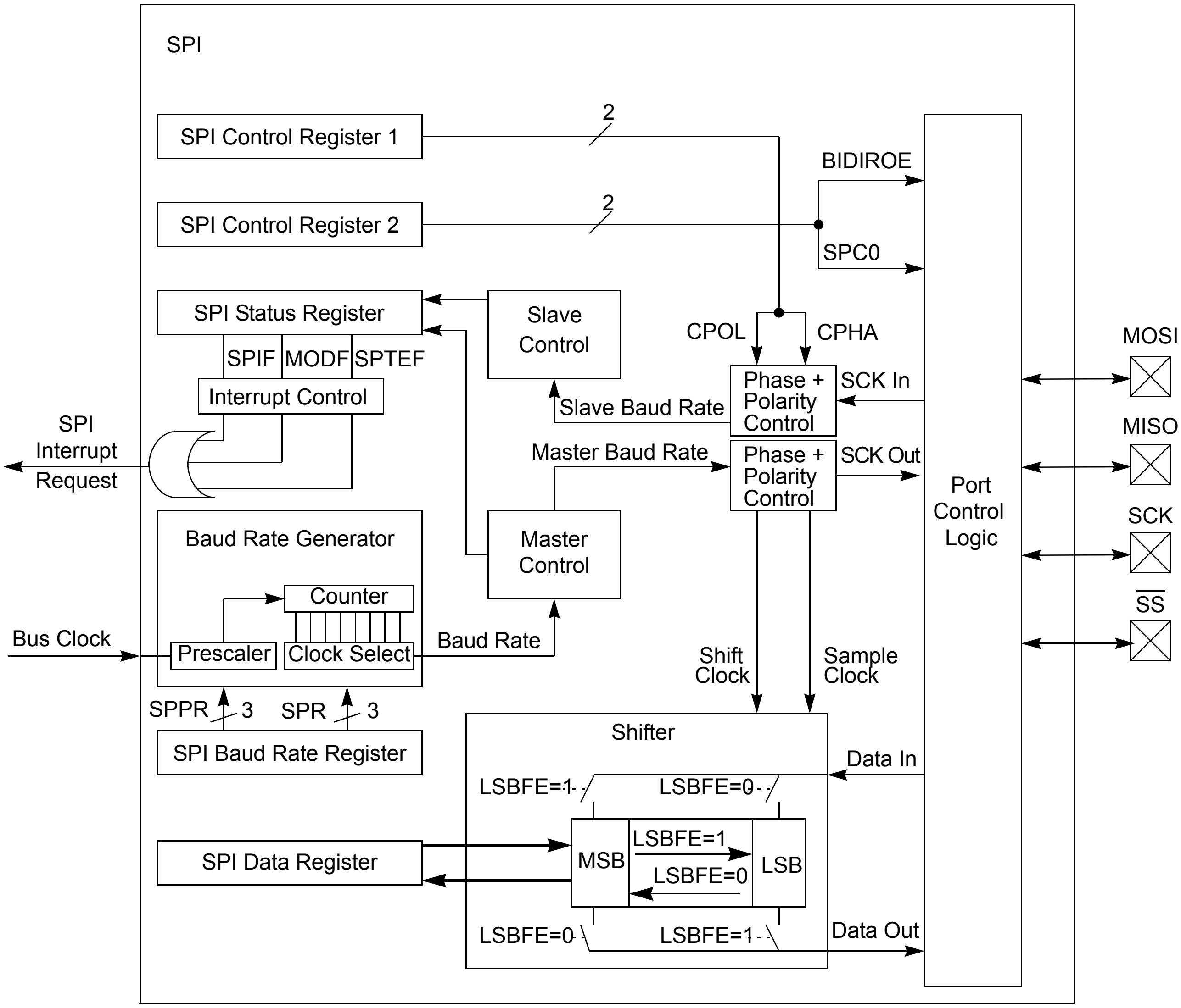

Figure 13-1. SPI Block Diagram

13.2 External Signal Description

This section lists the name and description of all ports including inputs and outputs that do, or may, connect off chip. The SPI module has a total of four external pins.

13.2.1 MOSI — Master Out/Slave In Pin

This pin is used to transmit data out of the SPI module when it is configured as a master and receive data when it is configured as slave.

13.2.2 MISO — Master In/Slave Out Pin

This pin is used to transmit data out of the SPI module when it is configured as a slave and receive data when it is configured as master.

The CPOL clock polarity control bit specifies an active high or low clock and has no significant effect on the transmission format.

The CPHA clock phase control bit selects one of two fundamentally different transmission formats.

Clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transmissions to allow a master device to communicate with peripheral slaves having different requirements.

13.4.3.2 CPHA = 0 Transfer Format

The first edge on the SCK line is used to clock the first data bit of the slave into the master and the first data bit of the master into the slave. In some peripherals, the first bit of the slave's data is available at the slave's data out pin as soon as the slave is selected. In this format, the first SCK edge is issued a half cycle after $\overline{\text{SS}}$ has become low.

A half SCK cycle later, the second edge appears on the SCK line. When this second edge occurs, the value previously latched from the serial data input pin is shifted into the LSB or MSB of the shift register, depending on LSBFE bit.

After this second edge, the next bit of the SPI master data is transmitted out of the serial data output pin of the master to the serial input pin on the slave. This process continues for a total of 16 edges on the SCK line, with data being latched on odd numbered edges and shifted on even numbered edges.

Data reception is double buffered. Data is shifted serially into the SPI shift register during the transfer and is transferred to the parallel SPI data register after the last bit is shifted in.

After 2n[1] (last) SCK edges:

- Data that was previously in the master SPI data register should now be in the slave data register and the data that was in the slave data register should be in the master.
- The SPIF flag in the SPI status register is set, indicating that the transfer is complete.

Figure 13-12 is a timing diagram of an SPI transfer where CPHA = 0. SCK waveforms are shown for CPOL = 0 and CPOL = 1. The diagram may be interpreted as a master or slave timing diagram because the SCK, MISO, and MOSI pins are connected directly between the master and the slave. The MISO signal is the output from the slave and the MOSI signal is the output from the master. The $\overline{\text{SS}}$ pin of the master must be either high or reconfigured as a general-purpose output not affecting the SPI.

[1] n depends on the selected transfer width, please refer to Section 13.3.2.2, "SPI Control Register 2 (SPICR2)

NOTE

Care must be taken when expecting data from a master while the slave is in wait or stop mode. Even though the shift register will continue to operate, the rest of the SPI is shut down (i.e., a SPIF interrupt will **not** be generated until exiting stop or wait mode). Also, the byte from the shift register will not be copied into the SPIDR register until after the slave SPI has exited wait or stop mode. In slave mode, a received byte pending in the receive shift register will be lost when entering wait or stop mode. An SPIF flag and SPIDR copy is generated only if wait mode is entered or exited during a tranmission. If the slave enters wait mode in idle mode and exits wait mode in idle mode, neither a SPIF nor a SPIDR copy will occur.

13.4.7.3 SPI in Stop Mode

Stop mode is dependent on the system. The SPI enters stop mode when the module clock is disabled (held high or low). If the SPI is in master mode and exchanging data when the CPU enters stop mode, the transmission is frozen until the CPU exits stop mode. After stop, data to and from the external SPI is exchanged correctly. In slave mode, the SPI will stay synchronized with the master.

The stop mode is not dependent on the SPISWAI bit.

13.4.7.4 Reset

The reset values of registers and signals are described in Section 13.3, “Memory Map and Register Definition”, which details the registers and their bit fields.

- If a data transmission occurs in slave mode after reset without a write to SPIDR, it will transmit garbage, or the data last received from the master before the reset.
- Reading from the SPIDR after reset will always read zeros.

13.4.7.5 Interrupts

The SPI only originates interrupt requests when SPI is enabled (SPE bit in SPICR1 set). The following is a description of how the SPI makes a request and how the MCU should acknowledge that request. The interrupt vector offset and interrupt priority are chip dependent.

The interrupt flags MODF, SPIF, and SPTEF are logically ORed to generate an interrupt request.

13.4.7.5.1 MODF

MODF occurs when the master detects an error on the $\overline{\text{SS}}$ pin. The master SPI must be configured for the MODF feature (see Table 13-3). After MODF is set, the current transfer is aborted and the following bit is changed:

- MSTR = 0, The master bit in SPICR1 resets.

The MODF interrupt is reflected in the status register MODF flag. Clearing the flag will also clear the interrupt. This interrupt will stay active while the MODF flag is set. MODF has an automatic clearing process which is described in Section 13.3.2.4, “SPI Status Register (SPISR)”.

Table 15-6. LCDFPENR0–LCDFPENR4 Field Descriptions

Field	Description
39:0 FP[39:0]EN	**Frontplane Output Enable** — The FP[39:0]EN bit enables the frontplane driver outputs. If LCDEN = 0, these bits have no effect on the state of the I/O pins. It is recommended to set FP[39:0]EN bits before LCDEN is set. 0 Frontplane driver output disabled on FP[39:0]. 1 Frontplane driver output enabled on FP[39:0].

15.3.2.4 LCD RAM (LCDRAM)

The LCD RAM consists of 20 bytes. After reset the LCD RAM contents will be zero, as indicated by Figure 15-10.

		7	6	5	4	3	2	1	0
0x0008 LCDRAM	R W	FP1BP3	FP1BP2	FP1BP1	FP1BP0	FP0BP3	FP0BP2	FP0BP1	FP0BP0
	Reset	0	0	0	0	0	0	0	0
0x0009 LCDRAM	R W	FP3BP3	FP3BP2	FP3BP1	FP3BP0	FP2BP3	FP2BP2	FP2BP1	FP2BP0
	Reset	0	0	0	0	0	0	0	0
0x000A LCDRAM	R W	FP5BP3	FP5BP2	FP5BP1	FP5BP0	FP4BP3	FP4BP2	FP4BP1	FP4BP0
	Reset	0	0	0	0	0	0	0	0
0x000B LCDRAM	R W	FP7BP3	FP7BP2	FP7BP1	FP7BP0	FP6BP3	FP6BP2	FP6BP1	FP6BP0
	Reset	0	0	0	0	0	0	0	0
0x000C LCDRAM	R W	FP9BP3	FP9BP2	FP9BP1	FP9BP0	FP8BP3	FP8BP2	FP8BP1	FP8BP0
	Reset	0	0	0	0	0	0	0	0
0x000D LCDRAM	R W	FP11BP3	FP11BP2	FP11BP1	FP11BP0	FP10BP3	FP10BP2	FP10BP1	FP10BP0
	Reset	0	0	0	0	0	0	0	0
0x000E LCDRAM	R W	FP13BP3	FP13BP2	FP13BP1	FP13BP0	FP12BP3	FP12BP2	FP12BP1	FP12BP0
	Reset	0	0	0	0	0	0	0	0
0x000F LCDRAM	R W	FP15BP3	FP15BP2	FP15BP1	FP15BP0	FP14BP3	FP14BP2	FP14BP1	FP14BP0
	Reset	0	0	0	0	0	0	0	0
0x0010 LCDRAM	R W	FP17BP3	FP17BP2	FP17BP1	FP17BP0	FP16BP3	FP16BP2	FP16BP1	FP16BP0
	Reset	0	0	0	0	0	0	0	0

I = Value is indeterminate

Figure 15-10. LCD RAM (LCDRAM)

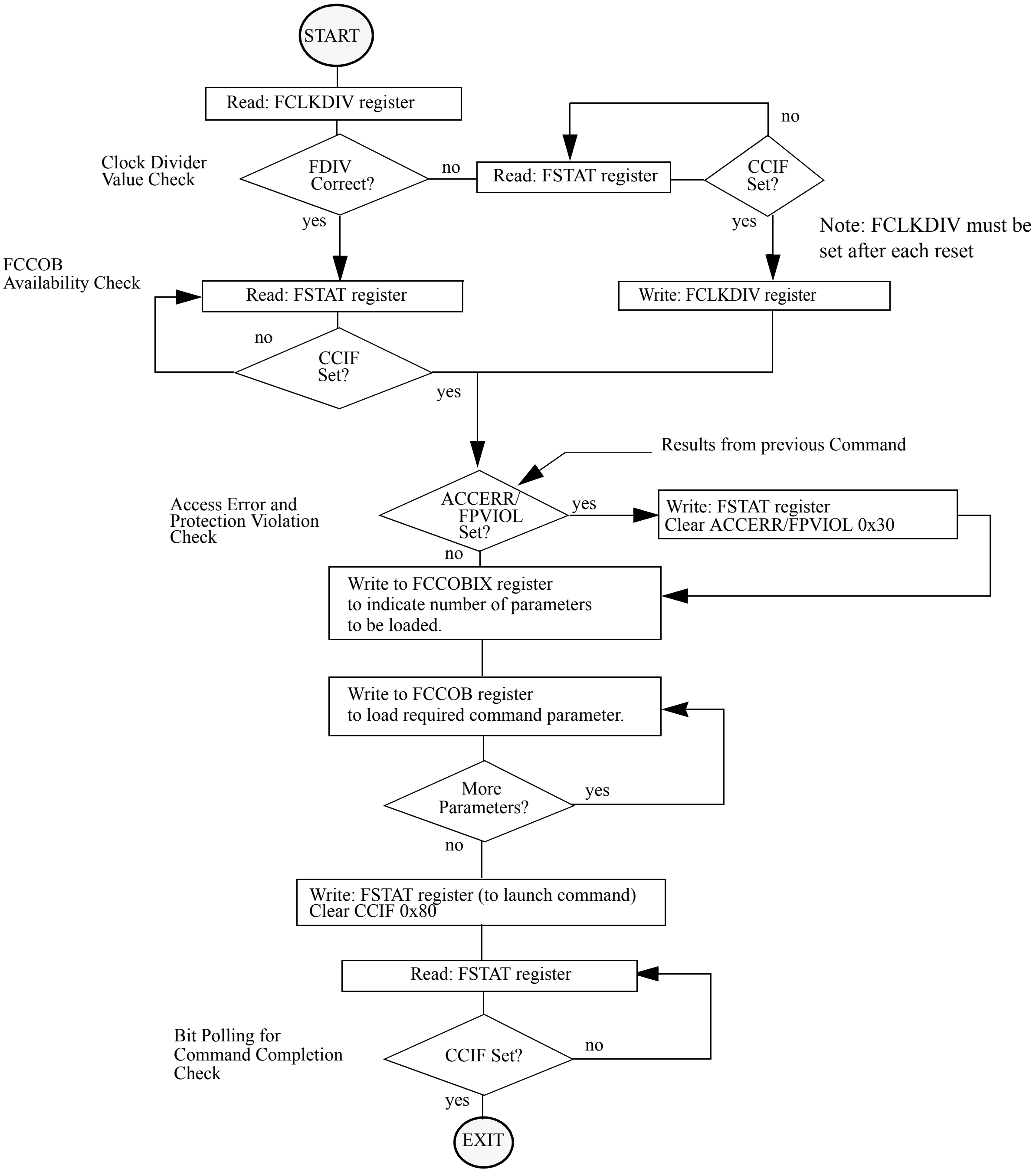

Figure 21-30. Generic Flash Command Write Sequence Flowchart

Table 21-49. Erase Flash Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 21-29)
		Set if an invalid global address [23:0] is supplied
		Set if the supplied P-Flash address is not phrase-aligned or if the EEPROM address is not word-aligned
	FPVIOL	Set if an area of the selected Flash block is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

21.4.7.9 Erase P-Flash Sector Command

The Erase P-Flash Sector operation will erase all addresses in a P-Flash sector.

Table 21-50. Erase P-Flash Sector Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x0A	Global address [23:16] to identify P-Flash block to be erased
FCCOB1	Global address [15:0] anywhere within the sector to be erased. Refer to Section 21.1.2.1 for the P-Flash sector size.	

Upon clearing CCIF to launch the Erase P-Flash Sector command, the Memory Controller will erase the selected Flash sector and then verify that it is erased. The CCIF flag will be set after the Erase P-Flash Sector operation has completed.

Table 21-51. Erase P-Flash Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 21-29)
		Set if an invalid global address [23:0] is supplied see Table 21-3)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the selected P-Flash sector is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

Table B-3. ADC Conversion Performance 5V range (-40°C < TJ < 150°C)

Num	C	Rating[1]		Symbol	Min	Typ	Max	Unit
Supply voltage 4.5V < V_{DDA} <5.5V, 4.5V < V_{REF} < 5.5V, (V_{REF} = V_{RH} - V_{RL}). f_{ADCCLK} = 8.0MHz The values are tested to be valid with no PortAD output drivers switching simultaneous with conversions.								
5	P	Resolution (V_{REF} = 5.12V)	10-Bit	LSB		5		mV
6	P	Differential Nonlinearity	10-Bit	DNL	-1	±0.5	1	counts
7	P	Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
8	P	Absolute Error[2]	10-Bit	AE	-3	±2	3	counts
9	C	Resolution (V_{REF} = 5.12V)	8-Bit	LSB		20		mV
10	C	Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
11	C	Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
12	C	Absolute Error	8-Bit	AE	-1.5	±1	1.5	counts

[1] The 8-bit mode operation is structurally tested in production test. Absolute values are tested in 10-bit mode.

[2] Absolute error includes the quantization error which is inherently 1/2 count for any A/D converter.

0x0200–0x037F Port Integration Module (PIM)

0x0266	PERE	R	0	0	0	0	PERE3	PERE2	PERE1	PERE0
		W								
0x0267	PERF	R	PERF7	PERF6	PERF5	PERF4	PERF3	PERF2	PERF1	PERF0
		W								
0x0268	PPSE	R	0	0	0	0	PPSE3	PPSE2	PPSE1	PPSE0
		W								
0x0269	PPSF	R	PPSF7	PPSF6	PPSF5	PPSF4	PPSF3	PPSF2	PPSF1	PPSF0
		W								
0x026A– 0x027F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0280	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0281	PTADL	R	PTADL7	PTADL6	PTADL5	PTADL4	PTADL3	PTADL2	PTADL1	PTADL0
		W								
0x0282	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0283	PTIADL	R	PTIADL7	PTIADL6	PTIADL5	PTIADL4	PTIADL3	PTIADL2	PTIADL1	PTIADL0
		W								
0x0284	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0285	DDRADL	R	DDRADL7	DDRADL6	DDRADL5	DDRADL4	DDRADL3	DDRADL2	DDRADL1	DDRADL0
		W								
0x0286	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0287	PERADL	R	PERADL7	PERADL6	PERADL5	PERADL4	PERADL3	PERADL2	PERADL1	PERADL0
		W								
0x0288	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0289	PPSADL	R	PPSADL7	PPSADL6	PPSADL5	PPSADL4	PPSADL3	PPSADL2	PPSADL1	PPSADL0
		W								
0x028A– 0x028B	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x028C	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x028D	PIEADL	R	PIEADL7	PIEADL6	PIEADL5	PIEADL4	PIEADL3	PIEADL2	PIEADL1	PIEADL0
		W								