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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	73
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s912zvhy64f1cll

Feature	MC9S12ZVHY64/ZVHL64		MC9S12ZVHY32/ZVHL32	
Internal 1 MHz RC oscillator	Yes		Yes	
Autonomous window watchdog	1 (with independent clock source)		1 (with independent clock source)	
Key Wakeup I/Os	19	24	19	24
General purpose I/Os (5 V)(1)	up to 73 for ZVHY up to 78 for ZVHL	up to 100	up to 73 for ZVHY up to 78 for ZVHL	up to 100
Direct Battery Voltage sense pin	Yes		Yes	
Vsup sense	Yes		Yes	
Chip temperature sensor	1 General sensor		1 General sensor	
VSUP Supply voltage	5.5 V – 18 V (normal operation) up to 40V (protected operation)		5.5 V – 18 V (normal operation) up to 40V (protected operation)	
VDDX Output current	Determined by power dissipation of external ballast		Determined by power dissipation of external ballast	
Maximum Bus Frequency	32 MHz		32 MHz	

1. Maximum I/O count based on multiplexing with peripherals.

1.3 Maskset 0N39G and 1N39G device compare

0N39G and 1N39G device module versions differ as shown in Table 1-3.

NOTE User should take care when switching from 0N39G to 1N39G device

Table 1-3. Device Difference for 0N39G and 1N39G

	0N39G	1N39G
SCI	V5	V6
BDC	V1	V2
MCU	no ADC reference voltage to IFR	ADC reference voltage to IFR

1.4 Chip-Level Features

On-chip modules available within the family include the following features:

- S12Z CPU core
- Up to 64 KB on-chip flash with ECC
- 2 KB EEPROM with ECC
- Up to 4 KB on-chip SRAM with ECC
- Phase locked loop (IPLL) frequency multiplier with internal filter

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0352	DDRU	R	DDRU7	DDRU6	DDRU5	DDRU4	DDRU3	DDRU2	DDRU1	DDRU0
		W								
0x0353	PERU	R	PERU7	PERU6	PERU5	PERU4	PERU3	PERU2	PERU1	PERU0
		W								
0x0354	PPSU	R	PPSU7	PPSU6	PPSU5	PPSU4	PPSU3	PPSU2	PPSU1	PPSU0
		W								
0x0355–0x035D	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x035E	SRRU	R	SRRU7	SRRU6	SRRU5	SRRU4	SRRU3	SRRU2	SRRU1	SRRU0
		W								
0x035F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0360–0x037F	Reserved	R	0	0	0	0	0	0	0	0
		W								

2.3.2 Register Descriptions

This section describes the details of all configuration registers.

- If not stated differently, writing to reserved bits has no effect and read returns zero.
- All register read accesses are synchronous to internal clocks.
- All registers can be written at any time, however a specific configuration might not become active. E.g. a pullup device does not become active while the port is used as a push-pull output.
- General-purpose data output availability depends on prioritization; input data registers always reflect the pin status independent of the use.
- Pull-device availability, pull-device polarity, wired-or mode, key-wake up functionality are independent of the prioritization unless noted differently.
- The description of registers PTx, PTIx, DDRx, DIENx, PERx, PPSx, SRRx, WOMx, PIEx and PIFx generically assumes a fully implemented 8-bit register. For availability of individual bits refer to Section 2.3.1, “Register Map“”.

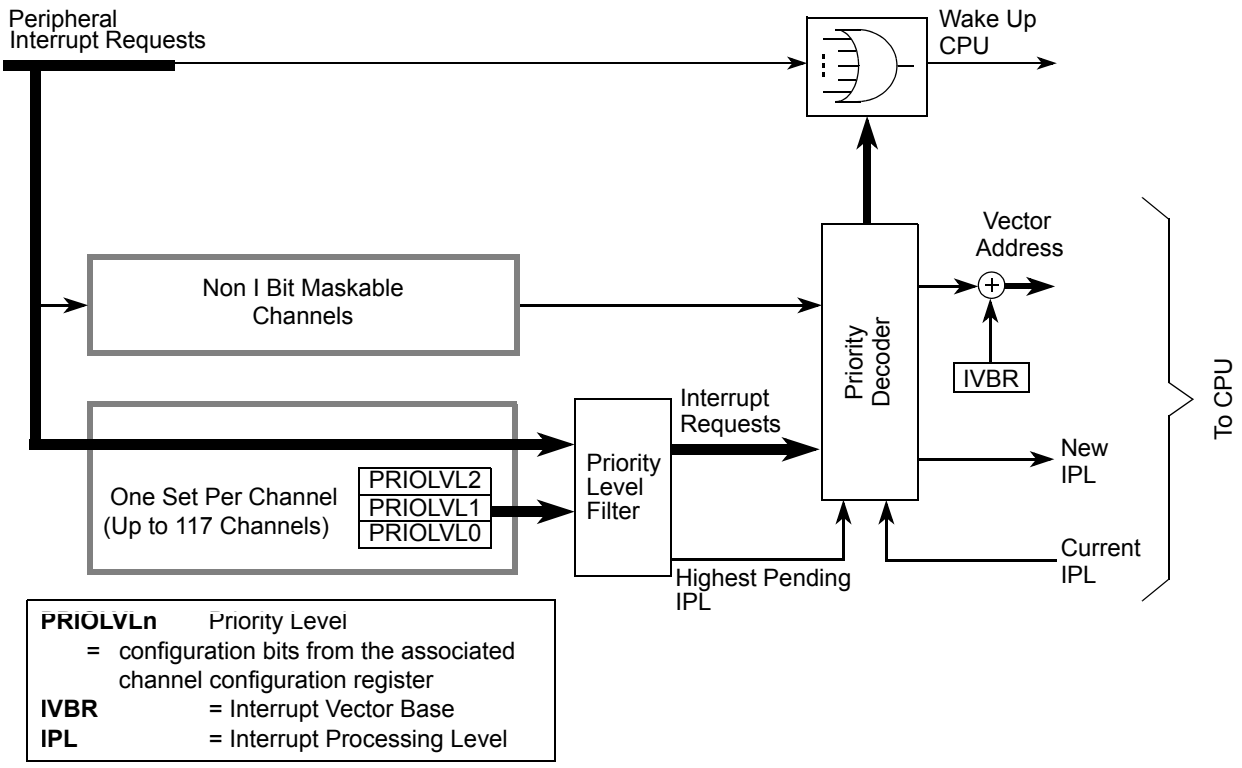


Figure 4-1. INT Block Diagram

4.2 External Signal Description

The INT module has no external signals.

4.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the INT module.

4.3.1 Module Memory Map

Table 4-3 gives an overview over all INT module registers.

Table 4-3. INT Memory Map

Address	Use	Access
0x000010–0x000011	Interrupt Vector Base Register (IVBR)	R/W
0x000012–0x000016	RESERVED	—
0x000017	Interrupt Request Configuration Address Register (INT_CFADDR)	R/W
0x000018	Interrupt Request Configuration Data Register 0 (INT_CFDATA0)	R/W

NOTE

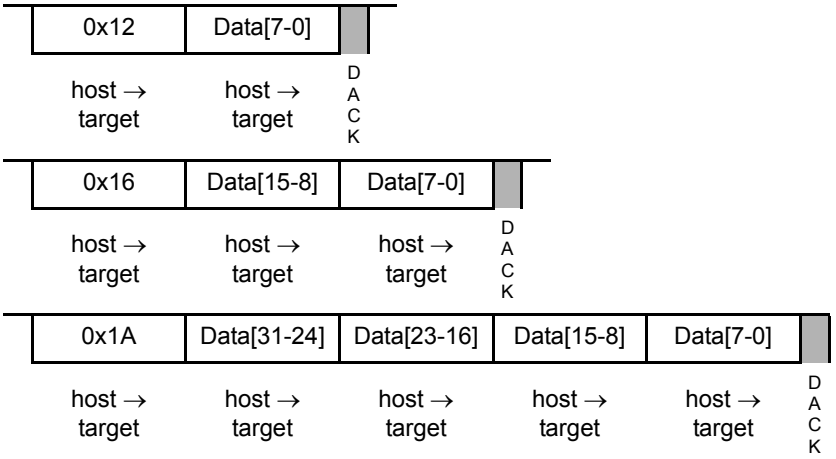
DUMP_MEM{_WS} is a valid command only when preceded by SYNC, NOP, READ_MEM{_WS}, or another DUMP_MEM{_WS} command. Otherwise, an illegal command response is returned, setting the ILLCMD bit. NOP can be used for inter-command padding without corrupting the address pointer.

The size field (sz) is examined each time a DUMP_MEM{_WS} command is processed, allowing the operand size to be dynamically altered. The examples show the DUMP_MEM.B{_WS}, DUMP_MEM.W{_WS} and DUMP_MEM.L{_WS} commands.

5.4.4.6 FILL_MEM.sz, FILL_MEM.sz_WS

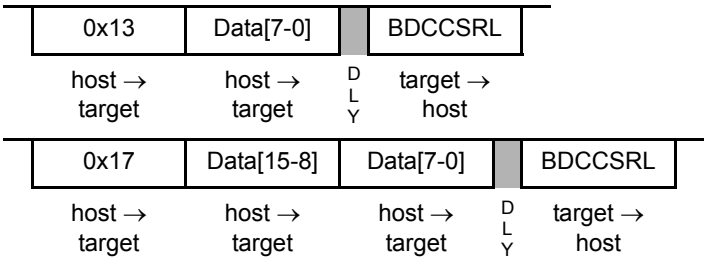
FILL_MEM.sz

Write memory specified by debug address register, then increment address — **Non-intrusive**



FILL_MEM.sz_WS

Write memory specified by debug address register with status, then increment address — **Non-intrusive**



5.4.11 Serial Communication Timeout

The host initiates a host-to-target serial transmission by generating a falling edge on the BKGD pin. If BKGD is kept low for more than 128 target clock cycles, the target understands that a SYNC command was issued. In this case, the target waits for a rising edge on BKGD in order to answer the SYNC request pulse. When the BDC detects the rising edge a soft reset is generated, whereby the current BDC command is discarded. If the rising edge is not detected, the target keeps waiting forever without any timeout limit.

If a falling edge is not detected by the target within 512 clock cycles since the last falling edge, a timeout occurs and the current command is discarded without affecting memory or the operating mode of the MCU. This is referred to as a soft-reset. This timeout also applies if 512 cycles elapse between 2 consecutive ERASE_FLASH commands. The soft reset is disabled whilst the internal flash mass erase operation is pending completion.

timeouts are also possible if a BDC command is partially issued, or data partially retrieved. Thus if a time greater than 512 BDCSI clock cycles is observed between two consecutive negative edges, a soft-reset occurs causing the partially received command or data retrieved to be discarded. The next negative edge at the BKGD pin, after a soft-reset has occurred, is considered by the target as the start of a new BDC command, or the start of a SYNC request pulse.

5.5 Application Information

5.5.1 Clock Frequency Considerations

Read commands without status and without ACK must consider the frequency relationship between BDCSI and the internal core clock. If the core clock is slow, then the internal access may not have been carried out within the standard 16 BDCSI cycle delay period (DLY). The host must then extend the DLY period or clock frequencies accordingly. Taking internal clock domain synchronizers into account, the minimum number of BDCSI periods required for the DLY is expressed by:

$$\#DLY > 3(f_{(BDCSI\ clock)} / f_{(core\ clock)}) + 4$$

and the minimum core clock frequency with respect to BDCSI clock frequency is expressed by

$$\text{Minimum } f_{(core\ clock)} = (3/(\#DLY \text{ cycles } -4))f_{(BDCSI\ clock)}$$

For the standard 16 period DLY this yields $f_{(core\ clock)} >= (1/4)f_{(BDCSI\ clock)}$

7.3.2.7 S12CPMU_UHV_V5 Clock Select Register (CPMUCLKS)

This register controls S12CPMU_UHV_V5 clock selection.

Module Base + 0x0009

	7	6	5	4	3	2	1	0
R W	PLLSEL	PSTP	CSAD	COP OSCSEL1	PRE	PCE	RTI OSCSEL	COP OSCSEL0
Reset	1	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 7-10. S12CPMU_UHV_V5 Clock Select Register (CPMUCLKS)

Read: Anytime

Write:

- Only possible if PROT=0 (CPMUPROT register) in all MCU Modes (Normal and Special Mode).
- All bits in Special Mode (if PROT=0).
- PLLSEL, PSTP, PRE, PCE, RTIOSCSEL: In Normal Mode (if PROT=0).
- CSAD: In Normal Mode (if PROT=0) until CPMUCOP write once has taken place.
- COPOSCSEL0: In Normal Mode (if PROT=0) until CPMUCOP write once has taken place. If COPOSCSEL0 was cleared by UPOSC=0 (entering Full Stop Mode with COPOSCSEL0=1 or insufficient OSCCLK quality), then COPOSCSEL0 can be set once again.
- COPOSCSEL1: In Normal Mode (if PROT=0) until CPMUCOP write once has taken place. COPOSCSEL1 will not be cleared by UPOSC=0 (entering Full Stop Mode with COPOSCSEL1=1 or insufficient OSCCLK quality if OSCCLK is used as clock source for other clock domains: for instance core clock etc.).

NOTE

After writing CPMUCLKS register, it is strongly recommended to read back CPMUCLKS register to make sure that write of PLLSEL, RTIOSCSEL and COPOSCSEL was successful. This is because under certain circumstances writes have no effect or bits are automatically changed (see CPMUCLKS register and bit descriptions).

NOTE

When using the oscillator clock as system clock (write PLLSEL = 0) it is highly recommended to enable the oscillator clock monitor reset feature (write OMRE = 1 in CPMUOSC2 register). If the oscillator monitor reset feature is disabled (OMRE = 0) and the oscillator clock is used as system clock, the system will stall in case of loss of oscillation.

Table 7-14. CPMUCOP Field Descriptions

Field	Description
7 WCOP	**Window COP Mode Bit** — When set, a write to the CPMUARMCOP register must occur in the last 25% of the selected period. A write during the first 75% of the selected period generates a COP reset. As long as all writes occur during this window, $55 can be written as often as desired. Once $AA is written after the $55, the time-out logic restarts and the user must wait until the next window before writing to CPMUARMCOP. Table 7-15 shows the duration of this window for the seven available COP rates. 0 Normal COP operation 1 Window COP operation
6 RSBCK	**COP and RTI Stop in Active BDM Mode Bit** 0 Allows the COP and RTI to keep running in Active BDM mode. 1 Stops the COP and RTI counters whenever the part is in Active BDM mode.
5 WRTMASK	**Write Mask for WCOP and CR[2:0] Bit** — This write-only bit serves as a mask for the WCOP and CR[2:0] bits while writing the CPMUCOP register. It is intended for BDM writing the RSBCK without changing the content of WCOP and CR[2:0]. 0 Write of WCOP and CR[2:0] has an effect with this write of CPMUCOP 1 Write of WCOP and CR[2:0] has no effect with this write of CPMUCOP. (Does not count for “write once”.)
2–0 CR[2:0]	**COP Watchdog Timer Rate Select** — These bits select the COP time-out rate (see Table 7-15 and Table 7-16). Writing a nonzero value to CR[2:0] enables the COP counter and starts the time-out period. A COP counter time-out causes a System Reset. This can be avoided by periodically (before time-out) initializing the COP counter via the CPMUARMCOP register. While all of the following four conditions are true the CR[2:0], WCOP bits are ignored and the COP operates at highest time-out period (2^{24} cycles) in normal COP mode (Window COP mode disabled): 1) COP is enabled (CR[2:0] is not 000) 2) BDM mode active 3) RSBCK = 0 4) Operation in Special Mode

Table 7-15. COP Watchdog Rates if COPOSCSEL1=0. (default out of reset)

CR2	CR1	CR0	COPCLK Cycles to time-out (COPCLK is either IRCCLK or OSCCLK depending on the COPOSCSEL0 bit)
0	0	0	COP disabled
0	0	1	2^{14}
0	1	0	2^{16}
0	1	1	2^{18}
1	0	0	2^{20}
1	0	1	2^{22}
1	1	0	2^{23}
1	1	1	2^{24}

Table 7-17. CPMUHTCTL Field Descriptions

Field	Description
5 VSEL	**Voltage Access Select Bit** — If set, the bandgap reference voltage V_{BG} can be accessed internally (i.e. multiplexed to an internal Analog to Digital Converter channel). If not set, the die temperature proportional voltage V_{HT} of the temperature sensor can be accessed internally. See device level specification for connectivity. For any of these access the HTE bit must be set. 0 An internal temperature proportional voltage V_{HT} can be accessed internally. 1 Bandgap reference voltage V_{BG} can be accessed internally.
3 HTE	**High Temperature Sensor/Bandgap Voltage Enable Bit** — This bit enables the high temperature sensor and bandgap voltage amplifier. 0 The temperature sensor and bandgap voltage amplifier is disabled. 1 The temperature sensor and bandgap voltage amplifier is enabled.
2 HTDS	**High Temperature Detect Status Bit** — This read-only status bit reflects the temperature status. Writes have no effect. 0 Junction Temperature is below level T_{HTID} or RPM. 1 Junction Temperature is above level T_{HTIA} and FPM.
1 HTIE	**High Temperature Interrupt Enable Bit** 0 Interrupt request is disabled. 1 Interrupt will be requested whenever HTIF is set.
0 HTIF	**High Temperature Interrupt Flag** — HTIF is set to 1 when HTDS status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (HTIE=1), HTIF causes an interrupt request. 0 No change in HTDS bit. 1 HTDS bit has changed.

NOTE

The voltage at the temperature sensor can be computed as follows:

$$V_{HT}(temp) = V_{HT(150)} - (150 - temp) * dV_{HT}$$

Figure 7-18. Voltage Access Select

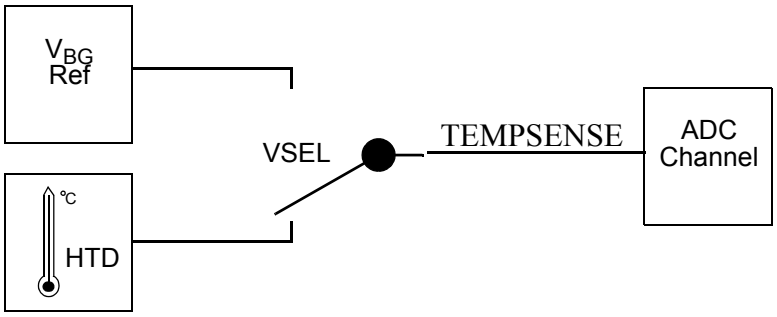


Table 8-19. Pin Action

PAMOD	PEDGE	Pin Action
0	0	Falling edge
0	1	Rising edge
1	0	Div. by 64 clock enabled with pin high level
1	1	Div. by 64 clock enabled with pin low level

NOTE

If the timer is not active (TEN = 0 in TSCR), there is no divide-by-64 because the ÷64 clock is generated by the timer prescaler.

Table 8-20. Timer Clock Selection

CLK1	CLK0	Timer Clock
0	0	Use timer prescaler clock as timer counter clock
0	1	Use PACLK as input to timer counter clock
1	0	Use PACLK/256 as timer counter clock frequency
1	1	Use PACLK/65536 as timer counter clock frequency

For the description of PACLK please refer Figure 8-30**.**

If the pulse accumulator is disabled (PAEN = 0), the prescaler clock from the timer is always used as an input clock to the timer counter. The change from one selected clock to the other happens immediately after these bits are written.

8.3.2.16 Pulse Accumulator Flag Register (PAFLG)

[1] .

Module Base + 0x0021

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PAOVF	PAIF
W								
Reset	0	0	0	0	0	0	0	0

Unimplemented or Reserved

Figure 8-25. Pulse Accumulator Flag Register (PAFLG)

Read: Anytime

Write: Anytime

When the TFFCA bit in the TSCR register is set, any access to the PACNT register will clear all the flags in the PAFLG register. Timer module or Pulse Accumulator must stay enabled (TEN=1 or PAEN=1) while clearing these bits.

10.5 Functional Description

10.5.1 Overview

The ADC12B_LBA consists of an analog sub-block and a digital sub-block. It is a successive approximation analog-to-digital converter including a sample-and-hold mechanism and an internal charge scaled C-DAC (switched capacitor scaled digital-to-analog converter) with a comparator to realize the successive approximation algorithm.

10.5.2 Analog Sub-Block

The analog sub-block contains all analog circuits (sample and hold, C-DAC, analog Comparator, and so on) required to perform a single conversion. Separate power supplies VDDA and VSSA allow noise from the MCU circuitry to be isolated from the analog sub-block for improved accuracy.

10.5.2.1 Analog Input Multiplexer

The analog input multiplexers connect one of the external or internal analog input channels to the sample and hold storage node.

10.5.2.2 Sample and Hold Machine with Sample Buffer Amplifier

The Sample and Hold Machine controls the storage and charge of the storage node (sample capacitor) to the voltage level of the analog signal at the selected ADC input channel. This architecture employs the advantage of reduced crosstalk between channels.

The sample buffer amplifier is used to raise the effective input impedance of the A/D machine, so that external components (higher bandwidth or higher impedance connected as specified) are less significant to accuracy degradation.

During the sample phase, the analog input connects first via a sample buffer amplifier with the storage node always for two ADC clock cycles (“Buffer” sample time). For the remaining sample time (“Final” sample time) the storage node is directly connected to the analog input source. Please see also Figure 10-28 for illustration and the Appendix of the device reference manual for more details.
The input analog signals are unipolar and must be within the potential range of VSSA to VDDA.
During the hold process, the analog input is disconnected from the storage node.

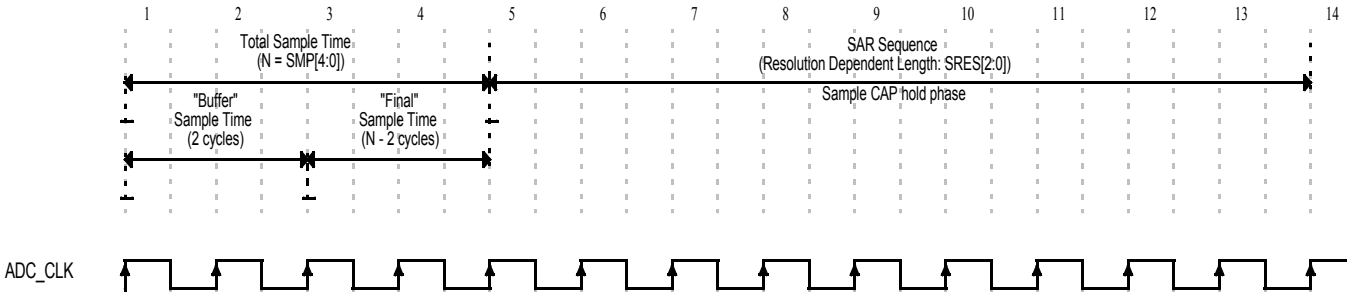


Figure 10-28. Sampling and Conversion Timing Example (8-bit Resolution, 4 Cycle Sampling)

11.2 External Signal Description

The MSCAN uses two external pins.

NOTE

On MCUs with an integrated CAN physical interface (transceiver) the MSCAN interface is connected internally to the transceiver interface. In these cases the external availability of signals TXCAN and RXCAN is optional.

11.2.1 RXCAN — CAN Receiver Input Pin

RXCAN is the MSCAN receiver input pin.

11.2.2 TXCAN — CAN Transmitter Output Pin

TXCAN is the MSCAN transmitter output pin. The TXCAN output pin represents the logic level on the CAN bus:

0 = Dominant state
1 = Recessive state

11.2.3 CAN System

A typical CAN system with MSCAN is shown in Figure 11-2. Each CAN station is connected physically to the CAN bus lines through a transceiver device. The transceiver is capable of driving the large current needed for the CAN bus and has current protection against defective CAN or defective stations.

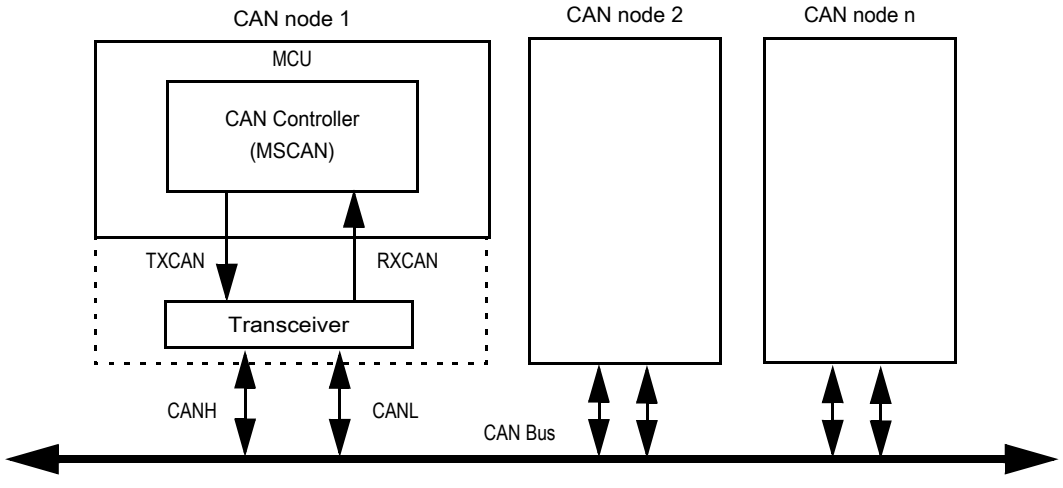


Figure 11-2. CAN System

IIC Interrupt	—	—	—	IBAL, TCF, IAAS bits in IBSR register	When either of IBAL, TCF or IAAS bits is set may cause an interrupt based on arbitration lost, transfer complete or address detect conditions

Internally there are three types of interrupts in IIC. The interrupt service routine can determine the interrupt type by reading the status register.

IIC Interrupt can be generated on

1. Arbitration lost condition (IBAL bit set)
2. Byte transfer condition (TCF bit set)
3. Address detect condition (IAAS bit set)

The IIC interrupt is enabled by the IBIE bit in the IIC control register. It must be cleared by writing 0 to the IBF bit in the interrupt service routine.

14.7 Application Information

14.7.1 IIC Programming Examples

14.7.1.1 Initialization Sequence

Reset will put the IIC bus control register to its default status. Before the interface can be used to transfer serial data, an initialization procedure must be carried out, as follows:

1. Update the frequency divider register (IBFD) and select the required division ratio to obtain SCL frequency from system clock.
2. Update the ADTYPE of IBCR2 to define the address length, 7 bits or 10 bits.
3. Update the IIC bus address register (IBAD) to define its slave address. If 10-bit address is applied IBCR2 should be updated to define the rest bits of address.
4. Set the IBEN bit of the IIC bus control register (IBCR) to enable the IIC interface system.
5. Modify the bits of the IIC bus control register (IBCR) to select master/slave mode, transmit/receive mode and interrupt enable or not.
6. If supported general call, the GCEN in IBCR2 should be asserted.

14.7.1.2 Generation of START

After completion of the initialization procedure, serial data can be transmitted by selecting the 'master transmitter' mode. If the device is connected to a multi-master bus system, the state of the IIC bus busy bit (IBB) must be tested to check whether the serial bus is free.

If the bus is free (IBB=0), the start condition and the first byte (the slave address) can be sent. The data written to the data register comprises the slave calling address and the LSB set to indicate the direction of transfer required from the slave.

The bus free time (i.e., the time between a STOP condition and the following START condition) is built into the hardware that generates the START cycle. Depending on the relative frequencies of the system

15.4.4.2 1/2 Duty Multiplexed with 1/2 Bias Mode

Duty = 1/2:DUTY1 = 1, DUTY0 = 0

Bias = 1/2:BIAS = 0

V_0 = VSSX, V_1 = V_2 = VLCD * 1/2, V_3 = VLCD

- BP2 and BP3 are not used, a maximum of 80 segments are displayed.

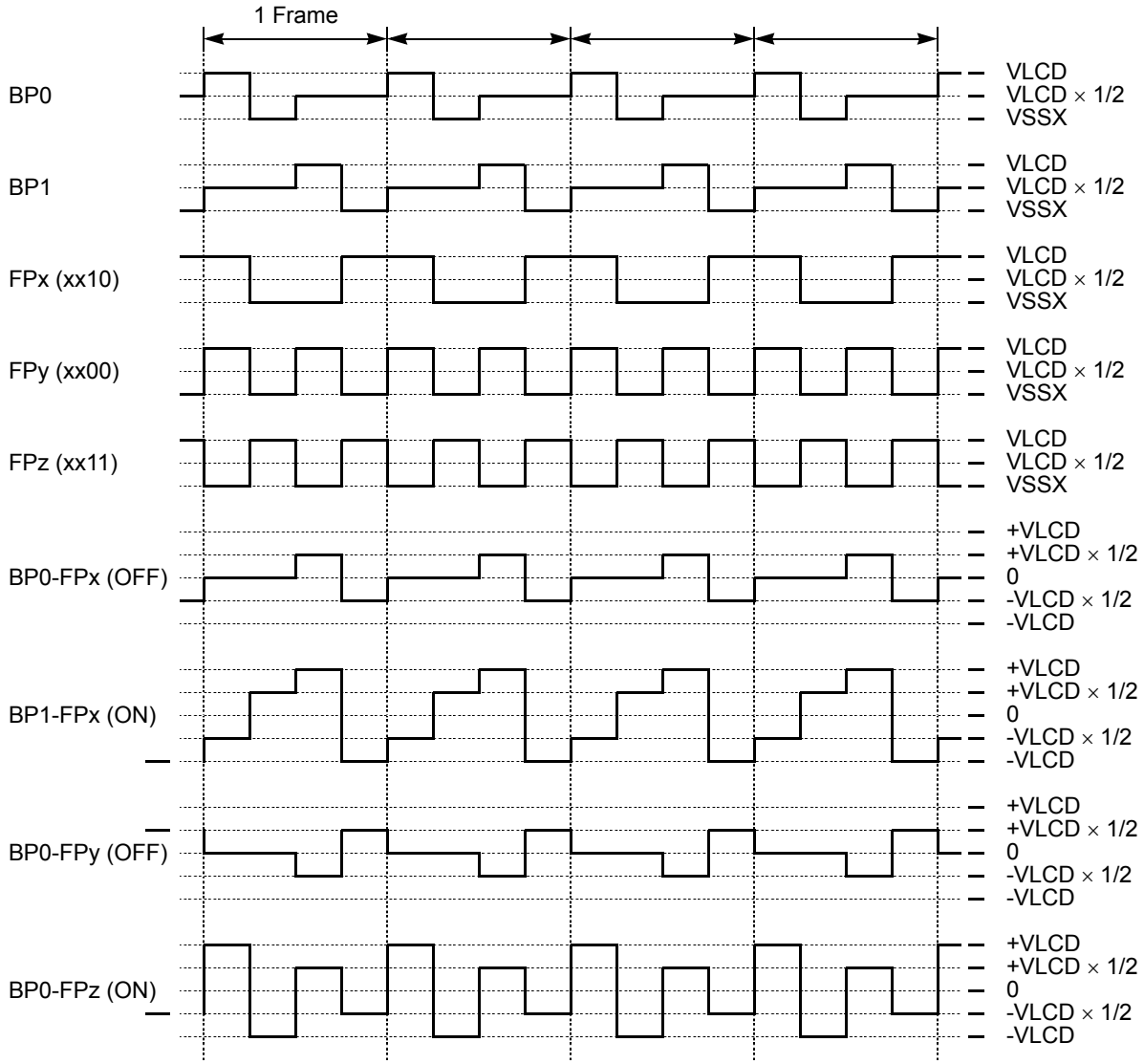


Figure 15-12. 1/2 Duty and 1/2 Bias

16.3.2.4 Motor Controller Channel Control Registers

Each PWM channel has one associated control register to control output delay, PWM alignment, and output mode. The registers are named MCCC0... MCCCn. In the following, MCCC0 is described as a reference for all other channel registers.

Offset Module Base + 0x0010 . . . 0x0017

	7	6	5	4	3	2	1	0
R	MCOM1	MCOM0	MCAM1	MCAM0	0	0	CD1	CD0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 16-7. Motor Controller Control Register Channel 0 (MCCC0)

Table 16-6. MCCC0 Field Descriptions

Field	Description
7:6 MCOM[1:0]	**Output Mode** — MCOM1, MCOM0 control the PWM channel's output mode. See Table 16-7.
5:4 MCAM[1:0]	**PWM Channel Alignment Mode** — MCAM1, MCAM0 control the PWM channel's PWM alignment mode and operation. See Table 16-8. MCAM[1:0] and MCOM[1:0] are double buffered. The values used for the generation of the output waveform will be copied to the working registers either at once (if all PWM channels are disabled or MCPER is set to 0) or if a timer counter overflow occurs. Reads of the register return the most recent written value, which are not necessarily the currently active values.
1:0 CD[1:0]	**PWM Channel Delay** — Each PWM channel can be individually delayed by a programmable number of PWM timer counter clocks. The delay will be n/f_{TC}. See Table 16-9.

Table 16-7. Output Mode

MCOM[1:0]	Output Mode
00	Half H-bridge mode, PWM on MnCxM, MnCxP is released
01	Half H-bridge mode, PWM on MnCxP, MnCxM is released
10	Full H-bridge mode
11	Dual full H-bridge mode

Table 16-8. PWM Alignment Mode

MCAM[1:0]	PWM Alignment Mode
00	Channel disabled
01	Left aligned
10	Right aligned
11	Center aligned

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0004 SSGTONEH	R	0	0	0	0	0	0	TONE9	TONE8
	W								
0x0005 SSGTONEL	R	TONE7	TONE6	TONE5	TONE4	TONE3	TONE2	TONE1	TONE0
	W								
0x0006 SSGAMPH	R	0	0	0	0	0	AMP10	AMP9	AMP8
	W								
0x0007 SSGAMPL	R	AMP7	AMP6	AMP5	AMP4	AMP3	AMP2	AMP1	AMP0
	W								
0x0008 SSGAAH	R	0	0	0	0	0	AA10	AA9	AA8
	W								
0x0009 SSGAAL	R	AA7	AA6	AA5	AA4	AA3	AA2	AA1	AA0
	W								
0x000A SSGATH	R	0	0	0	0	0	AT10	AT9	AT8
	W								
0x000B SSGATL	R	AT7	AT6	AT5	AT4	AT3	AT2	AT1	AT0
	W								
0x000C SSGDUR	R	DUR7	DUR6	DUR5	DUR4	DUR3	DUR2	DUR1	DUR0
	W								
0x000D SSGIE	R	0	0	0	0	0	0	0	RNDIE
	W								
0x000E SSGIF	R	0	0	0	0	0	0	0	RNDI
	W								
0x000F RESERVED	R	0	0	0	0	0	0	0	0
	W								
0x0010 SSGAMPBH	R	0	0	0	0	0	AMPB10	AMPB9	AMPB8
	W								
0x0011 SSGAMPBL	R	AMPB7	AMPB6	AMPB5	AMPB4	AMPB3	AMPB2	AMP1	AMPB0
	W								
0x0012 SSGDCNT	R	DCNT7	DCNT6	DCNT5	DCNT4	DCNT3	DCNT2	DCNT1	DCNT0
	W								

= Unimplemented or Reserved

Figure 19-2. The SSG Register Summary (Sheet 2 of 3)

Table 19-2. SSGCR Field Descriptions (continued)

Field	Description
1 RDR	**SSG Register Data Ready —** This bit indicates whether the registers data are ready to reload into the relative buffer registers. Writing any of SSGPS/SSGTONE/SSGAMP/SSGDUR/SSGAA/SSGAT/SSGADC will clear this bit. User should write 1 to this bit if registers setting has been done. Writing 0 to this bit will stop the SSG when the synchronous reload event occurs. 0 Register data is not ready to load into buffer register. 1 Register data is ready to load into buffer register.
0 STP	**SSG STOP** 0 SSG runs normally. 1 Immediately stop SSG.

19.3.2.2 SSG attack/decay control register (SSGADC)

SSGADC control the attack/decay enable and attack/decay function selection.

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	ADE	0	0	0	0	ADM[1:0]		ADS
W								
Reset	0	0	0	0	0	0	0	0

Figure 19-4. SSG attack/decay control register (SSGADC)

Read: Anytime

Write: Anytime

Table 19-3. SSGADC Field Descriptions

Field	Description
7 ADE	**SSG attack/decay enable** 0 SSG attack/decay function disabled. 1 SSG attack/decay function enabled.
2 - 1 ADM[1:0]	**SSG Linear, Gong or Exponential attack/decay Selection.** refer to Section 19.4.3, “SSG Attack and Decay function for detail. 00 Select linear attack/decay operation. 01 Select gong attack/decay operation. 10 Select exponential attack/decay operation. 11 Reserved.
0 ADS	**SSG Decay or attack Selection** 0 Select amplitude attack function. 1 Select amplitude decay function.

20.2.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field functions follow the register diagrams, in bit order.

20.2.2.1 ECC Status Register (ECCSTAT)

Module Base + 0x00000 — Access: User read only(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	RDY
W								
Reset	0	0	0	0	0	0	0	0

1. Read: Anytime
   Write: Never

Figure 20-2. ECC Status Register (ECCSTAT)

Table 20-2. ECCSTAT Field Description

Field	Description
0 RDY	**ECC Ready**— Shows the status of the ECC module. 0 Internal SRAM initialization is ongoing, access to the SRAM is disabled 1 Internal SRAM initialization is done, access to the SRAM is enabled

20.2.2.2 ECC Interrupt Enable Register (ECCIE)

Module Base + 0x00001 — Access: User read/write(1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	SBEEIE
W								
Reset	0	0	0	0	0	0	0	0

1. Read: Anytime
   Write: Anytime

Figure 20-3. ECC Interrupt Enable Register (ECCIE)

Table 20-3. ECCIE Field Description

Field	Description
0 SBEEIE	**Single bit ECC Error Interrupt Enable** — Enables Single ECC Error interrupt. 0 Interrupt request is disabled 1 Interrupt will be requested whenever SBEEIF is set

memory, can be activated for protection. The Flash memory addresses covered by these protectable regions are shown in the P-Flash memory map. The higher address region is mainly targeted to hold the boot loader code since it covers the vector space. Default protection settings as well as security information that allows the MCU to restrict access to the Flash module are stored in the Flash configuration field as described in Table 21-4.

Table 21-4. Flash Configuration Field

Global Address	Size (Bytes)	Description
0xFF_FE00-0xFF_FE07	8	Backdoor Comparison Key Refer to Section 21.4.7.11, “Verify Backdoor Access Key Command,” and Section 21.5.1, “Unsecuring the MCU using Backdoor Key Access”
0xFF_FE08-0xFF_FE09[1]	2	Protection Override Comparison Key. Refer to Section 21.4.7.17, “Protection Override Command”
0xFF_FE0A-0xFF_FE0B(1)	2	Reserved
0xFF_FE0C[1]	1	P-Flash Protection byte. Refer to Section 21.3.2.9, “P-Flash Protection Register (FPROT)”
0xFF_FE0D[1]	1	EEPROM Protection byte. Refer to Section 21.3.2.10, “EEPROM Protection Register (DFPROT)”
0xFF_FE0E[1]	1	Flash Nonvolatile byte Refer to Section 21.3.2.11, “Flash Option Register (FOPT)”
0xFF_FE0F[1]	1	Flash Security byte Refer to Section 21.3.2.2, “Flash Security Register (FSEC)”

1. 0xFF_FE08-0xFF_FE0F form a Flash phrase and must be programmed in a single command write sequence. Each byte in the 0xFF_FE0A - 0xFF_FE0B reserved field should be programmed to 0xFF.

comparator via an analog multiplexer. The pin itself is protected against reverse battery connections. To protect the pin from external fast transients an external resistor (R_{VSENSE_R}) is needed for protection.

22.2.2 VSUP — Voltage Supply Pin

This pin is the chip supply. It can be internally connected for voltage measurement. The voltage present at this input is scaled down by an internal voltage divider, and can be routed to the internal ADC or to a comparator via an analog multiplexer.

22.3 Memory Map and Register Definition

This section provides the detailed information of all registers for the BATS module.

22.3.1 Register Summary

Figure 22-2 shows the summary of all implemented registers inside the BATS module.

0x0480–0x04A7 Pulse-Width-Modulator (PWM)

0x0498	PWMPER4	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x0499	PWMPER5	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x049A	PWMPER6	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x049B	PWMPER7	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x049C	PWMDTY0	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x049D	PWMDTY1	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x049E	PWMDTY2	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x049F	PWMDTY3	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x04A0	PWMDTY4	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x04A1	PWMDTY5	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x04A2	PWMDTY6	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x04A3	PWMDTY7	R W	Bit 7	6	5	4	3	2	1	Bit 0
0x04A4- 0x04A7	Reserved	R W	0	0	0	0	0	0	0	0

0x04A8–0x05BF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x04A8- 0x05BF	Reserved	R W	0	0	0	0	0	0	0	0

0x05C0–0x05EF Timer Module (TIM0)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05C0	TIM0TIOS	R W	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0