Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	73
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s912zvhy64f1vll

3.1.4.2 Power modes

The S12ZMMC module is only active in run and wait mode.There is no bus activity in stop mode.

3.1.5 Block Diagram

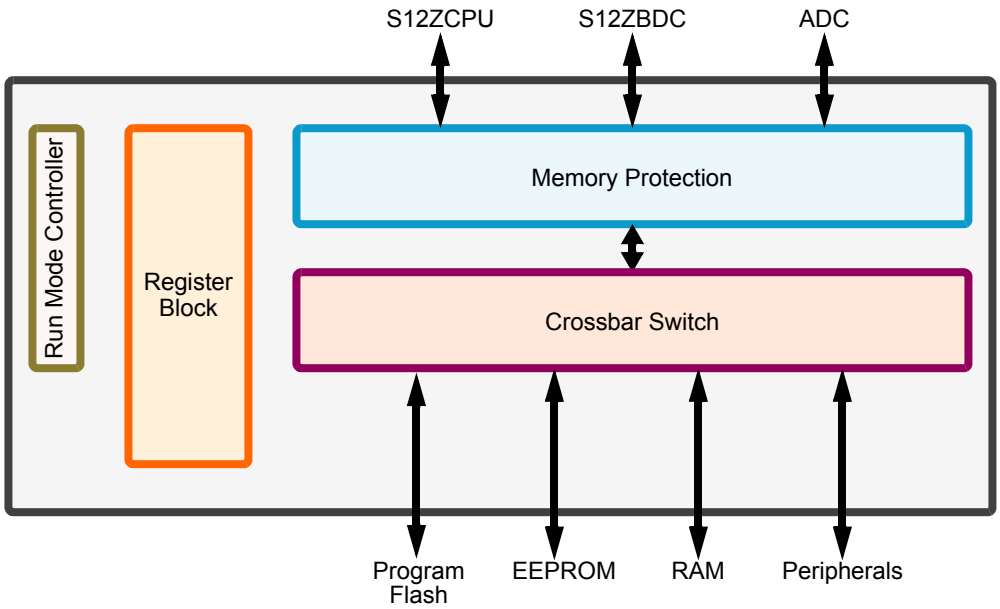


Figure 3-1. S12ZMMC Block Diagram

3.2 External Signal Description

The S12ZMMC uses two external pins to determine the devices operating mode: RESET and MODC (Table 3-3)
See device overview for the mapping of these signals to device pins.

Table 3-3. External System Pins Associated With S12ZMMC

Pin Name	Description
$\overline{\text{RESET}}$	External reset signal. The $\overline{\text{RESET}}$ signal is active low.
MODC	This input is captured in bit MODC of the MODE register when the external $\overline{\text{RESET}}$ pin deasserts.

3.3 Memory Map and Register Definition

3.3.1 Memory Map

A summary of the registers associated with the MMC block is shown in Figure 3-2. Detailed descriptions of the registers and bits are given in the subsections that follow.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0070	MODE	R	MODC	0	0	0	0	0	0	0
		W								
0x0071-0x007F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0080	MMCECH	R	ITR[3:0]				TGT[3:0]			
		W								
0x0081	MMCECL	R	ACC[3:0]				ERR[3:0]			
		W								
0x0082	MMCCCRH	R	CPUU	0	0	0	0	0	0	0
		W								
0x0083	MMCCCRL	R	0	CPUX	0	CPUI	0	0	0	0
		W								
0x0084	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0085	MMCPCH	R	CPUPC[23:16]							
		W								
0x0086	MMCPCM	R	CPUPC[15:8]							
		W								
0x0087	MMCPCL	R	CPUPC[7:0]							
		W								
0x0088-0x00FF	Reserved	R	0	0	0	0	0	0	0	0
		W								

= Unimplemented or Reserved

Figure 3-2. S12ZMMC Register Summary

3.3.2 Register Descriptions

This section consists of the S12ZMMC control and status register descriptions in address order.

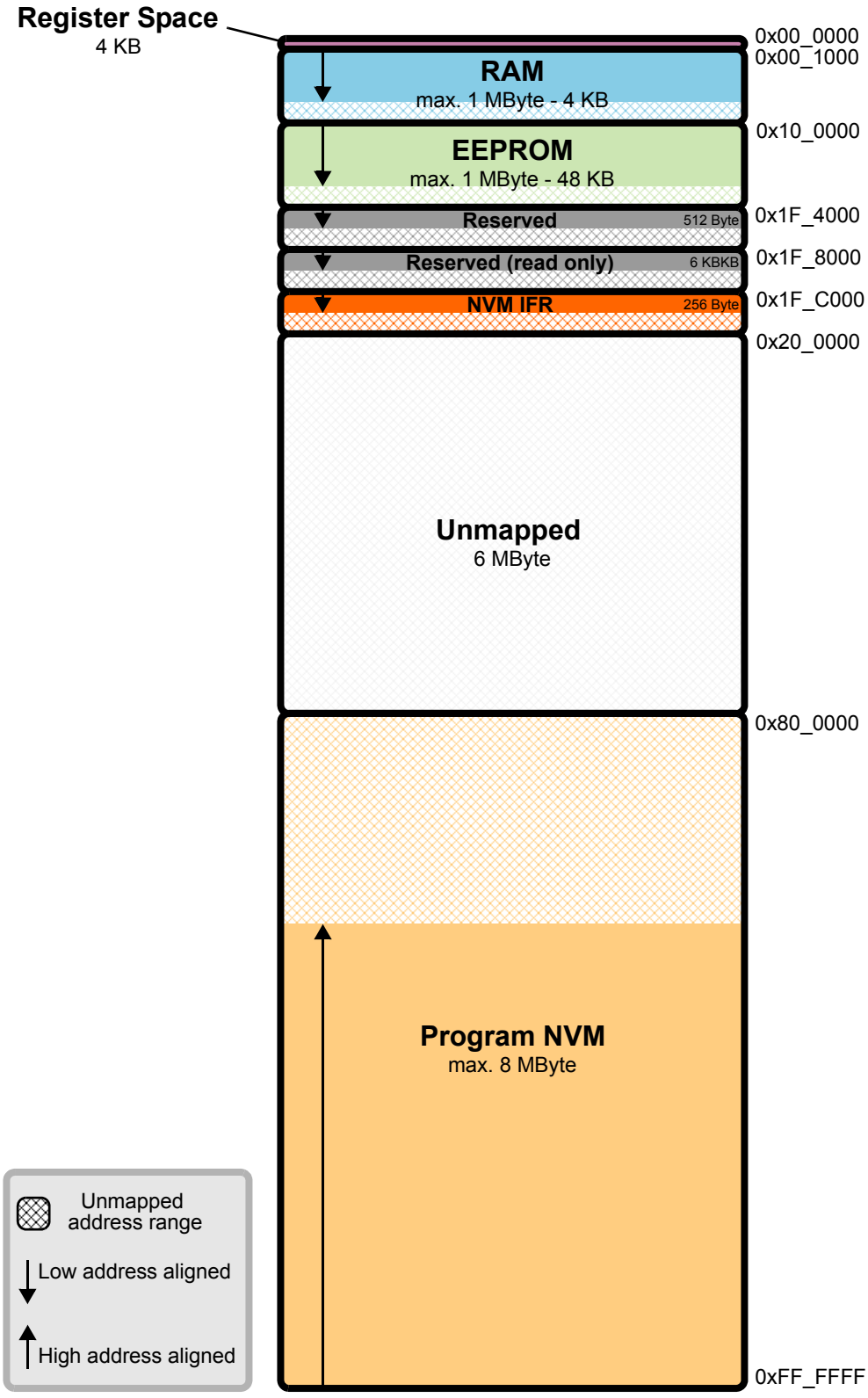


Figure 3-8. Global Memory Map

drive at the latest after 6 clock cycles, before the target drives a brief high speedup pulse seven target clock cycles after the perceived start of the bit time. The host should sample the bit level about 10 target clock cycles after it started the bit time.

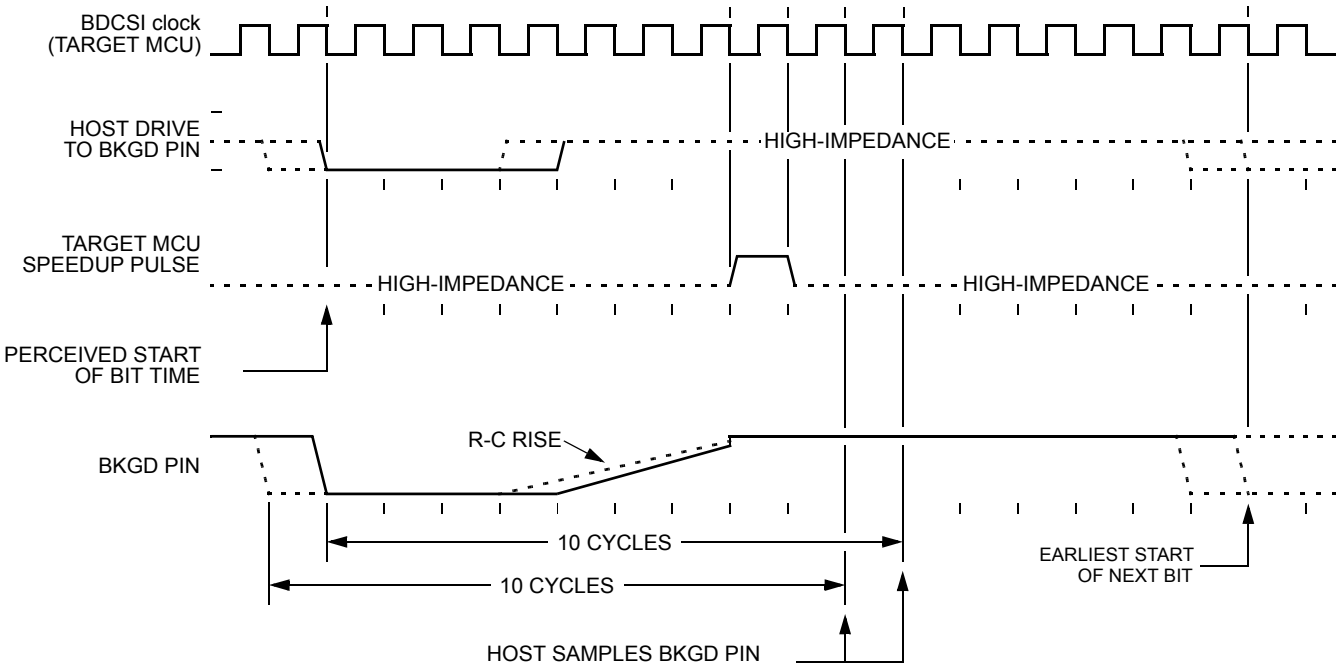


Figure 5-7. BDC Target-to-Host Serial Bit Timing (Logic 1)

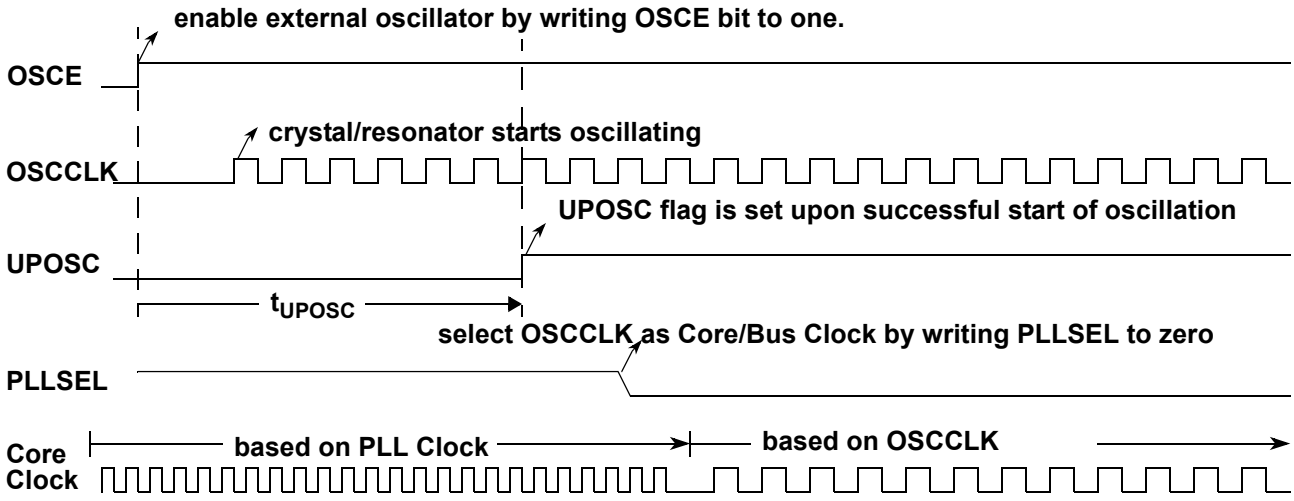
Figure 5-8 shows the host receiving a logic 0 from the target. The host initiates the bit time but the target finishes it. Since the target wants the host to receive a logic 0, it drives the BKGD pin low for 13 target clock cycles then briefly drives it high to speed up the rising edge. The host samples the bit level about 10 target clock cycles after starting the bit time.

7.4.5 External Oscillator

7.4.5.1 Enabling the External Oscillator

An example of how to use the oscillator as source of the Bus Clock is shown in Figure 7-39.

Figure 7-39. Enabling the external oscillator



10.4.2.4 ADC Timing Register (ADCTIM)

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R	0	PRS[6:0]						
W								
Reset	0	0	0	0	0	1	0	1

= Unimplemented or Reserved

Figure 10-7. ADC Timing Register (ADCTIM))

Read: Anytime

Write: These bits are writable if bit ADC_EN is clear or bit SMOD_ACC is set

Table 10-6. ADCTIM Field Descriptions

Field	Description
6-0 PRS[6:0]	**ADC Clock Prescaler** — These 7bits are the binary prescaler value PRS. The ADC conversion clock frequency is calculated as follows: $f_{ATDCLK} = \frac{f_{BUS}}{2 \times (PRS + 1)}$ Refer to Device Specification for allowed frequency range of f_{ATDCLK}.

Figure 11-24. Receive/Transmit Message Buffer — Extended Identifier Mapping (continued)

Register Name	Bit 7	6	5	4	3	2	1	Bit0

= Unused, always read 'x'

Read:

- For transmit buffers, anytime when TXEx flag is set (see Section 11.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 11.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)").
- For receive buffers, only when RXF flag is set (see Section 11.3.2.5, "MSCAN Receiver Flag Register (CANRFLG)").

Write:

- For transmit buffers, anytime when TXEx flag is set (see Section 11.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 11.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)").
- Unimplemented for receive buffers.

Reset: Undefined because of RAM-based implementation

Figure 11-25. Receive/Transmit Message Buffer — Standard Identifier Mapping

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
IDR0 0x00X0	R	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
	W								
IDR1 0x00X1	R	ID2	ID1	ID0	RTR	IDE (=0)			
	W								
IDR2 0x00X2	R								
	W								
IDR3 0x00X3	R								
	W								

= Unused, always read 'x'

11.3.3.1 Identifier Registers (IDR0–IDR3)

The identifier registers for an extended format identifier consist of a total of 32 bits: ID[28:0], SRR, IDE, and RTR. The identifier registers for a standard format identifier consist of a total of 13 bits: ID[10:0], RTR, and IDE.

Figure 11-40 shows how the first 32-bit filter bank (CANIDAR0–CANIDAR3, CANIDMR0–CANIDMR3) produces a filter 0 hit. Similarly, the second filter bank (CANIDAR4–CANIDAR7, CANIDMR4–CANIDMR7) produces a filter 1 hit.

- Four identifier acceptance filters, each to be applied to:
  - The 14 most significant bits of the extended identifier plus the SRR and IDE bits of CAN 2.0B messages.
  - The 11 bits of the standard identifier, the RTR and IDE bits of CAN 2.0A/B messages. Figure 11-41 shows how the first 32-bit filter bank (CANIDAR0–CANIDAR3, CANIDMR0–CANIDMR3) produces filter 0 and 1 hits. Similarly, the second filter bank (CANIDAR4–CANIDAR7, CANIDMR4–CANIDMR7) produces filter 2 and 3 hits.
- Eight identifier acceptance filters, each to be applied to the first 8 bits of the identifier. This mode implements eight independent filters for the first 8 bits of a CAN 2.0A/B compliant standard identifier or a CAN 2.0B compliant extended identifier.
  Figure 11-42 shows how the first 32-bit filter bank (CANIDAR0–CANIDAR3, CANIDMR0–CANIDMR3) produces filter 0 to 3 hits. Similarly, the second filter bank (CANIDAR4–CANIDAR7, CANIDMR4–CANIDMR7) produces filter 4 to 7 hits.
- Closed filter. No CAN message is copied into the foreground buffer RxFG, and the RXF flag is never set.

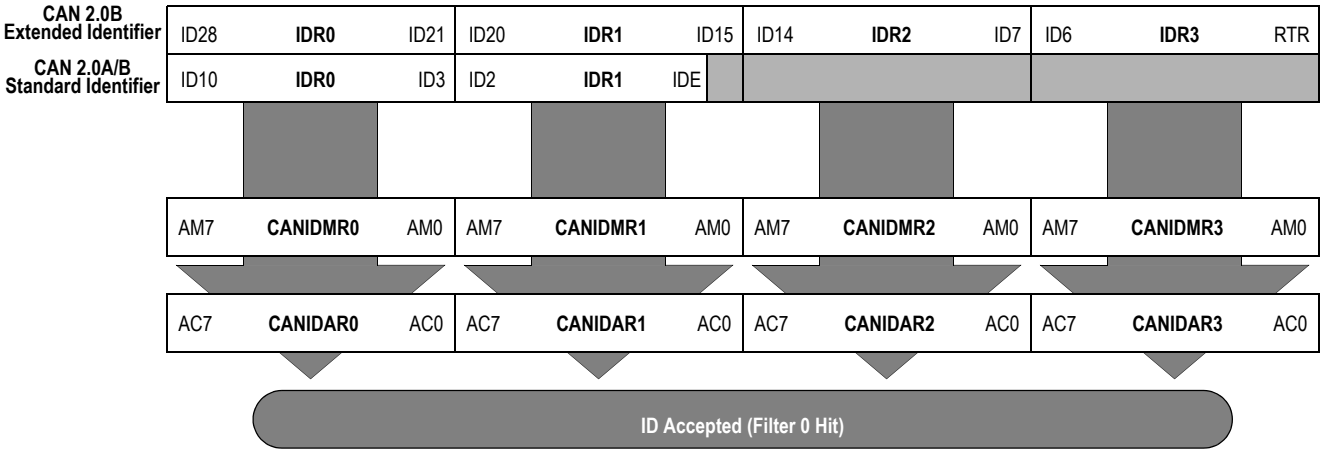


Figure 11-40. 32-bit Maskable Identifier Acceptance Filter

- Run mode

  This is the basic mode of operation.
- Wait mode

  SPI operation in wait mode is a configurable low power mode, controlled by the SPISWAI bit located in the SPICR2 register. In wait mode, if the SPISWAI bit is clear, the SPI operates like in run mode. If the SPISWAI bit is set, the SPI goes into a power conservative state, with the SPI clock generation turned off. If the SPI is configured as a master, any transmission in progress stops, but is resumed after CPU goes into run mode. If the SPI is configured as a slave, reception and transmission of data continues, so that the slave stays synchronized to the master.
- Stop mode

  The SPI is inactive in stop mode for reduced power consumption. If the SPI is configured as a master, any transmission in progress stops, but is resumed after CPU goes into run mode. If the SPI is configured as a slave, reception and transmission of data continues, so that the slave stays synchronized to the master.

For a detailed description of operating modes, please refer to Section 13.4.7, “Low Power Mode Options”.

13.1.4 Block Diagram

Figure 13-1 gives an overview on the SPI architecture. The main parts of the SPI are status, control and data registers, shifter logic, baud rate generator, master/slave control logic, and port control logic.

Chapter 14
Inter-Integrated Circuit (IICV3) Block Description

Table 14-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V01.03	28 Jul 2006	14.7.1.7/14-565	- Update flow-chart of interrupt routine for 10-bit address
V01.04	17 Nov 2006	14.3.1.2/14-545	- Revise Table1-5
V01.05	14 Aug 2007	14.3.1.1/14-545	- Backward compatible for IBAD bit name

14.1 Introduction

The inter-IC bus (IIC) is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange between devices. Being a two-wire device, the IIC bus minimizes the need for large numbers of connections between devices, and eliminates the need for an address decoder.

This bus is suitable for applications requiring occasional communications over a short distance between a number of devices. It also provides flexibility, allowing additional devices to be connected to the bus for further expansion and system development.

The interface is designed to operate up to 100 kbps with maximum bus loading and timing. The device is capable of operating at higher baud rates, up to a maximum of clock/20, with reduced bus loading. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pF.

14.1.1 Features

The IIC module has the following key features:

- Compatible with I2C bus standard
- Multi-master operation
- Software programmable for one of 256 different serial clock frequencies
- Software selectable acknowledge bit
- Interrupt driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated start signal generation

14.4.1.8 Handshaking

The clock synchronization mechanism can be used as a handshake in data transfer. Slave devices may hold the SCL low after completion of one byte transfer (9 bits). In such case, it halts the bus clock and forces the master clock into wait states until the slave releases the SCL line.

14.4.1.9 Clock Stretching

The clock synchronization mechanism can be used by slaves to slow down the bit rate of a transfer. After the master has driven SCL low the slave can drive SCL low for the required period and then release it.If the slave SCL low period is greater than the master SCL low period then the resulting SCL bus signal low period is stretched.

14.4.1.10 Ten-bit Address

A ten-bit address is indicated if the first 5 bits of the first address byte are 0x11110. The following rules apply to the first address byte.

SLAVE ADDRESS	R/W BIT	DESCRIPTION
0000000	0	General call address
0000010	x	Reserved for different bus format
0000011	x	Reserved for future purposes
11111XX	x	Reserved for future purposes
11110XX	x	10-bit slave addressing

Figure 14-13. Definition of bits in the first byte.

The address type is identified by ADTYPE. When ADTYPE is 0, 7-bit address is applied. Reversely, the address is 10-bit address.Generally, there are two cases of 10-bit address.See the Figure 14-14 and Figure 14-15.

S	Slave Add1st 7bits 11110+ADR10+ADR9	R/W 0	A1	Slave Add 2nd byte ADR[8:1]	A2	Data	A3

Figure 14-14. A master-transmitter addresses a slave-receiver with a 10-bit address

S	Slave Add1st 7bits 11110+ADR10+ADR9	R/W 0	A1	Slave Add 2nd byte ADR[8:1]	A2	Sr	Slave Add 1st 7bits 11110+ADR10+ADR9	R/W 1	A3	Data	A4

Figure 14-15. A master-receiver addresses a slave-transmitter with a 10-bit address.

In the Figure 14-15, the first two bytes are the similar to Figure 14-14. After the repeated START(Sr),the first slave address is transmitted again, but the R/W is 1, meaning that the slave is acted as a transmitter.

19.3.2.4 SSG Tone Register (SSGTONE)

SSGTONE is SSG tone register. The tone frequency range is between 100Hz to 8KHz. Refer to Table 19-7 for the tone frequency divide ratio and possible tone frequency.

Module Base + 0x0004

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	TONE9	TONE8
W								
Reset	0	0	0	0	0	0	0	0

Figure 19-7. SSG Tone Register (SSGTONEH)

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	TONE7	TONE6	TONE5	TONE4	TONE3	TONE2	TONE1	TONE0
W								
Reset	0	0	0	0	0	0	0	0

Figure 19-8. SSG Tone Register (SSGTONEL)

Read: Anytime

Write: Anytime

Table 19-6. SSGPS Field Descriptions

Field	Description
9–0 TONE[9:0]	**SSG Tone Register Bits —** The tone frequency is equal to prescaler clock / (2*(SSGTONE+1)).

Table 19-7. Tone Frequency configuration

Prescaler Clock Frequency	Tone Frequency Range	SSGTONE[9:0]	Adjacent Tone Frequency Gap Range
15KHz	100Hz~7.5KHz	0x4A~0x0	1.351Hz~3750Hz
30KHz	100Hz~7.5KHz	0x95~0x1	0.671Hz~2500Hz
60KHz	100Hz~7.5KHz	0x12B~0x3	0.334Hz~1500Hz
90KHz	100Hz~7.5KHz	0x1C1~0x5	0.223~1072Hz
125KHz	100Hz~7.813KHz	0x270~0x7	0.16Hz~1115Hz

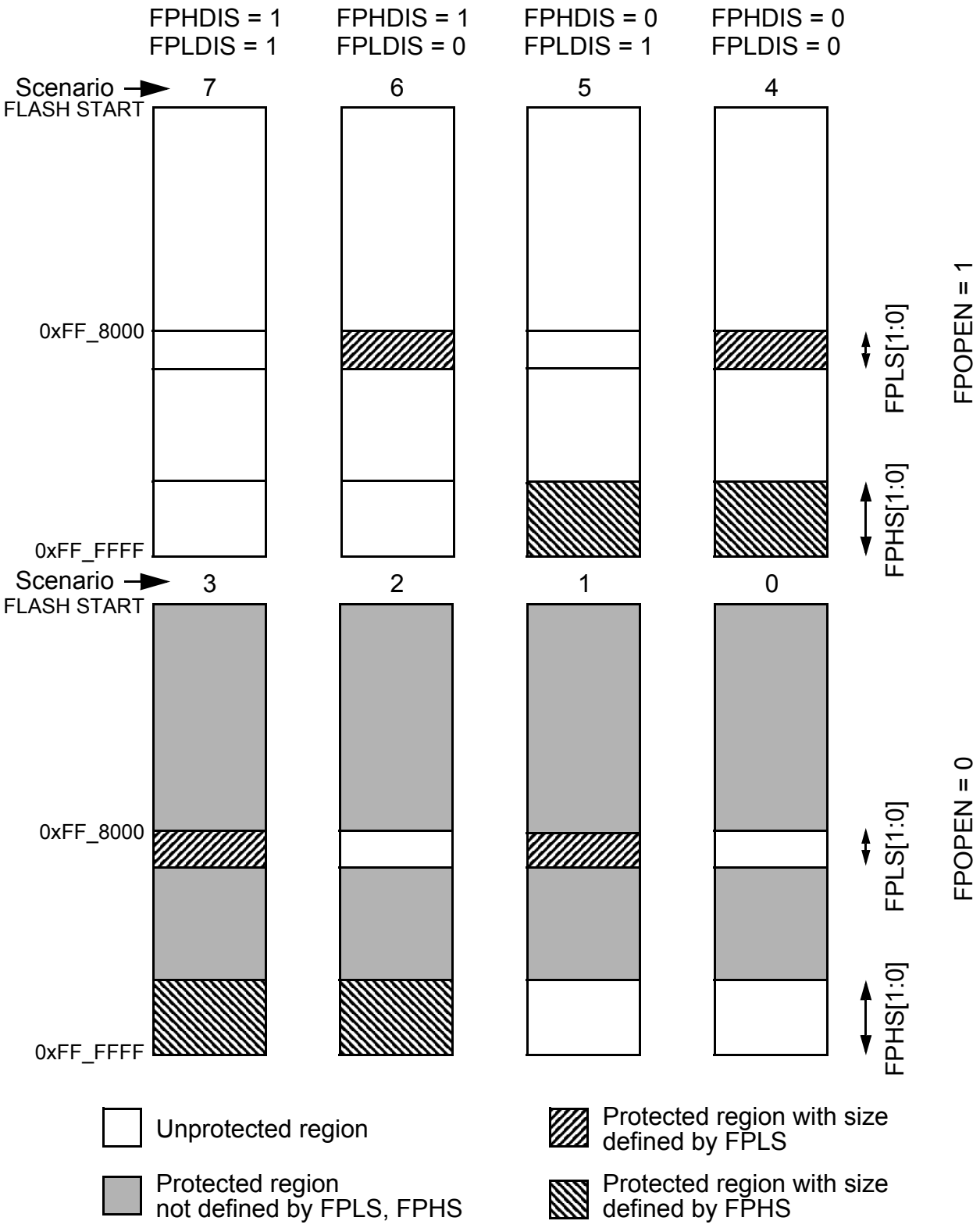


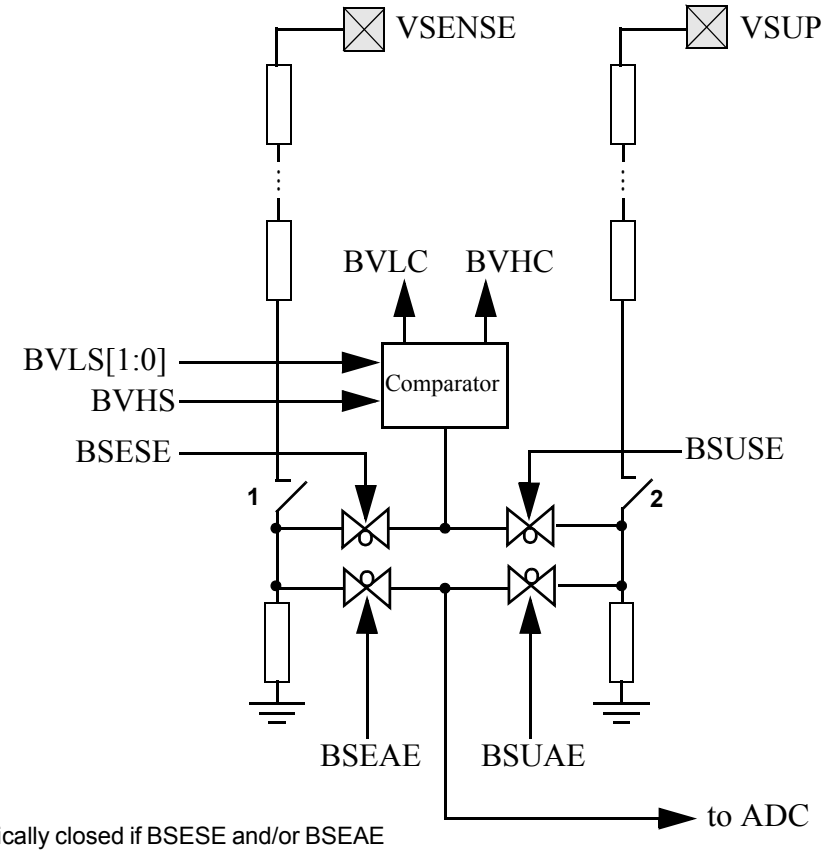
Figure 21-14. P-Flash Protection Scenarios

During stop mode operation the path from the VSUP pin through the resistor chain to ground is opened and the low voltage sense features are disabled.
The content of the configuration register is unchanged.

22.1.3 Block Diagram

Figure 22-1 shows a block diagram of the BATS module. See device guide for connectivity to ADC channel.

Figure 22-1. BATS Block Diagram



1 automatically closed if BSESE and/or BSEAE is active, open during Stop mode
2 automatically closed if BSUSE and/or BSUAE is active, open during Stop mode

22.2 External Signal Description

This section lists the name and description of all external ports.

22.2.1 VSENSE — Supply (Battery) Voltage Sense Pin

This pin can be connected to the supply (Battery) line for voltage measurements. The voltage present at this input is scaled down by an internal voltage divider, and can be routed to the internal ADC or to a

Appendix A
MCU Electrical Specifications

A.1 General

This supplement contains the most accurate electrical information for the MC9S12ZVHY/MC9S12ZVHL Families available at the time of publication.

This introduction is intended to give an overview on several common topics like power supply, current injection etc.

A.1.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

NOTE

This classification is shown in the column labeled “C” in the parameter tables where appropriate.

- P:Those parameters are guaranteed during production testing on each individual device.
- C: Those parameters are achieved in design characterization by measuring a statistically relevant sample size across process variations.
- T:Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
- D:Those parameters are derived mainly from simulations.

Table I-1. Voltage Regulator Electrical Characteristics

-40°C <= TJ <= 150°C unless noted otherwise, VDDA, VDDM and VDDX must be shorted on the application board.							
Num	**C**	**Characteristic**	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
13	P	Base Current For External PNP(VDDX)	I_{BCTL}	1.5	—	—	mA
14a	D	Startup from Reset (normal mode)	$n_{STARTUP}$	396	—	504	t_{bus}
14b	D	Startup from Reset (special mode)	$n_{STARTUP}$	555	—	555	t_{bus}
15	D	Recover time from STOP	t_{STP_REC}	—	23	—	µs

1. For the given maximum load currents and V_{SUP} input voltages, the MCU will stay out of reset.
2. Load current without the use of external PNP transistor
3. Please note that the core current is derived from VDDX
4. LVI is monitored on the VDDA supply domain
5. LVRX is monitored on the VDDX supply domain only active during full performance mode. During reduced performance mode (stopmode) voltage supervision is solely performed by the POR block monitoring core VDD.
6. The ACLK trimming must be set that the minimum period equals to 0.2ms
7. CPMUHTTR=0x88

NOTE

The LVR monitors the voltages VDD, VDDF and VDDX. If the voltage drops on these supplies to a level which could prohibit the correct function (e.g. code execution) of the microcontroller, the LVR triggers.

12b	D	Capacitance of the LIN pin, Recessive state	C_{LIN}			45	pF
13	M	Internal pull-up (slave)	R_{slave}	27	34	40	kΩ

1. For 3.5V<= V_{LINSUP} <7V, the LINPHY is still working but with degraded parametrics.
2. The V_{LINSUP} voltage is provided by the VLINSUP supply. This supply mapping is described in device level documentation.
3. At temperatures above 25C the current may be naturally limited by the driver, in this case the limitation circuit is not engaged and the flag is not set.

M.3 Dynamic Electrical Characteristics

Table M-3. Dynamic electrical characteristics of the LINPHY

Characteristics noted under conditions 7V<= V_{LINSUP} <=18V unless otherwise noted(1). Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Num	C	Ratings	Symbol	Min	Typ	Max	Unit
1	P	Minimum duration of wake-up pulse generating a wake-up interrupt	t_{WUFR}	56	72	120	µs
2	P	TxD-dominant timeout	t_{DTLIM}	16388		16389	t_{IRC}
3	P	Propagation delay of receiver	t_{rx_pd}			6	µs
4	P	Symmetry of receiver propagation delay rising edge w.r.t. falling edge	t_{rx_sym}	-2		2	µs
LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR NOMINAL SLEW RATE - 20.0KBIT/S							
5	T	Rising/falling edge time (min to max / max to min)	t_{rise}		6.5		µs
6	T	Over-current masking window (IRC trimmed at 1MHz)	t_{OCLIM}	15		16	µs
7	M	Duty cycle 1 $T_{HRec(max)} = 0.744 \times V_{LINSUP}$ $T_{HDom(max)} = 0.581 \times V_{LINSUP}$ V_{LINSUP} = 7.0V...18V t_{Bit} = 50us D1 = $t_{Bus\_rec(min)} / (2 \times t_{Bit})$	D1	0.396			
8	M	Duty cycle 2 $T_{HRec(min)} = 0.422 \times V_{LINSUP}$ $T_{HDom(min)} = 0.284 \times V_{LINSUP}$ V_{LINSUP} = 7.6V...18V t_{Bit} = 50us D2 = $t_{Bus\_rec(max)} / (2 \times t_{Bit})$	D2			0.581	
LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR SLOW SLEW RATE - 10.4KBIT/S							
9	T	Rising/falling edge time (min to max / max to min)	t_{rise}		13		µs
10	T	Over-current masking window (IRC trimmed at 1MHz)	t_{OCLIM}	31		32	µs

0x0788–0x07BF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0788-0x07BF	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x07C0–0x07C7 Inter IC Bus (IIC0)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07C0	IIC0IBAD	R	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
		W								
0x07C1	IIC0IBFD	R	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
		W								
0x07C2	IIC0IBCR	R	IBEN	IBIE	MS/$\overline{SL}$	TX/$\overline{RX}$	TXAK	0	0	IBSWAI
		W						RSTA		
0x07C3	IIC0IBSR	R	TCF	IAAS	IBB	IBAL	0	SRW	IBIF	RXAK
		W								
0x07C4	IIC0IBDR	R	D7	D6	D5	D4	D3	D2	D1	D 0
		W								
0x07C5	IIC0IBCR2	R	GCEN	ADTYPE	0	0	0	ADR10	ADR9	ADR8
		W								
0x07C6	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x07C7	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x07C8–0x07FF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07C8-0x07FF	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0A90–0x0A97 Stepper Stall Detector (SSD1)

			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0A92	SSD1CTL	R	RTZE	SDCPU	SSDWAI	FTST	0	0	ACLKS	
		W								
0x0A93	SSD1FLG	R	MCZIF	0	0	0	0	0	0	AOVIF
		W								
0x0A94	MDC1CNTH	R	MDCCNT[15:8]							
		W								
0x0A95	MDC1CNTL	R	MDCCNT[7:0]							
		W								
0x0A96	ITG1ACCH	R	ITGACC[15:8]							
		W								
0x0A97	ITG1ACCL	R	ITGACC[7:0]							
		W								

0x0A98–0x0ADF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0A98-0x0ADF	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0AE0–0x0AEF Real Time Clock (RTC)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0AE0	RTCCTL1	R	RTCEN	0	0	0	0	0	COMPE	0
		W								
0x0AE1	RTCCTL2	R	CLKSRC1	CLKSRC0	0	0	RTCPS3	RTCPS2	RTCPS1	RTCPS0
		W								
0x0AE2	RTCCTL3	R			0	0	FRZ	0	CALS	0
		W	RTCWE1	RTCWE0						
0x0AE3	RTCCTL4	R	0	0	HRIE	MINIE	SECIE	COMPIE	0	TB0IE
		W								
0x0AE4	RTCS1	R	CDLC	0	HRF	MINF	SECF	COMPF	0	TB0F
		W								
0x0AE5	RTCCCR	R	CCS		Q					
		W								
0x0AE6	RTCMODH	R	RTCMODH							
		W								
0x0AE7	RTCMODL	R	RTCMODL							
		W								