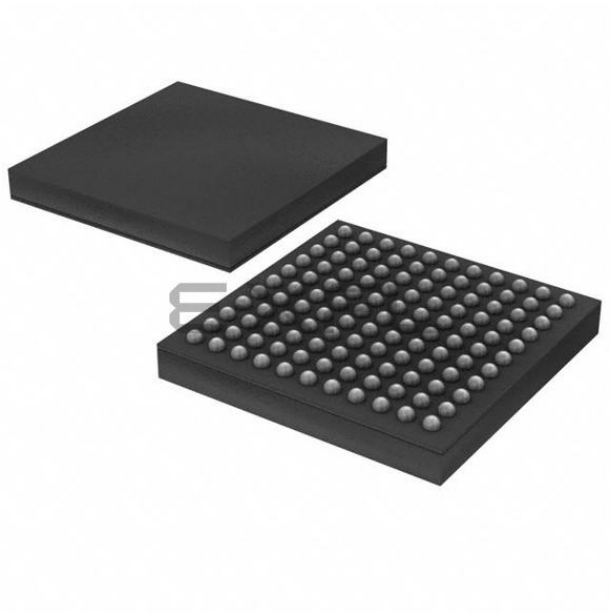

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-VFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32wg995f256-bga120t

2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32WG microcontroller. The flash memory is readable and writable from both the Cortex-M4 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32WG.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32WG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32WG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 External Bus Interface (EBI)

The External Bus Interface provides access to external parallel interface devices such as SRAM, FLASH, ADCs and LCDs. The interface is memory mapped into the address bus of the Cortex-M4. This enables seamless access from software without manually manipulating the IO settings each time a read or write is performed. The data and address lines are multiplexed in order to reduce the number of pins required to interface the external devices. The timing is adjustable to meet specifications of the external devices. The interface is limited to asynchronous devices.

3.3.2 Environmental

Table 3.3. Environmental

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ESDHBM}	ESD (Human Body Model HBM)	T_{AMB}=25°C			2500	V
V_{ESDCDM}	ESD (Charged Device Model, CDM)	T_{AMB}=25°C			500	V

Latch-up sensitivity passed: ±100 mA/1.5 × V_{SUPPLY}(max) according to JEDEC JESD 78 method Class II, 85°C.

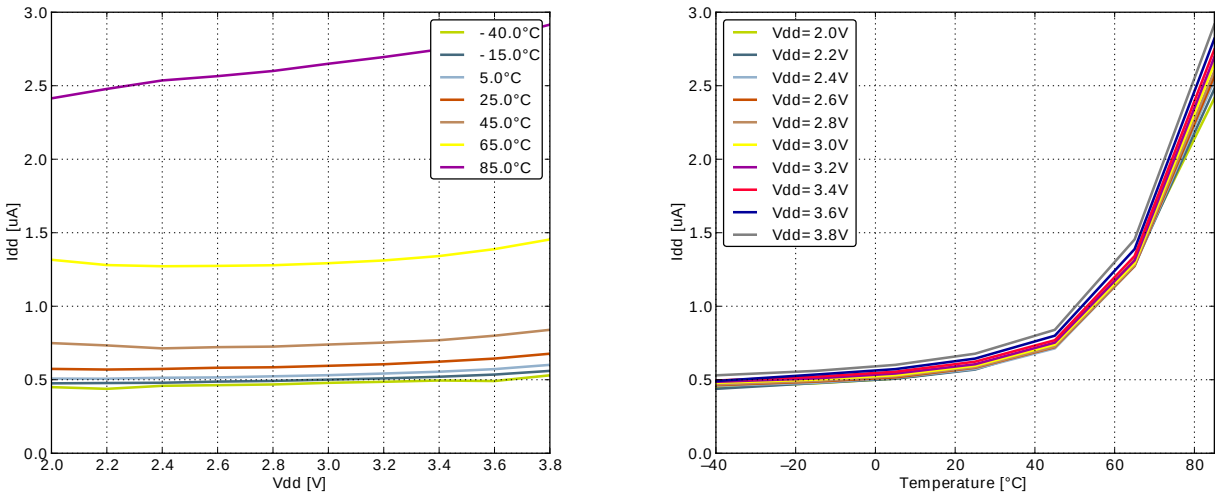
3.4 Current Consumption

Table 3.4. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	48 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		225	236	µA/MHz
		48 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		225		µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		226	238	µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		227		µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		228	240	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		229		µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		230	243	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		231		µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		232	245	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		233		µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		238	250	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		238		µA/MHz

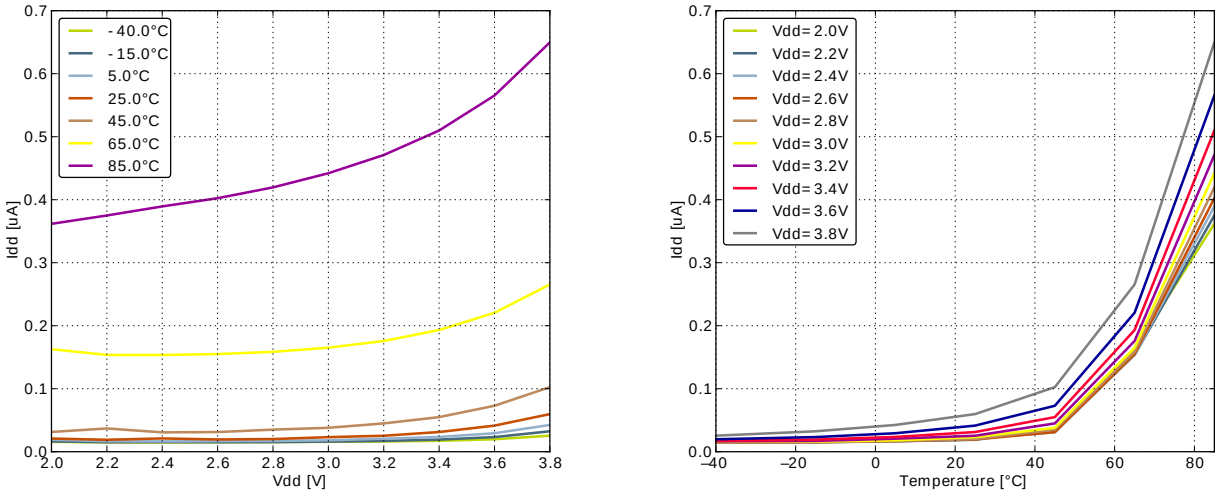
3.4.3 EM3 Current Consumption

Figure 3.9. EM3 current consumption.



3.4.4 EM4 Current Consumption

Figure 3.10. EM4 current consumption.



3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 3.5. Energy Modes Transitions

Symbol	Parameter	Min	Typ	Max	Unit
t_{EM10}	Transition time from EM1 to EM0		0		HF-CORE-CLK cycles
t_{EM20}	Transition time from EM2 to EM0		2		µs
t_{EM30}	Transition time from EM3 to EM0		2		µs
t_{EM40}	Transition time from EM4 to EM0		163		µs

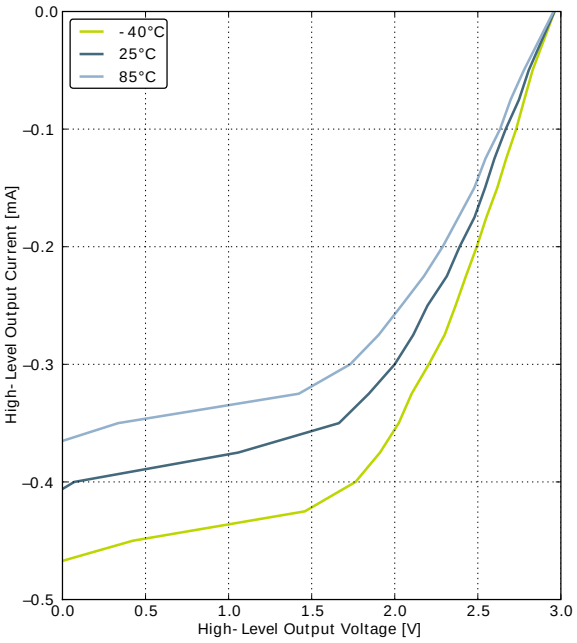
3.6 Power Management

The EFM32WG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

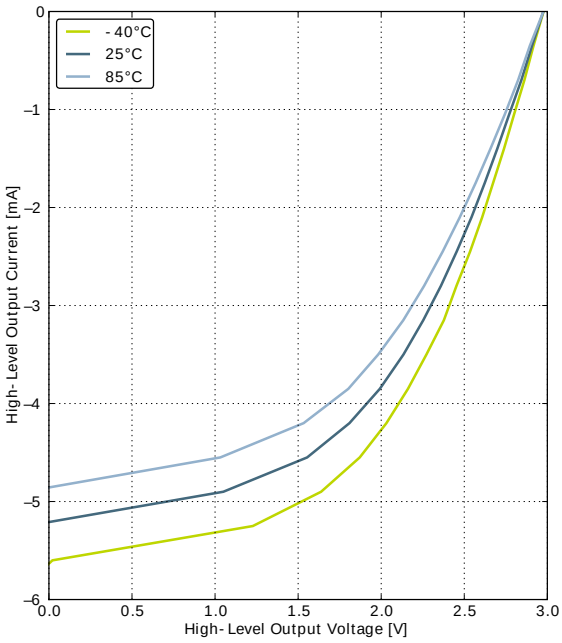
Table 3.6. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BODextthr-}$	BOD threshold on falling external supply voltage		1.74		1.96	V
$V_{BODextthr+}$	BOD threshold on rising external supply voltage			1.85	1.98	V
$V_{PORthr+}$	Power-on Reset (POR) threshold on rising external supply voltage				1.98	V
t_{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		µs
$C_{DECOUPLE}$	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		µF
C_{USB_VREGO}	USB voltage regulator out decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGO pin and GROUND		1		µF
C_{USB_VREGI}	USB voltage regulator in decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGI pin and GROUND		4.7		µF

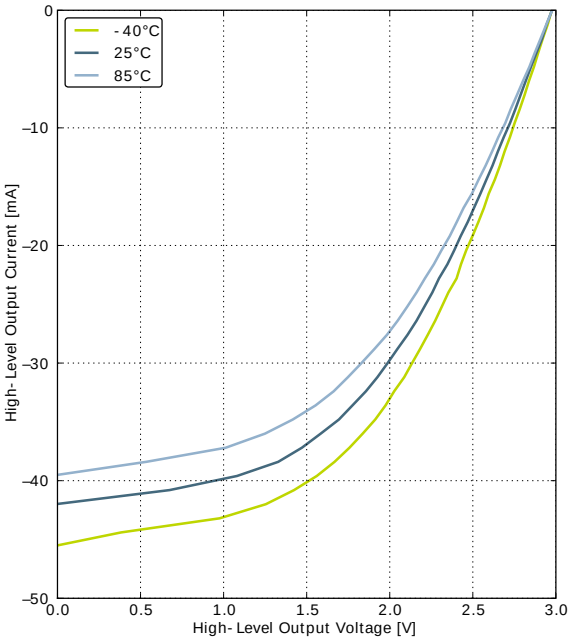
Figure 3.14. Typical High-Level Output Current, 3V Supply Voltage



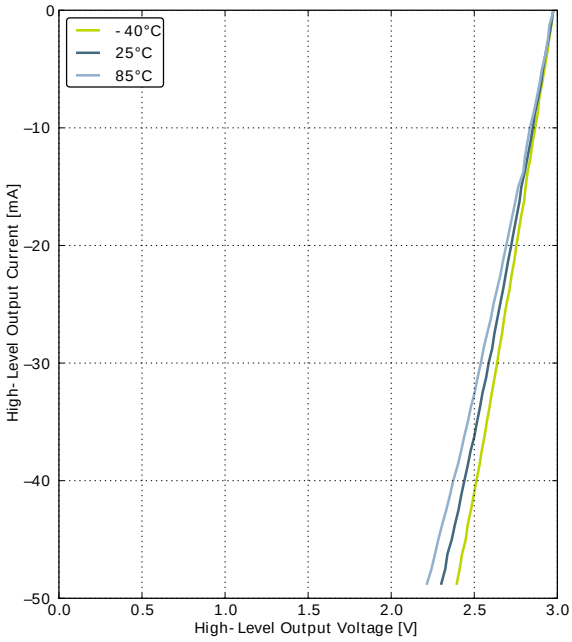
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.9. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		X[1]		25	pF
I_{LFXO}	Current consumption for core and buffer after startup.	ESR=30 kOhm, C_L=10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

[1]See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup in energyAware Designer in Simplicity Studio

For safe startup of a given crystal, the energyAware Designer in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

3.9.2 HFXO

Table 3.10. HFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Supported nominal crystal Frequency		4		48	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 48 MHz			50	Ohm
		Crystal frequency 32 MHz		30	60	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		µA
		32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		µA
t_{HFXO}	Startup time	32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		400		µs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		58		dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference		59		dB
$SNDR_{DAC}$	Signal to Noise-pulse Distortion Ratio (SNDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		57		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		54		dB
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		56		dB
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		53		dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference		55		dB
$SFDR_{DAC}$	Spurious-Free Dynamic Range(SFDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dBc
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		56		dBc
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		61		dBc
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		55		dBc
		500 kSamples/s, 12 bit, differential, V_{DD} reference		60		dBc
$V_{DACOFFSET}$	Offset voltage	After calibration, single ended		2	9	mV
		After calibration, differential		2		mV
DNL_{DAC}	Differential non-linearity			±1		LSB
INL_{DAC}	Integral non-linearity			±5		LSB
MC_{DAC}	No missing codes			12		bits

[1]Measured with a static input code and no loading on the output.

3.12 Operational Amplifier (OPAMP)

The electrical characteristics for the Operational Amplifiers are based on simulations.

Table 3.17. OPAMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{OPAMP}	Active Current	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, Unity Gain		370	460	µA
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, Unity Gain		95	135	µA

Figure 3.34. OPAMP Negative Power Supply Rejection Ratio

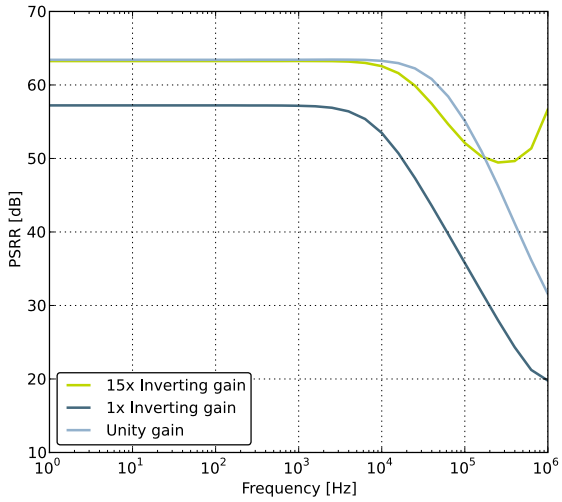


Figure 3.35. OPAMP Voltage Noise Spectral Density (Unity Gain) V_{out}=1V

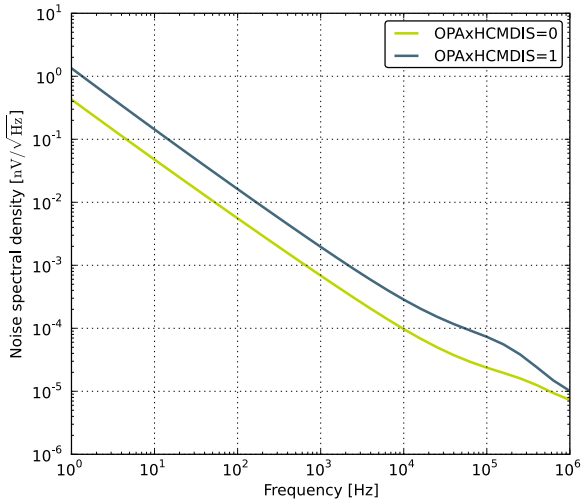
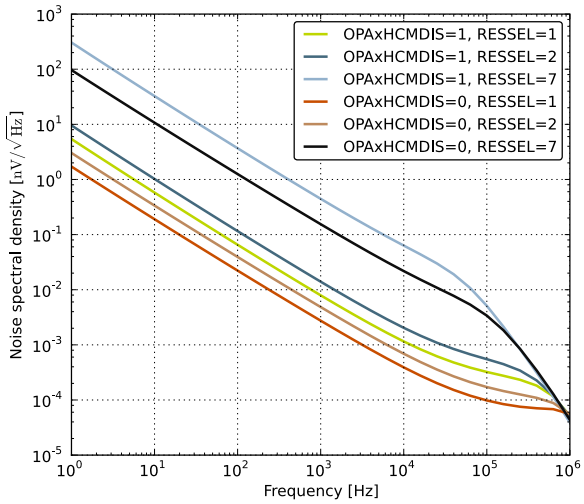


Figure 3.36. OPAMP Voltage Noise Spectral Density (Non-Unity Gain)



3.13 Analog Comparator (ACMP)

Table 3.18. ACMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ACMPIN}	Input voltage range		0		V_{DD}	V
V_{ACMPCM}	ACMP Common Mode voltage range		0		V_{DD}	V
I_{ACMP}	Active current	BIASPROG=0b0000, FULLBIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1	0.4	µA
		BIASPROG=0b1111, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87	15	µA
		BIASPROG=0b1111, FULLBIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195	520	µA
$I_{ACMPREF}$	Current consumption of internal voltage reference	Internal voltage reference off. Using external voltage reference		0		µA
		Internal voltage reference		5		µA
$V_{ACMPOFFSET}$	Offset voltage	BIASPROG= 0b1010, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register	-12	0	12	mV
$V_{ACMPHYST}$	ACMP hysteresis	Programmable		17		mV
R_{CSRES}	Capacitive Sense Internal Resistance	CSRESSEL=0b00 in ACMPn_INPUTSEL		39		kOhm
		CSRESSEL=0b01 in ACMPn_INPUTSEL		71		kOhm
		CSRESSEL=0b10 in ACMPn_INPUTSEL		104		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		136		kOhm
$t_{ACMPSTART}$	Startup time				10	µs

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 47) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

Total ACMP Active Current

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \quad (3.1)$$

3.14 Voltage Comparator (VCMP)

Table 3.19. VCMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VCMPIN}	Input voltage range			V_{DD}		V
V_{VCMPCM}	VCMP Common Mode voltage range			V_{DD}		V
I_{VCMP}	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.3	0.6	µA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.		22	35	µA
$t_{VCMPREF}$	Startup time reference generator	NORMAL		10		µs
$V_{VCMPOFFSET}$	Offset voltage	Single ended		10		mV
		Differential		10		mV
$V_{VCMPHYST}$	VCMP hysteresis			61	210	mV
$t_{VCMPSTART}$	Startup time				10	µs

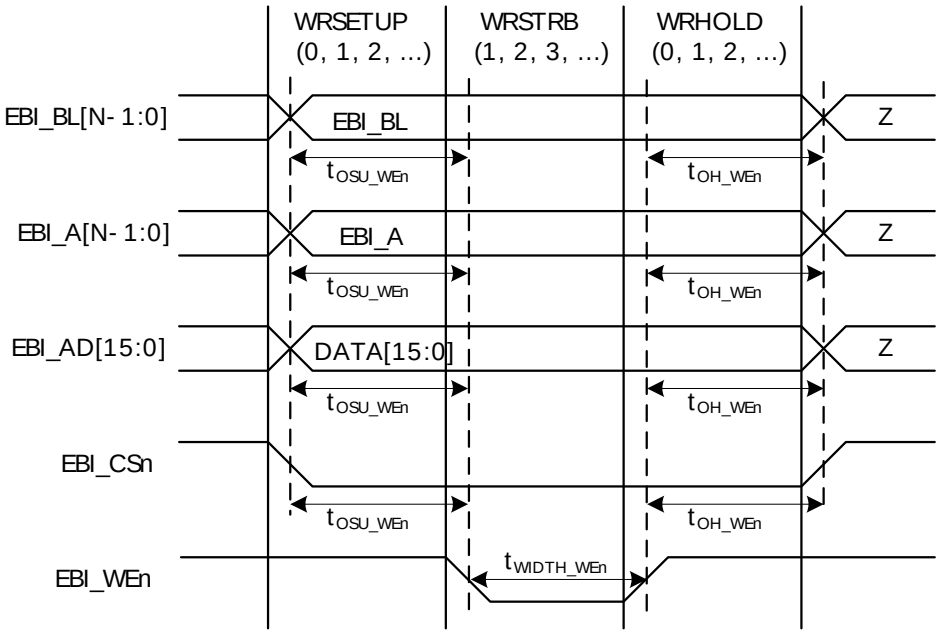
The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

VCMP Trigger Level as a Function of Level Setting

$$V_{DD\ Trigger\ Level}=1.667V+0.034 \times TRIGLEVEL \quad (3.2)$$

3.15 EBI

Figure 3.38. EBI Write Enable Timing



Symbol	Parameter	Min	Typ	Max	Unit
t_{H_ARDY} [1] [2] [3] [4]	Hold time, from trailing EBI_REn, EBI_WEn edge to EBI_ARDY invalid	-1 + (3 * $t_{HFCORECLK}$)			ns

[1]Applies for all addressing modes (figure only shows D16A8.)
[2]Applies for EBI_REn, EBI_WEn (figure only shows EBI_REn)
[3]Applies for all polarities (figure only shows active low signals)
[4]Measurement done at 10% and 90% of V_{DD} (figure shows 50% of $_{VDD}$)

3.16 LCD

Table 3.25. LCD

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LCDFR}	Frame rate		30		200	Hz
NUM_{SEG}	Number of segments supported			36×8		seg
V_{LCD}	LCD supply voltage range	Internal boost circuit enabled	2.0		3.8	V
I_{LCD}	Steady state current consumption.	Display disconnected, static mode, framerate 32 Hz, all segments on.		250		nA
		Display disconnected, quadruplex mode, framerate 32 Hz, all segments on, bias mode to ONETHIRD in LCD_DISPCTRL register.		550		nA
$I_{LCDBOOST}$	Steady state Current contribution of internal boost.	Internal voltage boost off		0		µA
		Internal voltage boost on, boosting from 2.2 V to 3.0 V.		8.4		µA
V_{BOOST}	Boost Voltage	VBLEV of LCD_DISPCTRL register to LEVEL0		3.02		V
		VBLEV of LCD_DISPCTRL register to LEVEL1		3.15		V
		VBLEV of LCD_DISPCTRL register to LEVEL2		3.28		V
		VBLEV of LCD_DISPCTRL register to LEVEL3		3.41		V
		VBLEV of LCD_DISPCTRL register to LEVEL4		3.54		V
		VBLEV of LCD_DISPCTRL register to LEVEL5		3.67		V
		VBLEV of LCD_DISPCTRL register to LEVEL6		3.73		V
		VBLEV of LCD_DISPCTRL register to LEVEL7		3.74		V

The total LCD current is given by Equation 3.3 (p. 53) . $I_{LCDBOOST}$ is zero if internal boost is off.

Total LCD Current Based on Operational Mode and Internal Boost

$$I_{LCDTOTAL} = I_{LCD} + I_{LCDBOOST} \quad (3.3)$$

3.17 I2C

Table 3.26. I2C Standard-mode (Sm)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		100[1]	kHz
t_{LOW}	SCL clock low time	4.7			µs
t_{HIGH}	SCL clock high time	4.0			µs
$t_{SU,DAT}$	SDA set-up time	250			ns
$t_{HD,DAT}$	SDA hold time	8		3450[2,3]	ns
$t_{SU,STA}$	Repeated START condition set-up time	4.7			µs
$t_{HD,STA}$	(Repeated) START condition hold time	4.0			µs
$t_{SU,STO}$	STOP condition set-up time	4.0			µs
t_{BUF}	Bus free time between a STOP and a START condition	4.7			µs

[1]For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32WG Reference Manual.
[2]The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
[3]When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450*10^{-9} [s] * $f_{HFPERCLK}$ [Hz]) - 4).

Table 3.27. I2C Fast-mode (Fm)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		400[1]	kHz
t_{LOW}	SCL clock low time	1.3			µs
t_{HIGH}	SCL clock high time	0.6			µs
$t_{SU,DAT}$	SDA set-up time	100			ns
$t_{HD,DAT}$	SDA hold time	8		900[2,3]	ns
$t_{SU,STA}$	Repeated START condition set-up time	0.6			µs
$t_{HD,STA}$	(Repeated) START condition hold time	0.6			µs
$t_{SU,STO}$	STOP condition set-up time	0.6			µs
t_{BUF}	Bus free time between a STOP and a START condition	1.3			µs

[1]For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32WG Reference Manual.
[2]The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
[3]When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900*10^{-9} [s] * $f_{HFPERCLK}$ [Hz]) - 4).

Table 3.28. I2C Fast-mode Plus (Fm+)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		1000[1]	kHz
t_{LOW}	SCL clock low time	0.5			µs
t_{HIGH}	SCL clock high time	0.26			µs
$t_{SU,DAT}$	SDA set-up time	50			ns
$t_{HD,DAT}$	SDA hold time	8			ns
$t_{SU,STA}$	Repeated START condition set-up time	0.26			µs
$t_{HD,STA}$	(Repeated) START condition hold time	0.26			µs
$t_{SU,STO}$	STOP condition set-up time	0.26			µs
t_{BUF}	Bus free time between a STOP and a START condition	0.5			µs

[1]For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32WG Reference Manual.

3.18 USART SPI

Figure 3.43. SPI Master Timing

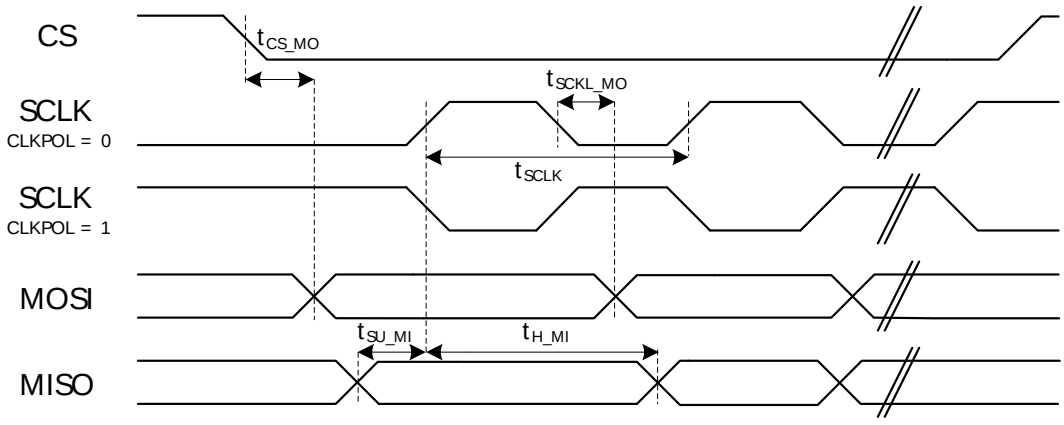


Table 3.29. SPI Master Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{SCLK} [1] [2]	SCLK period		2 * $t_{HFPERCLK}$			ns
t_{CS_MO} [1] [2]	CS to MOSI		-2.00		2.00	ns
t_{SCLK_MO} [1] [2]	SCLK to MOSI		-1.00		3.00	ns
t_{SU_MI} [1] [2]	MISO setup time	IOVDD = 3.0 V	36.00			ns
t_{H_MI} [1] [2]	MISO hold time		-6.00			ns

[1]Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

[2]Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

4 Pinout and Package

Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32WG995.

4.1 Pinout

The *EFM32WG995* pinout is shown in Figure 4.1 (p. 58) and Table 4.1 (p. 58). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32WG995 Pinout (top view, not to scale)

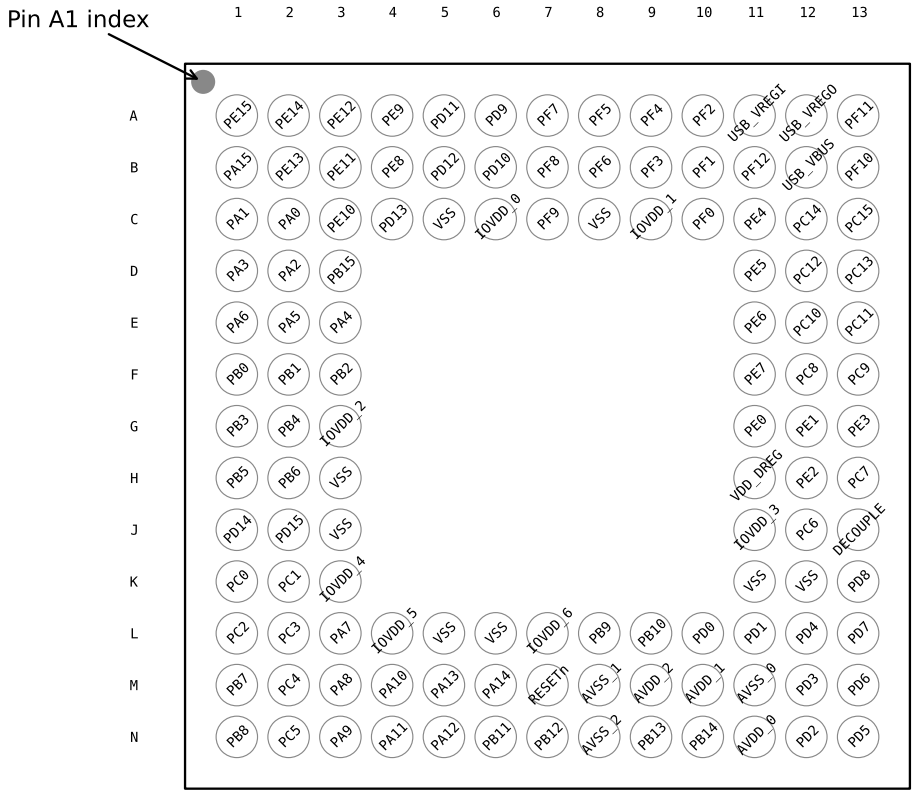


Table 4.1. Device Pinout

BGA120 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A1	PE15	LCD_SEG11	EBI_AD07 #0/1/2	TIM3_CC1 #0	LEU0_RX #2	
A2	PE14	LCD_SEG10	EBI_AD06 #0/1/2	TIM3_CC0 #0	LEU0_TX #2	
A3	PE12	LCD_SEG8	EBI_AD04 #0/1/2	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 4.2. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2							Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3							Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2	PD6					Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8							Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9							Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10							Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11							Analog comparator ACMP1, channel 3.
ACMP1_CH4	PC12							Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13							Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14							Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15							Analog comparator ACMP1, channel 7.
ACMP1_O	PF2	PE3	PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11							Bootloader RX
BOOT_TX	PE10							Bootloader TX
BU_STAT	PE3							Backup Power Domain status, whether or not the system is in backup mode
BU_VIN	PD8							Battery input for Backup Power Domain
BU_VOUT	PE2							Power output for Backup Power Domain
CMU_CLK0	PA2	PC12	PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8	PE12					Clock Management Unit, clock output number 1.
DAC0_N0 / OPAMP_N0	PC5							Operational Amplifier 0 external negative input.
DAC0_N1 / OPAMP_N1	PD7							Operational Amplifier 1 external negative input.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
OPAMP_N2	PD3							Operational Amplifier 2 external negative input.
DAC0_OUT0 / OPAMP_OUT0	PB11							Digital to Analog Converter DAC0_OUT0 / OPAMP output channel number 0.
DAC0_OUT0ALT / OPAMP_OUT0ALT	PC0	PC1	PC2	PC3	PD0			Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1 / OPAMP_OUT1	PB12							Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1.
DAC0_OUT1ALT / OPAMP_OUT1ALT	PC12	PC13	PC14	PC15	PD1			Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
OPAMP_OUT2	PD5	PD0						Operational Amplifier 2 output.
DAC0_P0 / OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
DAC0_P1 / OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0	PF0	PF0				Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1				Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15	PD1	PD2				Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_A00	PA12	PA12	PA12					External Bus Interface (EBI) address output pin 00.
EBI_A01	PA13	PA13	PA13					External Bus Interface (EBI) address output pin 01.
EBI_A02	PA14	PA14	PA14					External Bus Interface (EBI) address output pin 02.
EBI_A03	PB9	PB9	PB9					External Bus Interface (EBI) address output pin 03.
EBI_A04	PB10	PB10	PB10					External Bus Interface (EBI) address output pin 04.
EBI_A05	PC6	PC6	PC6					External Bus Interface (EBI) address output pin 05.
EBI_A06	PC7	PC7	PC7					External Bus Interface (EBI) address output pin 06.
EBI_A07	PE0	PE0	PE0					External Bus Interface (EBI) address output pin 07.
EBI_A08	PE1	PE1	PE1					External Bus Interface (EBI) address output pin 08.
EBI_A09	PE2	PC9	PC9					External Bus Interface (EBI) address output pin 09.
EBI_A10	PE3	PC10	PC10					External Bus Interface (EBI) address output pin 10.
EBI_A11	PE4	PE4	PE4					External Bus Interface (EBI) address output pin 11.
EBI_A12	PE5	PE5	PE5					External Bus Interface (EBI) address output pin 12.
EBI_A13	PE6	PE6	PE6					External Bus Interface (EBI) address output pin 13.
EBI_A14	PE7	PE7	PE7					External Bus Interface (EBI) address output pin 14.
EBI_A15	PC8	PC8	PC8					External Bus Interface (EBI) address output pin 15.
EBI_A16	PB0	PB0	PB0					External Bus Interface (EBI) address output pin 16.
EBI_A17	PB1	PB1	PB1					External Bus Interface (EBI) address output pin 17.
EBI_A18	PB2	PB2	PB2					External Bus Interface (EBI) address output pin 18.
EBI_A19	PB3	PB3	PB3					External Bus Interface (EBI) address output pin 19.
EBI_A20	PB4	PB4	PB4					External Bus Interface (EBI) address output pin 20.
EBI_A21	PB5	PB5	PB5					External Bus Interface (EBI) address output pin 21.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_HSNC	PA11	PA11	PA11					External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREn	PC3	PC3	PC3					External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEn	PC5	PC5	PC5					External Bus Interface (EBI) NAND Write Enable output.
EBI_REn	PF5	PF9	PF5					External Bus Interface (EBI) Read Enable output.
EBI_VSNC	PA10	PA10	PA10					External Bus Interface (EBI) TFT Vertical Synchronization pin.
EBI_WEn	PF4	PF8	PF4					External Bus Interface (EBI) Write Enable output.
ETM_TCLK	PD7	PF8	PC6	PA6				Embedded Trace Module ETM clock .
ETM_TD0	PD6	PF9	PC7	PA2				Embedded Trace Module ETM data 0.
ETM_TD1	PD3	PD13	PD3	PA3				Embedded Trace Module ETM data 1.
ETM_TD2	PD4	PB15	PD4	PA4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5	PF3	PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12	PE1					I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11	PE0					I2C1 Serial Data input / output.
LCD_BCAP_N	PA13							LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12							LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14							LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4							LCD driver common line number 0.
LCD_COM1	PE5							LCD driver common line number 1.
LCD_COM2	PE6							LCD driver common line number 2.
LCD_COM3	PE7							LCD driver common line number 3.
LCD_SEG0	PF2							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG1	PF3							LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG2	PF4							LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0.

1. The dimensions in parenthesis are reference.
2. Datum "C" and seating plane are defined by the crown of the soldier balls.
3. All dimensions are in millimeters.

The BGA120 Package uses SAC105 solderballs.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see:
http://www.silabs.com/support/quality/pages/default.aspx.

7 Revision History

7.1 Revision 1.40

June 13th, 2014

Removed "Preliminary" markings.

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Added AUXHFRCO to blockdiagram and electrical characteristics.

Updated current consumption data.

Updated transition between energy modes data.

Updated power management data.

Updated GPIO data.

Updated LFRCO, HFRCO and ULFRCO data.

Updated ADC data.

Updated DAC data.

Updated OPAMP data.

Updated ACMP data.

Updated VCMP data.

Added EBI timing chapter.

7.2 Revision 1.31

November 21st, 2013

Updated figures.

Updated errata-link.

Updated chip marking.

Added link to Environmental and Quality information.

Re-added missing DAC-data.

7.3 Revision 1.30

September 30th, 2013

Added I2C characterization data.

Added SPI characterization data.

Corrected the DAC and OPAMP2 pin sharing information in the Alternate Functionality Pinout section.

Added the USB bootloader information.

Corrected the ADC resolution from 12, 10 and 6 bit to 12, 8 and 6 bit.

Updated the EM0 and EM1 current consumption numbers. Updated the the EM1 plots and removed the EM0 plots.

Updated Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

7.4 Revision 1.20

June 28th, 2013

Corrected pinout top view figure.

Updated PCB Land Pattern, PCB Solder Mask and PCB Stencil Design figures.

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

7.5 Revision 1.10

May 6th, 2013

Updated current consumption table and figures in Electrical characteristics section.

Other minor corrections.

7.6 Revision 1.00

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Corrected BGA solder balls material from Sn96.5/Ag3/Cu0.5 to SAC105.

Other minor corrections.

7.7 Revision 0.95

May 3rd, 2012

Updated EM2/EM3 current consumption at 85°C.

7.8 Revision 0.90

February 27th, 2012

Initial preliminary release.