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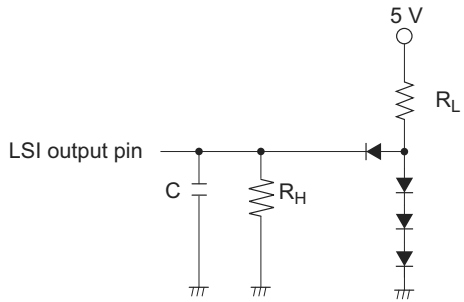
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2600
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SmartCard
Peripherals	Motor Control PWM, POR, PWM, WDT
Number of I/O	72
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-BFQFP
Supplier Device Package	128-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2636uf20jv

Item	Page	Revision (See Manual for Details)
24.1.3 DC Characteristics Table 24-2 DC Characteristics	982	Table amended

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0.5 V to V_{CC} – 0.5 V
	$\overline{STBY}$, $\overline{NMI}$, MD2 to MD0		—	—	1.0		
	HRxD0, HRxD1, FWE		—	—	1.0		
	Ports 4, 9		—	—	1.0		V_{in} = 0.5 V to AV_{CC} – 0.5 V

24.1.4 AC Characteristics Figure 24-2 Output Load Circuit	985	Figure amended



C = 50 pF: Ports 10 to 13, A to F
(In case of expansion bus control signal output pin setting)
C = 30 pF: All ports except ports 10 to 13, A to F
R_L = 2.4 kΩ
R_H = 12 kΩ
Input/output timing measurement levels
- Low level: 0.8 V
- High level: 2.0 V

24.2.3 DC Characteristics Table 24-12 DC Characteristics	996	Table amended

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	$\overline{IRQ0}$ to $\overline{IRQ5}$	V_T^-	1.0	—	—	V	
		V_T^+	—	—	V_{CC} × 0.7		
		$V_T^+ - V_T^-$	0.4	—	—		

	997	Table amended

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0.5 V to V_{CC} – 0.5 V
	$\overline{STBY}$, $\overline{NMI}$, MD2 to MD0		—	—	1.0		
	HRxD0, HRxD1, FWE		—	—	1.0		
	Ports 4, 9		—	—	1.0		V_{in} = 0.5 V to AV_{CC} – 0.5 V

Pin No.	Pin Name			
FP-128B	Mode 4	Mode 5	Mode 6	Mode 7
57	PJ2/PWM2C	PJ2/PWM2C	PJ2/PWM2C	PJ2/PWM2C
58	PJ3/PWM2D	PJ3/PWM2D	PJ3/PWM2D	PJ3/PWM2D
59	PWMVCC	PWMVCC	PWMVCC	PWMVCC
60	PJ4/PWM2E	PJ4/PWM2E	PJ4/PWM2E	PJ4/PWM2E
61	PJ5/PWM2F	PJ5/PWM2F	PJ5/PWM2F	PJ5/PWM2F
62	PJ6/PWM2G	PJ6/PWM2G	PJ6/PWM2G	PJ6/PWM2G
63	PJ7/PWM2H	PJ7/PWM2H	PJ7/PWM2H	PJ7/PWM2H
64	PWMVSS	PWMVSS	PWMVSS	PWMVSS
65	P30/TxD0	P30/TxD0	P30/TxD0	P30/TxD0
66	P31/RxD0	P31/RxD0	P31/RxD0	P31/RxD0
67	VSS	VSS	VSS	VSS
68	VSS	VSS	VSS	VSS
69	P32/SCK0/SDA1[*2]/ $\overline{\text{IRQ4}}$	P32/SCK0/SDA1[*2]/ $\overline{\text{IRQ4}}$	P32/SCK0/SDA1[*2]/ $\overline{\text{IRQ4}}$	P32/SCK0/SDA1[*2]/ $\overline{\text{IRQ4}}$
70	P33/TxD1/SCL1[*2]	P33/TxD1/SCL1[*2]	P33/TxD1/SCL1[*2]	P33/TxD1/SCL1[*2]
71	P34/RxD1/SDA0[*2]	P34/RxD1/SDA0[*2]	P34/RxD1/SDA0[*2]	P34/RxD1/SDA0[*2]
72	P35/SCK1/SCL0[*2]/ $\overline{\text{IRQ5}}$	P35/SCK1/SCL0[*2]/ $\overline{\text{IRQ5}}$	P35/SCK1/SCL0[*2]/ $\overline{\text{IRQ5}}$	P35/SCK1/SCL0[*2]/ $\overline{\text{IRQ5}}$
73	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$
74	NMI	NMI	NMI	NMI
75	PLLCAP	PLLCAP	PLLCAP	PLLCAP
76	VSS	VSS	VSS	VSS
77	PLLVSS	PLLVSS	PLLVSS	PLLVSS
78	OSC2[*1]	OSC2[*1]	OSC2[*1]	OSC2[*1]
79	OSC1[*1]	OSC1[*1]	OSC1[*1]	OSC1[*1]
80	VCC	VCC	VCC	VCC
81	VCC	VCC	VCC	VCC
82	VCL	VCL	VCL	VCL
83	XTAL	XTAL	XTAL	XTAL
84	VSS	VSS	VSS	VSS
85	EXTAL	EXTAL	EXTAL	EXTAL
86	FWE[*3]	FWE[*3]	FWE[*3]	FWE[*3]

4.2 Reset

4.2.1 Overview

A reset has the highest exception priority.

When the $\overline{\text{RES}}$ pin goes low, all current operations are stopped, and this LSI enters reset state. A reset initializes the internal state of the CPU and the registers of on-chip supporting modules. Immediately after a reset, interrupt control mode 0 is set.

When the $\overline{\text{RES}}$ pin goes from low to high, reset exception handling starts.

The H8S/2636 can also be reset by overflow of the watchdog timer. For details see section 12, Watchdog Timer.

4.2.2 Reset Sequence

This LSI enters reset state when the $\overline{\text{RES}}$ pin goes low.

To ensure that this LSI is reset, hold the $\overline{\text{RES}}$ pin low for at least 20 ms at power-up. To reset during operation, hold the $\overline{\text{RES}}$ pin low for at least 20 states.

When the $\overline{\text{RES}}$ pin goes high after being held low for the necessary time, this LSI starts reset exception handling as follows.

1. The internal state of the CPU and the registers of the on-chip supporting modules are initialized, the T bit is cleared to 0 in EXR, and the I bit is set to 1 in EXR and CCR.
2. The reset exception handling vector address is read and transferred to the PC, and program execution starts from the address indicated by the PC.

Figures 4-2 and 4-3 show examples of the reset sequence.

8.2.2 DTC Mode Register B (MRB)

Bit	:	7	6	5	4	3	2	1	0
		CHNE	DISEL	—	—	—	—	—	—
Initial value:		*	*	*	*	*	*	*	*
R/W	:	—	—	—	—	—	—	—	—

*: Undefined

MRB is an 8-bit register that controls the DTC operating mode.

Bit 7—DTC Chain Transfer Enable (CHNE): Specifies chain transfer. With chain transfer, a number of data transfers can be performed consecutively in response to a single transfer request.

In data transfer with CHNE set to 1, determination of the end of the specified number of transfers, clearing of the interrupt source flag, and clearing of DTCER is not performed.

Bit 7

CHNE	Description
0	End of DTC data transfer (activation waiting state is entered)
1	DTC chain transfer (new register information is read, then data is transferred)

Bit 6—DTC Interrupt Select (DISEL): Specifies whether interrupt requests to the CPU are disabled or enabled after a data transfer.

Bit 6

DISEL	Description
0	After a data transfer ends, the CPU interrupt is disabled unless the transfer counter is 0 (the DTC clears the interrupt source flag of the activating interrupt to 0)
1	After a data transfer ends, the CPU interrupt is enabled (the DTC does not clear the interrupt source flag of the activating interrupt to 0)

Bits 5 to 0—Reserved: These bits have no effect on DTC operation in the chip, and should always be written with 0.

8.3.9 Operation Timing

Figures 8-10 to 8-12 show an example of DTC operation timing.

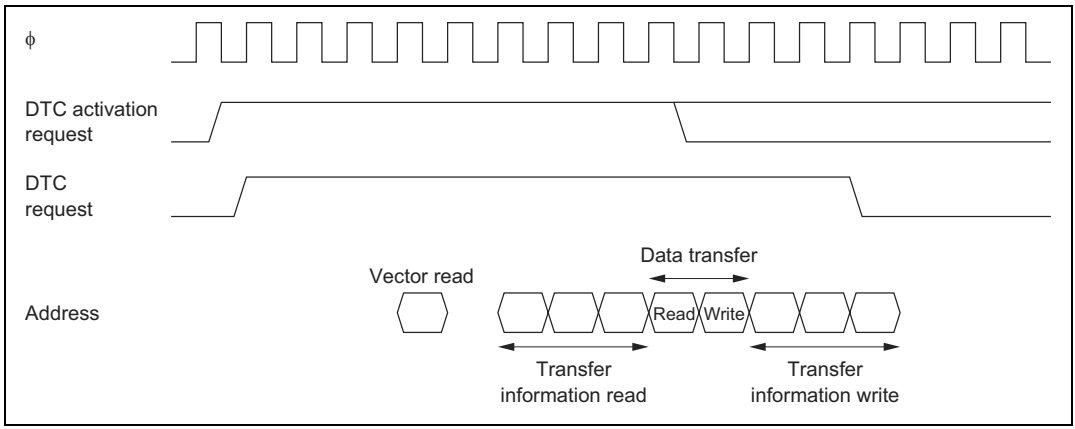


Figure 8-10 DTC Operation Timing (Example in Normal Mode or Repeat Mode)

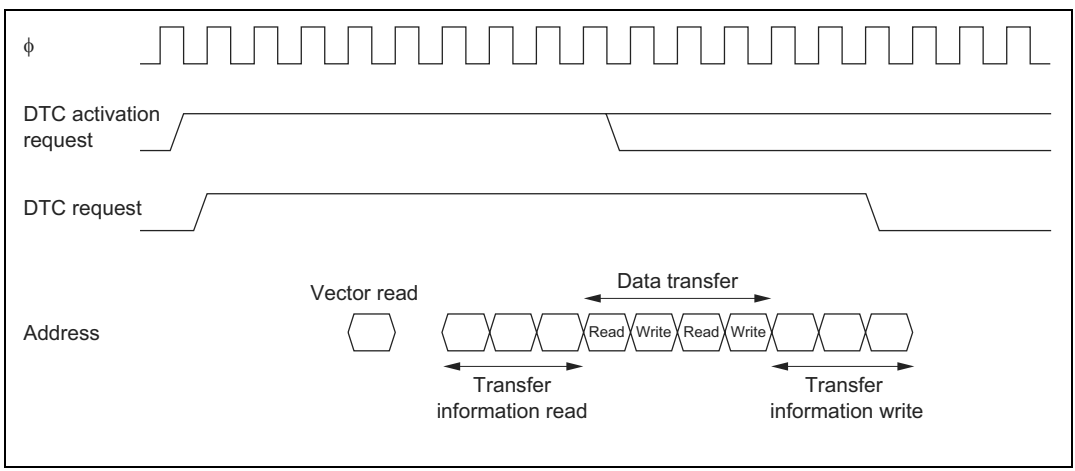


Figure 8-11 DTC Operation Timing (Example of Block Transfer Mode, with Block Size of 2)

9.8.3 Pin Functions for Each Mode

Modes 4 and 5: In modes 4 and 5, port C pins function as address outputs automatically.

Figure 9-12 shows the port C pin functions.

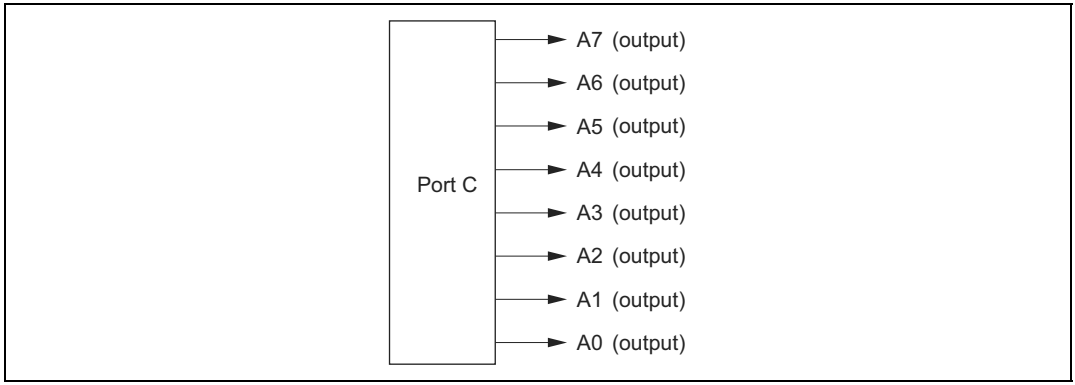


Figure 9-12 Port C Pin Functions (Modes 4 and 5)

Mode 6: In mode 6, port C pints function as address outputs or input ports and I/O can be specified in bit units. When each bit in PCDDR is set to 1, the corresponding pin functions as an address output and when the bit cleared to 0, the pin functions as an input port.

Figure 9-13 shows the port C pin functions.

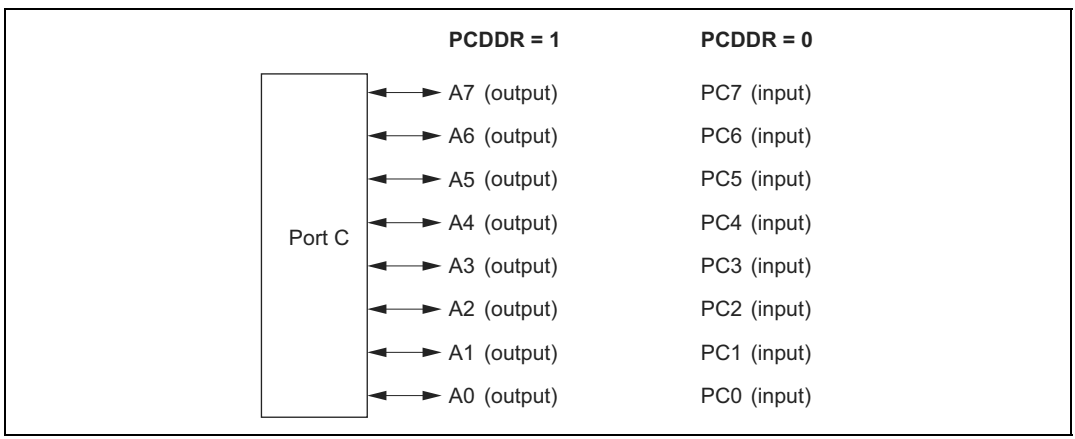


Figure 9-13 Port C Pin Functions (Mode 6)

10.2.5 Timer Status Register (TSR)

Channel 0: TSR0
Channel 3: TSR3

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
Initial value	:	1	1	0	0	0	0	0	0
R/W	:	—	—	—	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: * Can only be written with 0 for flag clearing.

Channel 1: TSR1
Channel 2: TSR2
Channel 4: TSR4
Channel 5: TSR5

Bit	:	7	6	5	4	3	2	1	0
		TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
Initial value	:	1	1	0	0	0	0	0	0
R/W	:	R	—	R/(W)*	R/(W)*	—	—	R/(W)*	R/(W)*

Note: * Can only be written with 0 for flag clearing.

The TSR registers are 8-bit registers that indicate the status of each channel. The TPU has six TSR registers, one for each channel. The TSR registers are initialized to H'C0 by a reset, and in hardware standby mode.

- Phase counting mode 3

  Figure 10-31 shows an example of phase counting mode 3 operation, and table 10-11 summarizes the TCNT up/down-count conditions.

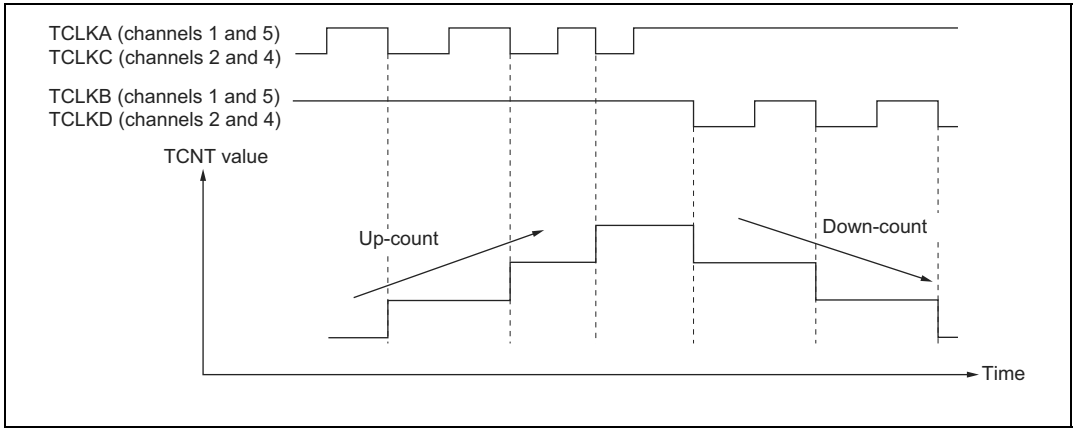


Figure 10-31 Example of Phase Counting Mode 3 Operation

Table 10-11 Up/Down-Count Conditions in Phase Counting Mode 3

TCLKA (Channels 1 and 5) TCLKC (Channels 2 and 4)	TCLKB (Channels 1 and 5) TCLKD (Channels 2 and 4)	Operation
High level	↑	Don't care
Low level	↓	
↑	Low level	
↓	High level	Up-count
High level	↓	Down-count
Low level	↑	Don't care
↑	High level	
↓	Low level	

Legend:

↑ : Rising edge

↓ : Falling edge

12.2.2 Timer Control/Status Register (TCSR)

TCSR0

Bit	:	7	6	5	4	3	2	1	0
		OVF	WT/$\overline{IT}$	TME	—	—	CKS2	CKS1	CKS0
Initial value	:	0	0	0	1	1	0	0	0
R/W	:	R/(W)*	R/W	R/W	—	—	R/W	R/W	R/W

Note: * Only a 0 may be written to this bit to clear the flag.

TCSR1

Bit	:	7	6	5	4	3	2	1	0
		OVF	WT/$\overline{IT}$	TME	PSS*2	RST/$\overline{NMI}$	CKS2	CKS1	CKS0
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/(W)*1	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Notes: 1. Only a 0 may be written to this bit to clear the flag.
2. Subclock functions (subactive mode, subsleep mode, and watch mode) are available in the U-mask and W-mask versions, and H8S/2635 Group only.

TCSR is an 8-bit readable/writable* register. Its functions include selecting the clock source to be input to TCNT, and the timer mode.

TCSR0 (TCSR1) is initialized to H'18 (H'00) by a reset and in hardware standby mode. It is not initialized in software standby mode.

Note: * TCSR is write-protected by a password to prevent accidental overwriting. For details see section 12.2.4, Notes on Register Access.

13.2.5 Serial Mode Register (SMR)

Bit	:	7	6	5	4	3	2	1	0
		C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SMR is an 8-bit register used to set the SCI's serial transfer format and select the baud rate generator clock source.

SMR can be read or written to by the CPU at all times.

SMR is initialized to H'00 by a reset and in hardware standby mode.

Bit 7—Communication Mode (C/$\overline{A}$): Selects asynchronous mode or clocked synchronous mode as the SCI operating mode.

Bit 7

C/$\overline{A}$	Description	
0	Asynchronous mode	(Initial value)
1	Clocked synchronous mode	

Bit 6—Character Length (CHR): Selects 7 or 8 bits as the data length in asynchronous mode. In clocked synchronous mode, a fixed data length of 8 bits is used regardless of the CHR setting.

Bit 6

CHR	Description	
0	8-bit data	(Initial value)
1	7-bit data*	

Note: * When 7-bit data is selected, the MSB (bit 7) of TDR is not transmitted, and it is not possible to choose between LSB-first or MSB-first transfer.

15.3 Operation

15.3.1 I²C Bus Data Format

The I²C bus interface has serial and I²C bus formats.

The I²C bus formats are addressing formats with an acknowledge bit. These are shown in figures 15-3 (a) and (b). The first frame following a start condition always consists of 8 bits.

The serial format is a non-addressing format with no acknowledge bit. Although start and stop conditions must be issued, this format can be used as a synchronous serial format. This is shown in figure 15-4.

Figure 15-5 shows the I²C bus timing.

The symbols used in figures 15-3 to 15-5 are explained in table 15-4.

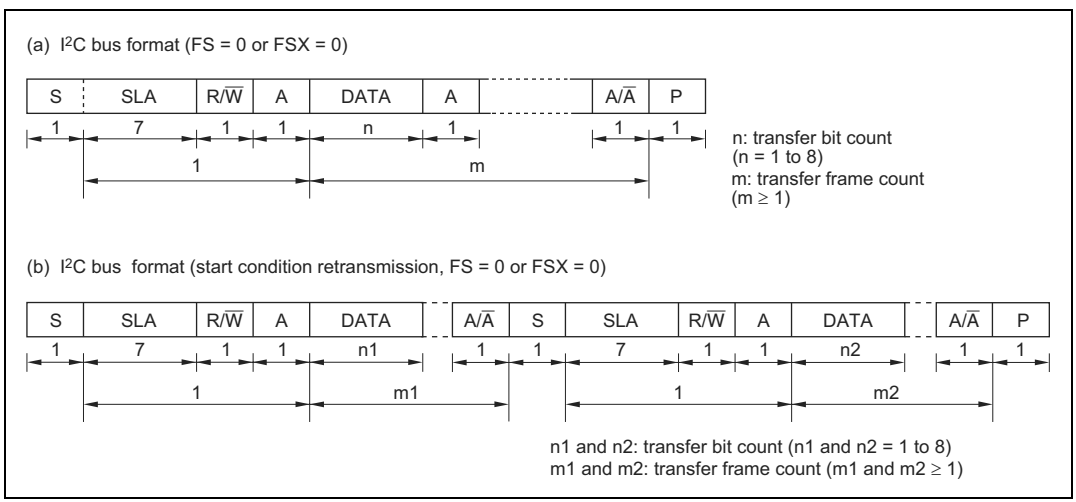


Figure 15-3 I²C Bus Data Formats (I²C Bus Formats)

16.2.18 Message Control (MC0 to MC15)

The message control register sets (MC0 to MC15) consist of eight 8-bit readable/writable registers (MCx[1] to MCx[8]). The HCAN has 16 sets of these registers (MC0 to MC15).

The initial value of these registers is undefined, so they must be initialized (by writing 0 or 1).

MCx [1]

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	DLC3	DLC2	DLC1	DLC0
Initial value:	*	*	*	*	*	*	*	*
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MCx [2]

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value:	*	*	*	*	*	*	*	*
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MCx [3]

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value:	*	*	*	*	*	*	*	*
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MCx [4]

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value:	*	*	*	*	*	*	*	*
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

*:Undefined

21A.13 Programmer Mode

In programmer mode, a PROM programmer can be used to perform programming/erasing via a socket adapter, just as for a discrete flash memory. Use a PROM programmer that supports the Renesas Electronics's 128-kbyte flash memory on-chip MCU device type (FZTAT128V5A).

21A.13.1 Socket Adapter and Memory Map

In programmer mode in which the PROM writer is used, reading from memory (verification), writing, and initializing the flash memory (erasing all of its contents) are enabled. At this time, a dedicated conversion socket adapter must be used. Table 21A-13 shows the types of the socket adapters. For programmer mode on this LSI, one of the socket adapters listed in table 21A-13 should be used.

Table 21A-13 Type of Socket Adapter

Part No.	Package Type	Socket Adapter Type	Manufacturer
HD64F2636UF	128 pin QFP	ME2636ESHF1H	Minato Electronics Inc.
HD64F2636F	(FP-128B)	HF2636Q128D4001	Data I/O Japan Corporation

The memory map of on-chip ROM is shown in figure 21A-17

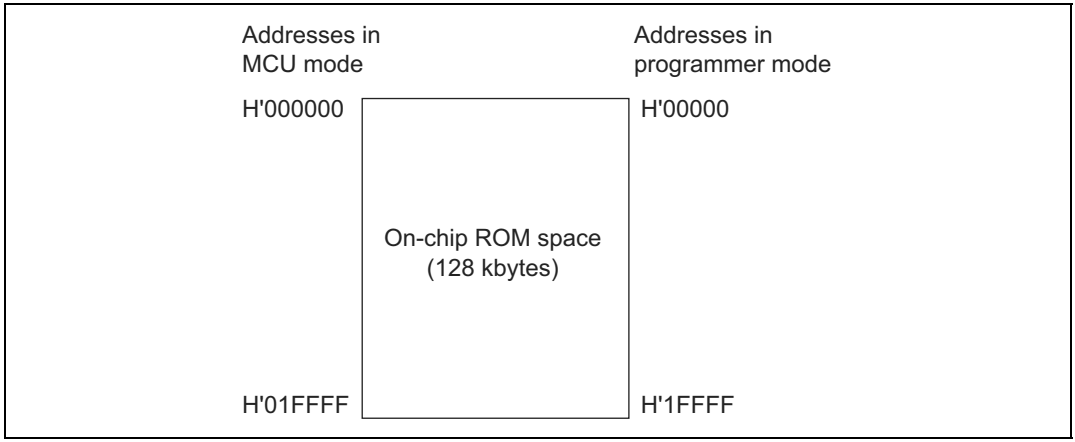


Figure 21A-17 On-Chip ROM Memory Map

Figure 21B-14 shows the flash memory state transition diagram.

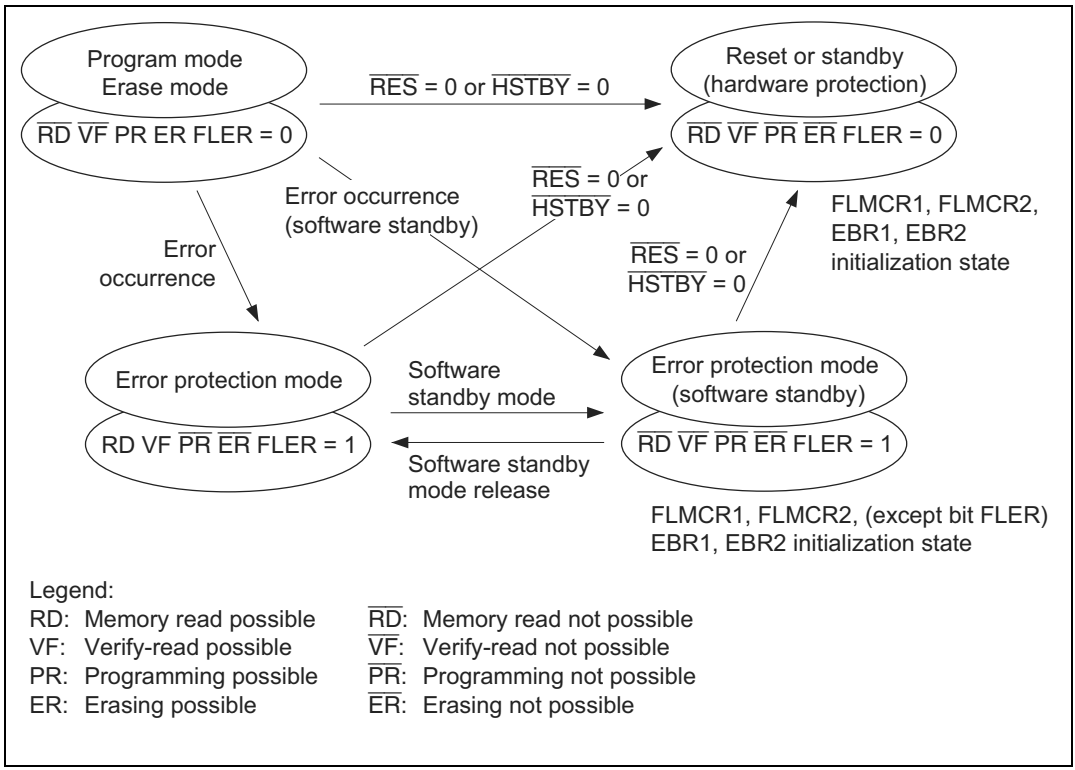


Figure 21B-14 Flash Memory State Transitions

21C.8.1 Boot Mode

When boot mode is used, the flash memory programming control program must be prepared in the host beforehand. The SCI channel to be used is set to asynchronous mode.

When a reset-start is executed after the H8S/2635 Group's pins have been set to boot mode, the boot program built into the H8S/2635 Group are started and the programming control program prepared in the host is serially transmitted to the H8S/2635 Group via the SCI. In the H8S/2635 Group, the programming control program received via the SCI is written into the programming control program area in on-chip RAM. After the transfer is completed, control branches to the start address of the programming control program area and the programming control program execution state is entered (flash memory programming is performed).

The transferred programming control program must therefore include coding that follows the programming algorithm given later.

The system configuration in boot mode is shown in figure 21C-7, and the boot mode execution procedure in figure 21C-8.

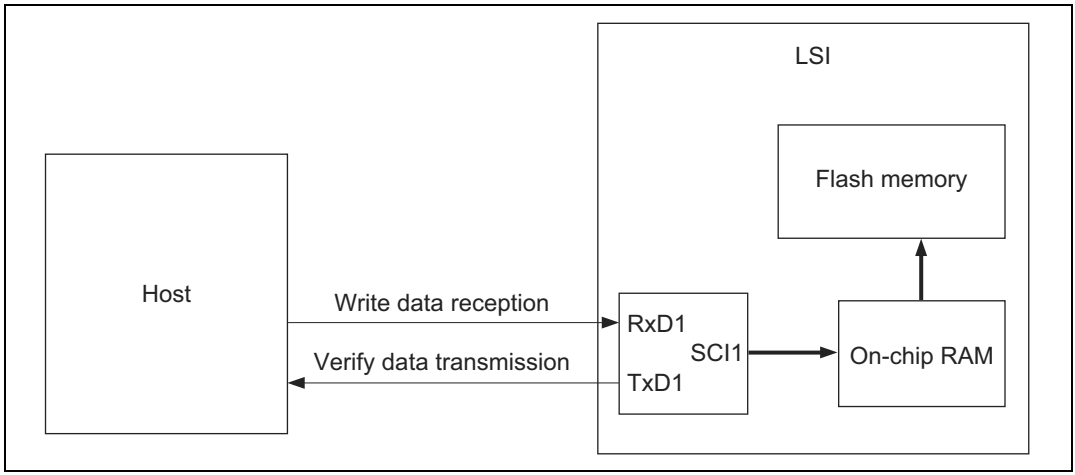


Figure 21C-7 System Configuration in Boot Mode

24.1.3 DC Characteristics

Table 24-2 lists the DC characteristics. Table 24-3 lists the permissible output currents.

Table 24-2 DC Characteristics

Conditions: V_{CC} = 4.5 V to 5.5 V, $PWMV_{CC}$ = 4.5 V to 5.5 V, AV_{CC} = 4.5 V to 5.5 V, V_{ref} = 4.5 V to AV_{CC}, V_{SS} = $PWMV_{SS}$ = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)*1 *6

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	$\overline{IRQ0}$ to $\overline{IRQ5}$	V_T^-	1.0	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$		
		$V_T^+ - V_T^-$	0.4	—	—		
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, FWE, MD2 to MD0	V_{IH}	$V_{CC} - 0.7$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$		
	Ports 1, 3, F		2.2	—	$V_{CC} + 0.3$		
	Ports A to E		$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$		
	Ports H, J		$PWMV_{CC} \times 0.8$	—	$PWMV_{CC} + 0.3$		
	HRxD0, HRxD1		2.2	—	$V_{CC} + 0.3$		
	Ports 4 and 9		$AV_{CC} \times 0.7$	—	$AV_{CC} + 0.3$		
Input low voltage	$\overline{RES}$, $\overline{STBY}$, NMI, FWE, MD2 to MD0	V_{IL}	–0.3	—	0.5	V	
	EXTAL		–0.3	—	0.8		
	Ports 1, 3, F		–0.3	—	0.8		
	Ports A to E		–0.3	—	$V_{CC} \times 0.2$		
	Ports H, J		–0.3	—	$PWMV_{CC} \times 0.2$		
	HRxD0, HRxD1		–0.3	—	$V_{CC} \times 0.2$		
	Ports 4, 9		–0.3	—	$AV_{CC} \times 0.2$		

(1) Clock Timing

Table 24-39 lists the clock timing

Table 24-39 Clock Timing

Conditions: V_{CC} = 4.5 V to 5.5 V, $PWMV_{CC}$ = 4.5 V to 5.5 V, AV_{CC} = 4.5 V to 5.5 V, V_{ref} = 4.5 V to AV_{CC}, V_{SS} = $PWMV_{SS}$ = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

		Condition			
		20MHz			
Item	**Symbol**	**Min.**	**Max.**	**Unit**	**Test Conditions**
Clock cycle time	t_{cyc}	50	250	ns	Figure 24-9
Clock high pulse width	t_{CH}	15	—	ns	
Clock low pulse width	t_{CL}	15	—	ns	
Clock rise time	t_{Cr}	—	10	ns	
Clock fall time	t_{Cf}	—	10	ns	
Clock oscillator settling time at reset (crystal)	t_{OSC1}	20	—	ms	Figure 24-10
Clock oscillator settling time in software standby (crystal)	t_{OSC2}	8	—	ms	Figure 23A-3 Figure 23B-3
External clock output stabilization delay time	t_{DEXT}	2	—	ms	Figure 24-10
32-kHz clock oscillation settling time	t_{OSC3}	—	2	s	
Subclock oscillator frequency	f_{SUB}	32.768		kHz	
Subclock (ϕ_{SUB}) cycle time	t_{SUB}	30.5		μs	

24.4.6 D/A Conversion Characteristics

Table 24-45 shows the D/A conversion characteristics.

Table 24-45 D/A Conversion Characteristics

Conditions: V_{CC} = 4.5 V to 5.5 V, $PWMV_{CC}$ = 4.5 V to 5.5 V, AV_{CC} = 4.5 V to 5.5 V, V_{ref} = 4.5 V to AV_{CC}, V_{SS} = $PWMV_{SS}$ = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

	Condition				
Item	**Min.**	**Typ.**	**Max.**	**Unit**	**Test Conditions**
Resolution	8	8	8	bits	
Conversion time	—	—	10	µs	20-pF capacitive load
Absolute accuracy	—	± 1.5	± 2.0	LSB	2-MΩ resistive load
	—	—	± 1.5	LSB	4-MΩ resistive load

TIOR0H—Timer I/O Control Register 0H H'FF12 TPU0

Bit	7	6	5	4	3	2	1	0
	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TGR0A I/O Control

0	0	0	0	TGR0A is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR0A is input capture register	Capture input source is TIOCA0 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 1/count clock	Input capture at TCNT1 count-up/ count-down

*: Don't care

TGR0B I/O Control

0	0	0	0	TGR0B is output compare register	Output disabled	
			1		Initial output is 0 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
	1	0	0		Output disabled	
			1		Initial output is 1 output	0 output at compare match
		1	0			1 output at compare match
			1			Toggle output at compare match
1	0	0	0	TGR0B is input capture register	Capture input source is TIOCB0 pin	Input capture at rising edge
			1			Input capture at falling edge
		1	*			Input capture at both edges
	1	*	*		Capture input source is channel 1/count clock	Input capture at TCNT1 count-up/ count-down*1

*: Don't care

Note: 1. When bits TPSC2 to TPSC0 in TCR1 are set to B'000 and ϕ/1 is used as the TCNT1 count clock, this setting is invalid and input capture is not generated.