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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2600
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SmartCard
Peripherals	Motor Control PWM, POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	128-BFQFP
Supplier Device Package	128-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2638f20v

Type	Instruction	Size*1	Function
Branch instructions	Bcc	—	Branches to a specified address if a specified condition is true. The branching conditions are listed below.

Mnemonic	Description	Condition
BRA(BT)	Always (true)	Always
BRN(BF)	Never (false)	Never
BHI	High	$C \vee Z = 0$
BLS	Low or same	$C \vee Z = 1$
BCC(BHS)	Carry clear (high or same)	$C = 0$
BCS(BLO)	Carry set (low)	$C = 1$
BNE	Not equal	$Z = 0$
BEQ	Equal	$Z = 1$
BVC	Overflow clear	$V = 0$
BVS	Overflow set	$V = 1$
BPL	Plus	$N = 0$
BMI	Minus	$N = 1$
BGE	Greater or equal	$N \oplus V = 0$
BLT	Less than	$N \oplus V = 1$
BGT	Greater than	$Z \vee (N \oplus V) = 0$
BLE	Less or equal	$Z \vee (N \oplus V) = 1$

	JMP	—	Branches unconditionally to a specified address.
	BSR	—	Branches to a subroutine at a specified address.
	JSR	—	Branches to a subroutine at a specified address.
	RTS	—	Returns from a subroutine

2.9 Basic Timing

2.9.1 Overview

The H8S/2600 CPU is driven by a system clock, denoted by the symbol ϕ. The period from one rising edge of ϕ to the next is referred to as a "state." The memory cycle or bus cycle consists of one, two, or three states. Different methods are used to access on-chip memory, on-chip supporting modules, and the external address space.

2.9.2 On-Chip Memory (ROM, RAM)

On-chip memory is accessed in one state. The data bus is 16 bits wide, permitting both byte and word transfer instruction. Figure 2-17 shows the on-chip memory access cycle. Figure 2-18 shows the pin states.

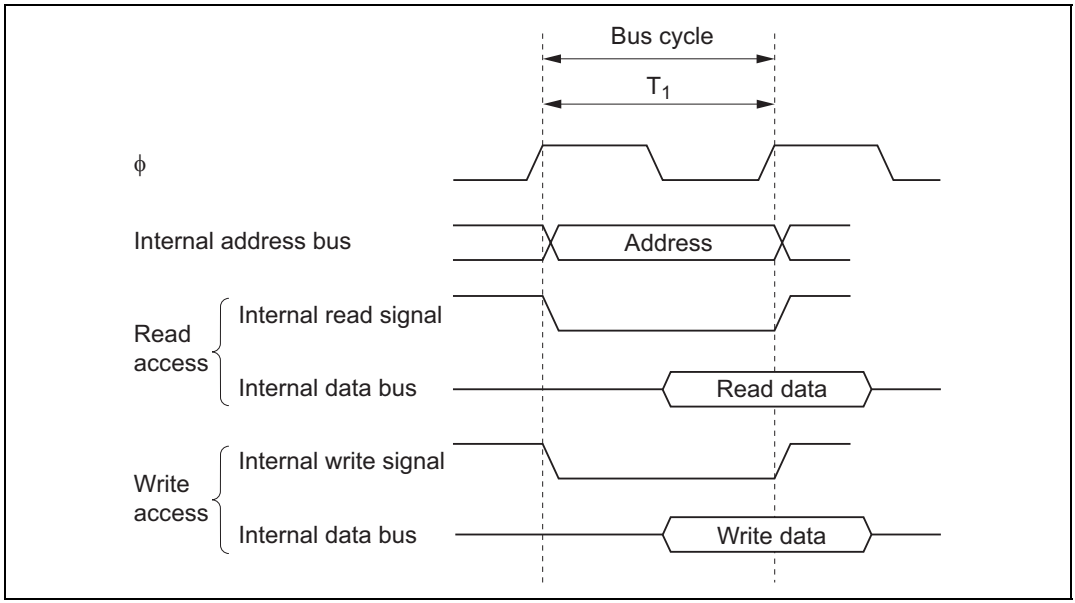


Figure 2-17 On-Chip Memory Access Cycle

3.3 Operating Mode Descriptions

3.3.1 Mode 4

The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM is disabled.

Ports 1, A, B, and C function as an address bus, ports D and E function as a data bus, and part of port F carries bus control signals.

The initial bus mode after a reset is 16 bits, with 16-bit access to all areas. However, note that if 8-bit access is designated by the bus controller for all areas, the bus mode switches to 8 bits.

3.3.2 Mode 5

The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM is disabled.

Ports 1, A, B, and C function as an address bus, port D function as a data bus, and part of port F carries bus control signals.

The initial bus mode after a reset is 8 bits, with 8-bit access to all areas. However, note that if 16-bit access is designated by the bus controller for any area, the bus mode switches to 16 bits and port E becomes a data bus.

3.3.3 Mode 6

The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM is enabled.

Ports 1, A, B, and C function as input port pins immediately after a reset. Address output can be performed by setting the corresponding DDR (data direction register) bits to 1.

Port D functions as a data bus, and part of port F carries bus control signals.

The initial bus mode after a reset is 8 bits, with 8-bit access to all areas. However, note that if 16-bit access is designated by the bus controller for any area, the bus mode switches to 16 bits and port E becomes a data bus.

3.5 Address Map in Each Operating Mode

An address map of the H8S/2636 is shown in figure 3-1.

An address map of the H8S/2638 and H8S/2639 is shown in figure 3-2.

An address map of the H8S/2630 is shown in figure 3-3.

An address map of the H8S/2635 is shown in figure 3-4.

An address map of the H8S/2634 is shown in figure 3-5.

The address space is 16 Mbytes in modes 4 to 7 (advanced modes).

The address space is divided into eight areas for modes 4 to 7. For details, see section 7, Bus Controller.

Example of Non-Overlapping Pulse Output (Example of Four-Phase Complementary Non-Overlapping Output): Figure 11-7 shows an example in which pulse output is used for four-phase complementary non-overlapping pulse output.

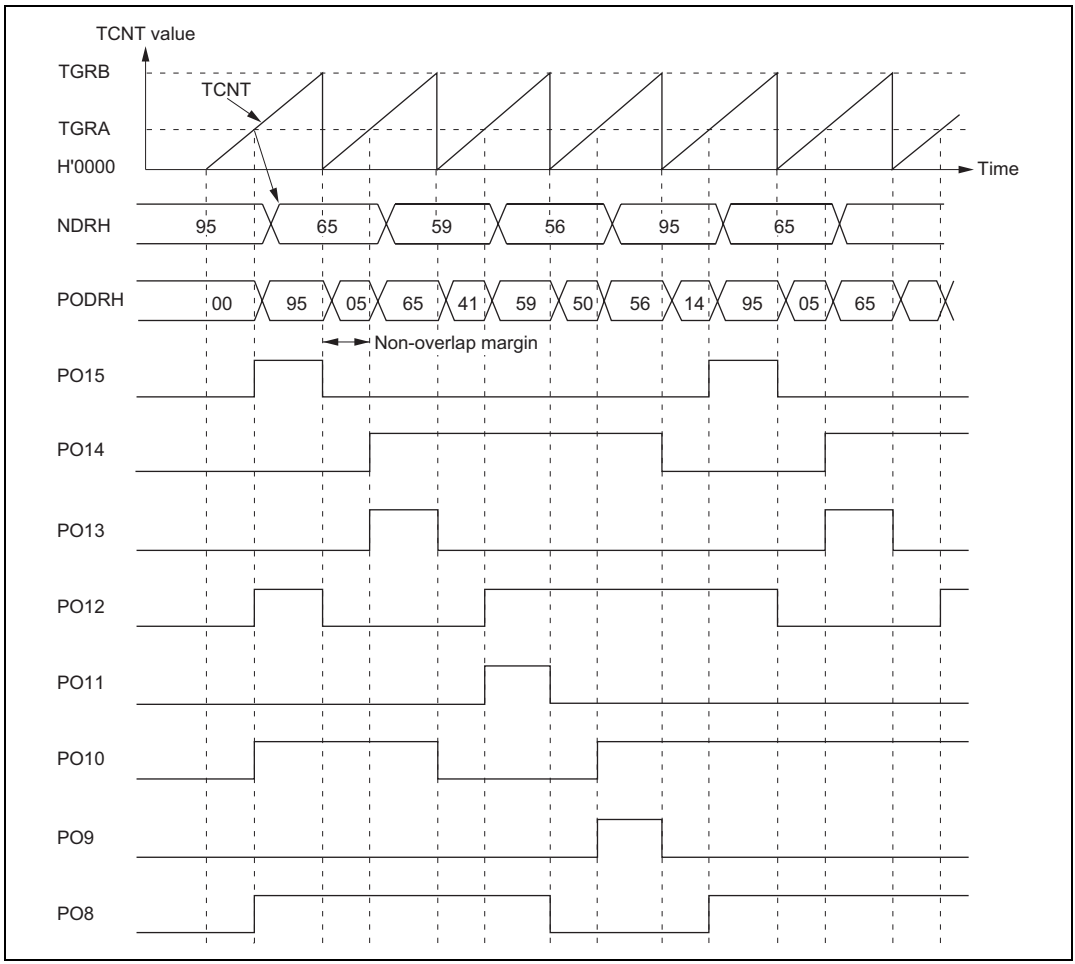


Figure 11-7 Non-Overlapping Pulse Output Example (Four-Phase Complementary)

Bit 6—Receive Interrupt Enable (RIE): Enables or disables receive data full interrupt (RXI) request and receive error interrupt (ERI) request generation when serial receive data is transferred from RSR to RDR and the RDRF flag in SSR is set to 1.

Bit 6

RIE	Description
0	Receive data full interrupt (RXI) request and receive error interrupt (ERI) request disabled* (Initial value)
1	Receive data full interrupt (RXI) request and receive error interrupt (ERI) request enabled

Note:* RXI and ERI interrupt request cancellation can be performed by reading 1 from the RDRF flag, or the FER, PER, or ORER flag, then clearing the flag to 0, or clearing the RIE bit to 0.

Bit 5—Transmit Enable (TE): Enables or disables the start of serial transmission by the SCI.

Bit 5

TE	Description
0	Transmission disabled*1 (Initial value)
1	Transmission enabled*2

Notes: 1. The TDRE flag in SSR is fixed at 1.
2. In this state, serial transmission is started when transmit data is written to TDR and the TDRE flag in SSR is cleared to 0.
SMR setting must be performed to decide the transfer format before setting the TE bit to 1.

Bit 4—Receive Enable (RE): Enables or disables the start of serial reception by the SCI.

Bit 4

RE	Description
0	Reception disabled*1 (Initial value)
1	Reception enabled*2

Notes: 1. Clearing the RE bit to 0 does not affect the RDRF, FER, PER, and ORER flags, which retain their states.
2. Serial reception is started in this state when a start bit is detected in asynchronous mode or serial clock input is detected in clocked synchronous mode.
SMR setting must be performed to decide the transfer format before setting the RE bit to 1.

	φ = 6 MHz			φ = 6.144 MHz			φ = 7.3728 MHz			φ = 8 MHz		
Bit Rate (bit/s)	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**
110	2	106	–0.44	2	108	0.08	2	130	–0.07	2	141	0.03
150	2	77	0.16	2	79	0.00	2	95	0.00	2	103	0.16
300	1	155	0.16	1	159	0.00	1	191	0.00	1	207	0.16
600	1	77	0.16	1	79	0.00	1	95	0.00	1	103	0.16
1200	0	155	0.16	0	159	0.00	0	191	0.00	0	207	0.16
2400	0	77	0.16	0	79	0.00	0	95	0.00	0	103	0.16
4800	0	38	0.16	0	39	0.00	0	47	0.00	0	51	0.16
9600	0	19	–2.34	0	19	0.00	0	23	0.00	0	25	0.16
19200	0	9	–2.34	0	9	0.00	0	11	0.00	0	12	0.16
31250	0	5	0.00	0	5	2.40	—	—	—	0	7	0.00
38400	0	4	–2.34	0	4	0.00	0	5	0.00	—	—	—

	φ = 9.8304 MHz			φ = 10 MHz			φ = 12 MHz			φ = 12.288 MHz		
Bit Rate (bit/s)	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**
110	2	174	–0.26	2	177	–0.25	2	212	0.03	2	217	0.08
150	2	127	0.00	2	129	0.16	2	155	0.16	2	159	0.00
300	1	255	0.00	2	64	0.16	2	77	0.16	2	79	0.00
600	1	127	0.00	1	129	0.16	1	155	0.16	1	159	0.00
1200	0	255	0.00	1	64	0.16	1	77	0.16	1	79	0.00
2400	0	127	0.00	0	129	0.16	0	155	0.16	0	159	0.00
4800	0	63	0.00	0	64	0.16	0	77	0.16	0	79	0.00
9600	0	31	0.00	0	32	–1.36	0	38	0.16	0	39	0.00
19200	0	15	0.00	0	15	1.73	0	19	–2.34	0	19	0.00
31250	0	9	–1.70	0	9	0.00	0	11	0.00	0	11	2.40
38400	0	7	0.00	0	7	1.73	0	9	–2.34	0	9	0.00

14.2.4 Serial Control Register (SCR)

Bit	:	7	6	5	4	3	2	1	0
		TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

In smart card interface mode, the function of bits 1 and 0 of SCR changes when bit 7 of the serial mode register (SMR) is set to 1.

Bits 7 to 2—Operate in the same way as for the normal SCI.

For details, see section 13.2.6, Serial Control Register (SCR).

Bits 1 and 0—Clock Enable 1 and 0 (CKE1, CKE0): These bits are used to select the SCI clock source and enable or disable clock output from the SCK pin.

In smart card interface mode, in addition to the normal switching between clock output enabling and disabling, the clock output can be specified as to be fixed high or low.

SCMR	SMR	SCR Setting		
SMIF	**C/$\overline{A}$, GM**	**CKE1**	**CKE0**	**SCK Pin Function**
0	See the SCI			
1	0	0	0	Operates as port I/O pin
1	0	0	1	Outputs clock as SCK output pin
1	1	0	0	Operates as SCK output pin, with output fixed low
1	1	0	1	Outputs clock as SCK output pin
1	1	1	0	Operates as SCK output pin, with output fixed high
1	1	1	1	Outputs clock as SCK output pin

16.2.8 Abort Acknowledge Register (ABACK)

The abort acknowledge register (ABACK) is a 16-bit readable/writable register containing status flags that indicate normal cancellation (aborting) of a mailbox (buffer) transmit messages.

ABACK

Bit:	15	14	13	12	11	10	9	8
	ABACK7	ABACK6	ABACK5	ABACK4	ABACK3	ABACK2	ABACK1	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R

Bit:	7	6	5	4	3	2	1	0
	ABACK15	ABACK14	ABACK13	ABACK12	ABACK11	ABACK10	ABACK9	ABACK8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: * Only a write of 1 is permitted, to clear the flag.

Bits 15 to 9 and 7 to 0—Abort Acknowledge Register (ABACK7 to ABACK1, ABACK15 to ABACK8): These bits indicate that a transmit message in the corresponding mailbox has been canceled (aborted) normally.

Bit y: ABACKx	Description
0	[Clearing condition] • Writing 1 (Initial value)
1	Completion of transmit message cancellation for corresponding mailbox

(x = 15 to 1, y = 15 to 9 and 7 to 0)

Bit 8—Reserved: This bit always reads 0. The write value should always be 0.

16.2.17 Local Acceptance Filter Masks (LAFML, LAFMH)

The local acceptance filter masks (LAFML, LAFMH) are 16-bit readable/writable registers that filter receive messages to be stored in the receive-only mailbox (MC0, MD0) according to the identifier. In these registers, consist of LAFMH15: MSB to LAFMH5: LSB are 11 standard/extended identifier bits, and LAFMH1: MSB to LAFML0: LSB are 18 extended identifier bits.

LAFML

Bit:	15	14	13	12	11	10	9	8
	LAFML7	LAFML6	LAFML5	LAFML4	LAFML3	LAFML2	LAFML1	LAFML0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

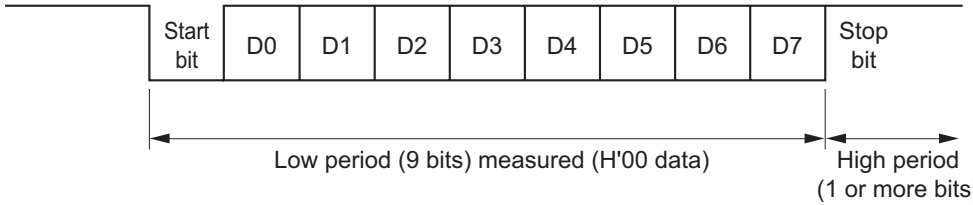
Bit:	7	6	5	4	3	2	1	0
	LAFML15	LAFML14	LAFML13	LAFML12	LAFML11	LAFML10	LAFML9	LAFML8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LAFMH

Bit:	15	14	13	12	11	10	9	8
	LAFMH7	LAFMH6	LAFMH5	—	—	—	LAFMH1	LAFMH0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R	R	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	LAFMH15	LAFMH14	LAFMH13	LAFMH12	LAFMH11	LAFMH10	LAFMH9	LAFMH8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Automatic SCI Bit Rate Adjustment



When boot mode is initiated, the LSI measures the low period of the asynchronous SCI communication data (H'00) transmitted continuously from the host. The SCI transmit/receive format should be set as follows: 8-bit data, 1 stop bit, no parity. The LSI calculates the bit rate of the transmission from the host from the measured low period, and transmits one H'00 byte to the host to indicate the end of bit rate adjustment. The host should confirm that this adjustment end indication (H'00) has been received normally, and transmit one H'55 byte to the LSI. If reception cannot be performed normally, initiate boot mode again (reset), and repeat the above operations. Depending on the host's transmission bit rate and the LSI's system clock frequency, there will be a discrepancy between the bit rates of the host and the LSI. Set the host transfer bit rate at 4,800, 9,600 or 19,200 bps to operate the SCI properly.

Table 21A-10 shows host transfer bit rates and system clock frequencies for which automatic adjustment of the LSI bit rate is possible. The boot program should be executed within this system clock range.

Table 21A-10 System Clock Frequencies for which Automatic Adjustment of LSI Bit Rate Is Possible

Host Bit Rate	System Clock Frequency for which Automatic Adjustment of LSI Bit Rate Is Possible
4,800 bps	4 to 20 MHz
9,600 bps	8 to 20 HHz
19,200 bps	16 to 20 MHz

Note: The system clock frequency used in boot mode is generated by an external crystal oscillator element. PLL frequency multiplication is not used.

External Clock

Table 22A-4 and figure 22A-7 show the input conditions for the external clock.

Table 22A-4 External Clock Input Conditions

		V_{CC} = 5.0 V ±10%			
Item	**Symbol**	**Min.**	**Max.**	**Unit**	**Test Conditions**
External clock input low pulse width	t_{EXL}	15	—	ns	Figure 22A-7
External clock input high pulse width	t_{EXH}	15	—	ns	
External clock rise time	t_{EXr}	—	5	ns	
External clock fall time	t_{EXf}	—	5	ns	

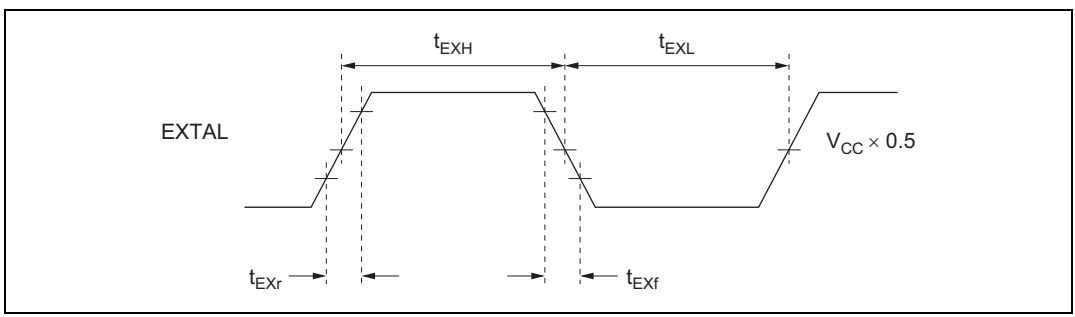


Figure 22A-7 External Clock Input Timing

ABACK0—Abort Acknowledge Register **H'F80C** **HCAN0**
ABACK1—Abort Acknowledge Register **H'FA0C** **HCAN1***

Bit	15	14	13	12	11	10	9	8
	ABACK7	ABACK6	ABACK5	ABACK4	ABACK3	ABACK2	ABACK1	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit	7	6	5	4	3	2	1	0
	ABACK15	ABACK14	ABACK13	ABACK12	ABACK11	ABACK10	ABACK9	ABACK8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Abort Acknowledge Register

0	[Clearing condition] • Writing 1
1	Completion of transmit message cancellation for corresponding mailbox

Note: * This register is not available in the H8S/2635 Group.

RXPR0—Receive Complete Register **H'F80E** **HCAN0**
RXPR1—Receive Complete Register **H'FA0E** **HCAN1***

Bit	15	14	13	12	11	10	9	8
	RXPR7	RXPR6	RXPR5	RXPR4	RXPR3	RXPR2	RXPR1	RXPR0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
	RXPR15	RXPR14	RXPR13	RXPR12	RXPR11	RXPR10	RXPR9	RXPR8
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Receive Complete Register

0	[Clearing condition] • Writing 1
1	Completion of message (data frame or remote frame) reception in corresponding mailbox

Note: * This register is not available in the H8S/2635 Group.

MC0[7]

Bit	7	6	5	4	3	2	1	0
	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Extended Identifier
Set the identifier (extended identifier) of data frames and remote frames

MC0[8]

Bit	7	6	5	4	3	2	1	0
	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Extended Identifier
Set the identifier (extended identifier) of data frames and remote frames

MC4[7]

Bit	7	6	5	4	3	2	1	0
	EXD_ID7	EXD_ID6	EXD_ID5	EXD_ID4	EXD_ID3	EXD_ID2	EXD_ID1	EXD_ID0
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Extended Identifier
Set the identifier (extended identifier) of data frames and remote frames

MC4[8]

Bit	7	6	5	4	3	2	1	0
	EXD_ID15	EXD_ID14	EXD_ID13	EXD_ID12	EXD_ID11	EXD_ID10	EXD_ID9	EXD_ID8
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Extended Identifier
Set the identifier (extended identifier) of data frames and remote frames

MD0[1]—Message Data 0[1]	**H'F8B0**	**HCAN0**
MD0[2]—Message Data 0[2]	**H'F8B1**	**HCAN0**
MD0[3]—Message Data 0[3]	**H'F8B2**	**HCAN0**
MD0[4]—Message Data 0[4]	**H'F8B3**	**HCAN0**
MD0[5]—Message Data 0[5]	**H'F8B4**	**HCAN0**
MD0[6]—Message Data 0[6]	**H'F8B5**	**HCAN0**
MD0[7]—Message Data 0[7]	**H'F8B6**	**HCAN0**
MD0[8]—Message Data 0[8]	**H'F8B7**	**HCAN0**

MDx[1]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MDx[2]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MDx[3]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MDx[4]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MDx[5]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MDx[6]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MDx[7]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MDx[8]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

*: Undefined
x = 0 to 15

PWBFR2A—PWM Buffer Register 2A **H'FC18** **PWM2**
PWBFR2B—PWM Buffer Register 2B **H'FC1A** **PWM2**
PWBFR2C—PWM Buffer Register 2C **H'FC1C** **PWM2**
PWBFR2D—PWM Buffer Register 2D **H'FC1E** **PWM2**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	TDS	—	—	DT9	DT8	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0
Initial value	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0
Read/Write	—	—	—	R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Duty
Bits 9 to 0 compromise the data transferred to bits 9 to 0 in PWDTR2

Transfer Destination Select
Selects the PWDTR2 register to which data is to be transferred

Register	TDS	Description
PWBFR2A	0	PWDTR2A selected
	1	PWDTR2E selected
PWBFR2B	0	PWDTR2B selected
	1	PWDTR2F selected
PWBFR2C	0	PWDTR2C selected
	1	PWDTR2G selected
PWBFR2D	0	PWDTR2D selected
	1	PWDTR2H selected

Note: When a PWCYR2 compare match occurs, data is transferred from PWBFR2A to PWDTR2A or PWDTR2E, from PWBFR2B to PWDTR2B or PWDTR2F, from PWBFR2C to PWDTR2C or PWDTR2G, and from PWBFR2D to PWDTR2D or PWDTR2H.

PHDDR—Port H Data Direction Register **H'FC20** **Port**

Bit	7	6	5	4	3	2	1	0
	PH7DDR	PH6DDR	PH5DDR	PH4DDR	PH3DDR	PH2DDR	PH1DDR	PH0DDR
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

C.5 Port A Block Diagram

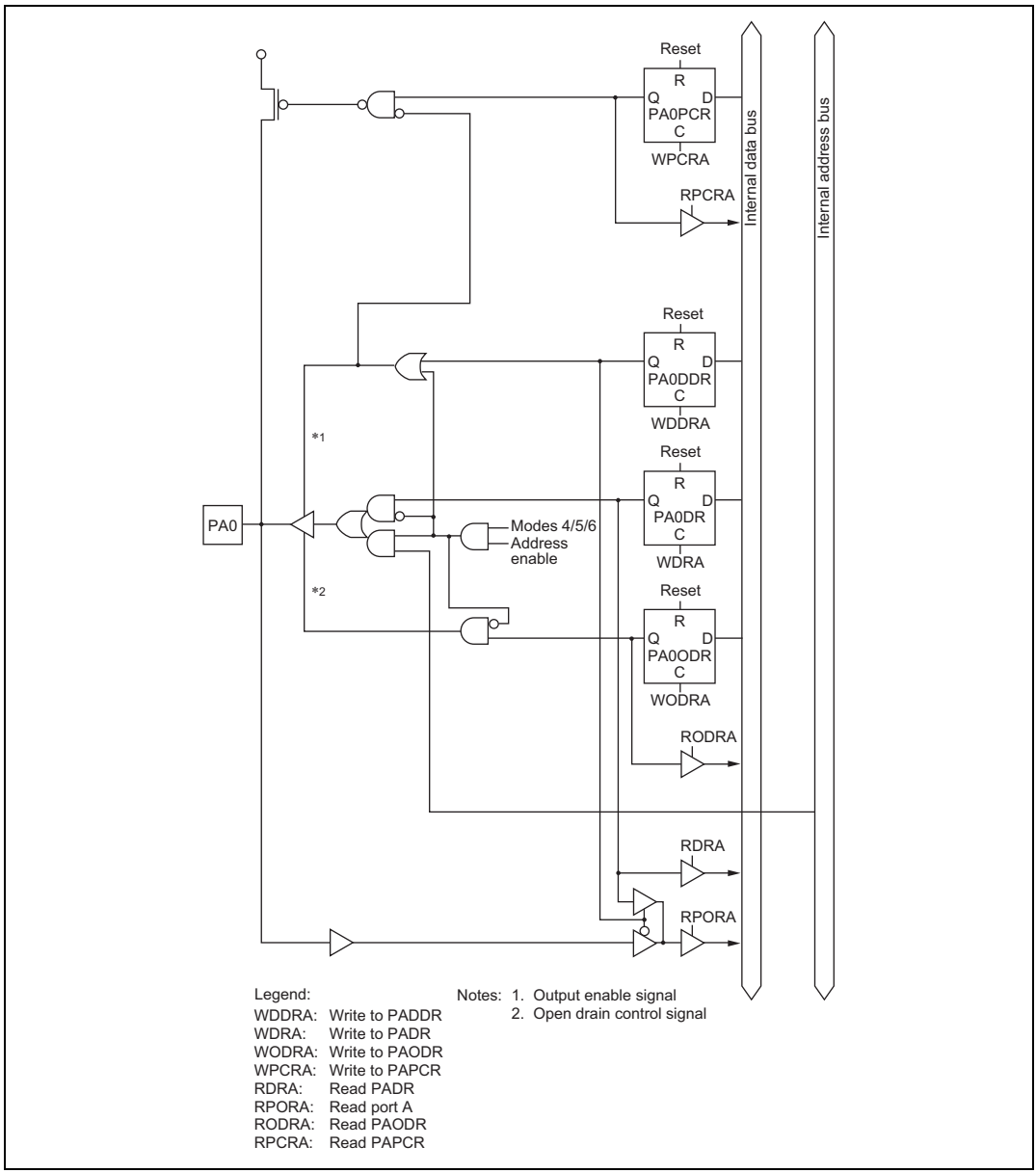


Figure C-5 (a) Port A Block Diagram (Pin PA0)