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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2600
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SmartCard
Peripherals	Motor Control PWM, POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	128-BFQFP
Supplier Device Package	128-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2638uf20v

(4) Condition Field: Specifies the branching condition of Bcc instructions.

Figure 2-12 shows examples of instruction formats.

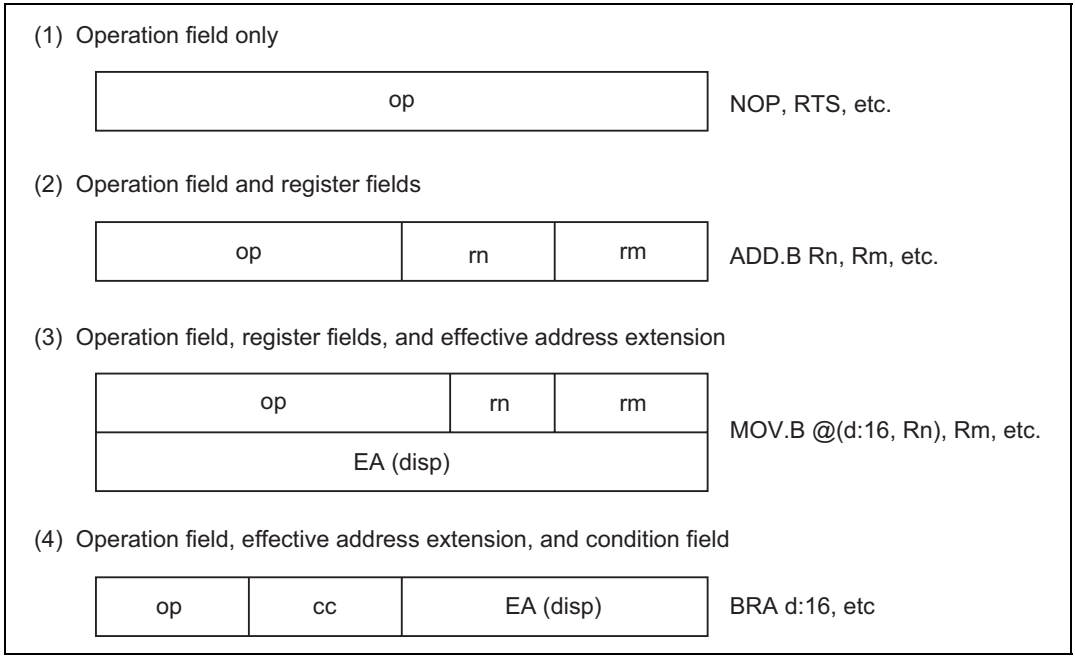


Figure 2-12 Instruction Formats (Examples)

3.5 Address Map in Each Operating Mode

An address map of the H8S/2636 is shown in figure 3-1.

An address map of the H8S/2638 and H8S/2639 is shown in figure 3-2.

An address map of the H8S/2630 is shown in figure 3-3.

An address map of the H8S/2635 is shown in figure 3-4.

An address map of the H8S/2634 is shown in figure 3-5.

The address space is 16 Mbytes in modes 4 to 7 (advanced modes).

The address space is divided into eight areas for modes 4 to 7. For details, see section 7, Bus Controller.

Figure 8-3 shows a block diagram of activation source control. For details see section 5, Interrupt Controller.

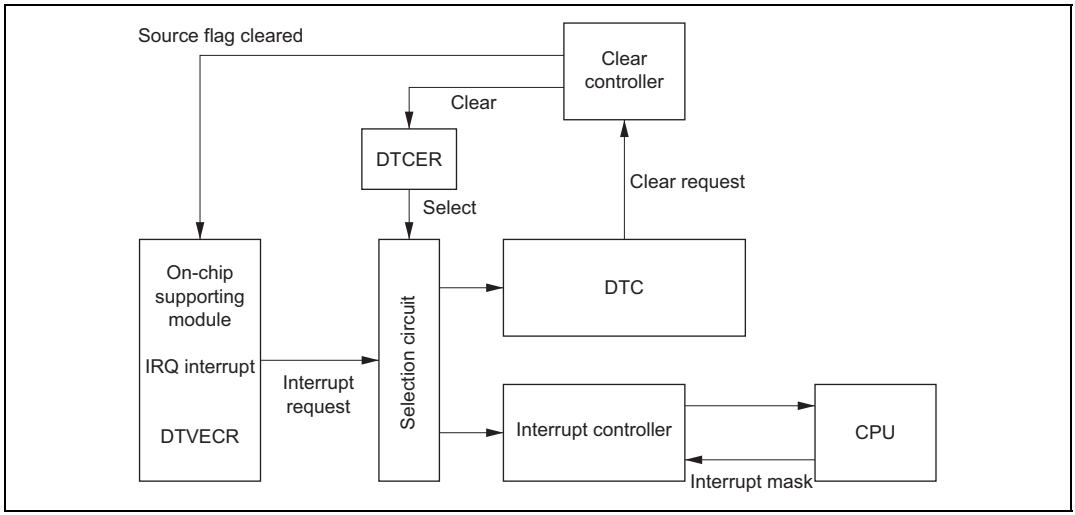


Figure 8-3 Block Diagram of DTC Activation Source Control

When an interrupt has been designated a DTC activation source, existing CPU mask level and interrupt controller priorities have no effect. If there is more than one activation source at the same time, the DTC operates in accordance with the default priorities.

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address	DTCE*1	Priority
I^2CI0 (1-byte transmission/ reception completed)*2	I^2C channel 0 (option)	100	H'04C8	DTCEF1	High
I^2CI1 (1-byte transmission/ reception completed)*2	I^2C channel 1 (option)	102	H'04CC	DTCEF0	
CMI1 (PWCYR1 compare match)	PWM	104	H'04D0	DTCEG7	
CMI2 (PWCYR2 compare match)		105	H'04D2	DTCEG6	
Reserved	—	106	H'04D4	—	
RM0 (HCAN1 mail box 0)	HCAN1	107	H'04D6	DTCEG4	
Reserved	—	108	H'04D8	—	
RM0 (HCAN0 mail box 0)	HCAN0	109	H'04DA	DTCEG2	
Reserved	—	110 to 124	H'04DC to H'04F8	—	Low

Notes: 1. DTCE bits with no corresponding interrupt are reserved, and should be written with 0.
2. I^2C bus interface is available as an option in the H8S/2638, H8S/2639, and H8S/2630. These bits become reserved bits when this optional feature is not used or in the H8S/2636.

8.3.6 Repeat Mode

In repeat mode, one operation transfers one byte or one word of data.

From 1 to 256 transfers can be specified. Once the specified number of transfers have ended, the initial state of the transfer counter and the address register specified as the repeat area is restored, and transfer is repeated. In repeat mode the transfer counter value does not reach H'00, and therefore CPU interrupts cannot be requested when DISEL = 0.

Table 8-6 lists the register information in repeat mode and figure 8-7 shows memory mapping in repeat mode.

Table 8-6 Register Information in Repeat Mode

Name	Abbreviation	Function
DTC source address register	SAR	Designates source address
DTC destination address register	DAR	Designates destination address
DTC transfer count register AH	CRAH	Holds number of transfers
DTC transfer count register AL	CRAL	Designates transfer count
DTC transfer count register B	CRB	Not used

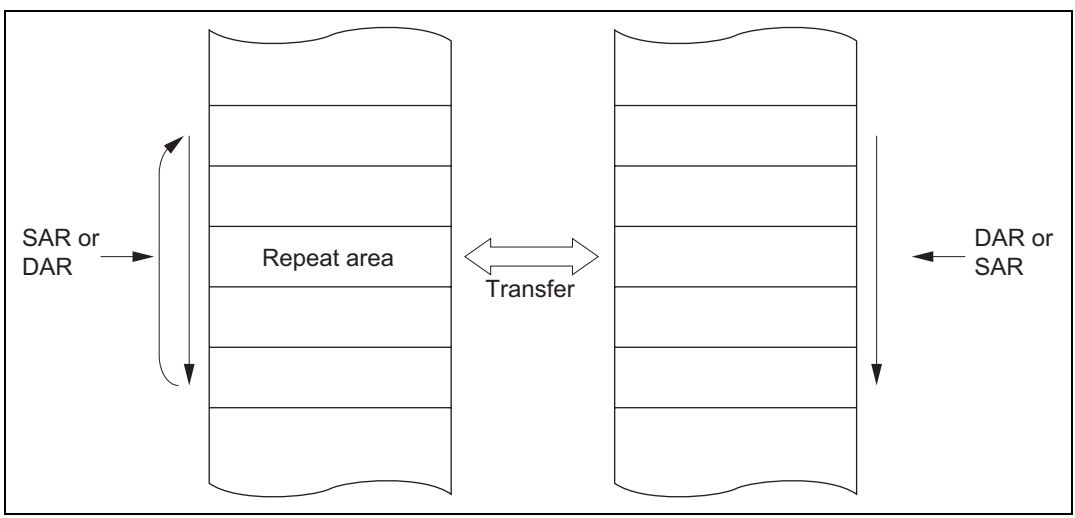


Figure 8-7 Memory Mapping in Repeat Mode

9.6.3 Pin Functions

Port A pins also function as SCI input/output pins (TxD2, RxD2, SCK2) and address bus output pins (A19 to A16). Port A pin functions are shown in table 9-9.

Table 9-9 Port A Pin Functions

Pin	Selection Method and Pin Functions
PA3/A19/SCK2	The pin function is switched as shown below according to the operating mode, bits AE3 to AE0 in PFCR, bit C/$\overline{A}$ in SMR and bits CKE0 and CKE1 in SCR of SCI2, and bit PA3DDR.

Operating mode	Modes 4 to 6					
AE3 to AE0	B'0000 to B'1011					B'1100 to B'1111
CKE1	0				1	—
C/$\overline{A}$	0			1	—	—
CKE0	0		1	—	—	—
PA3DDR	0	1	—	—	—	—
Pin function	PA3 input	PA3 output	SCK2 output	SCK2 output	SCK2 input	A19 output

Operating mode	Mode 7				
CKE1	0				1
C/$\overline{A}$	0			1	—
CKE0	0		1	—	—
PA3DDR	0	1	—	—	—
Pin function	PA3 input	PA3 output	SCK2 output	SCK2 output	SCK2 input

9.13 Port J

9.13.1 Overview

Port J is an 8-bit I/O port. Port J pins also function as motor control PWM timer output pins (PWM2A to PWM2H).

Figure 9-23 shows the port J pin configuration.

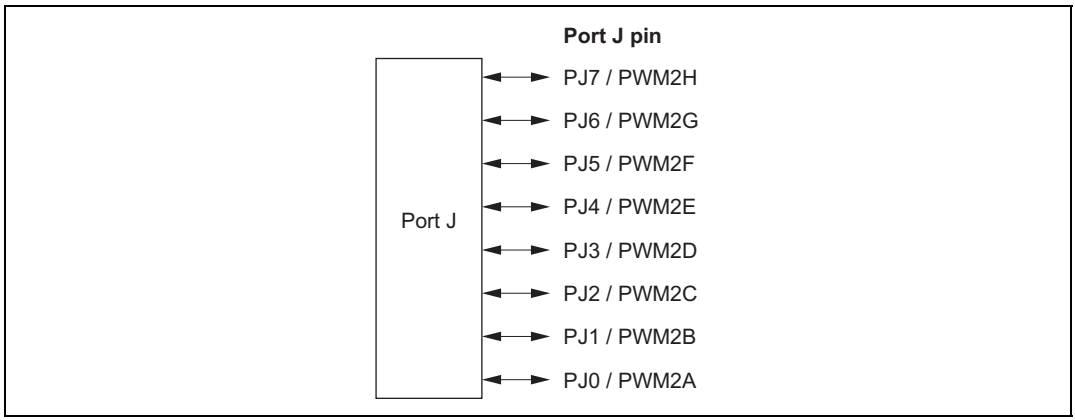


Figure 9-23 Port J Pin Functions

10.5 Interrupts

10.5.1 Interrupt Sources and Priorities

There are three kinds of TPU interrupt source: TGR input capture/compare match, TCNT overflow, and TCNT underflow. Each interrupt source has its own status flag and enable/disabled bit, allowing generation of interrupt request signals to be enabled or disabled individually.

When an interrupt request is generated, the corresponding status flag in TSR is set to 1. If the corresponding enable/disable bit in TIER is set to 1 at this time, an interrupt is requested. The interrupt request is cleared by clearing the status flag to 0.

Relative channel priorities can be changed by the interrupt controller, but the priority order within a channel is fixed. For details, see section 5, Interrupt Controller.

Table 10-13 lists the TPU interrupt sources.

11.1.4 Registers

Table 11-2 summarizes the PPG registers.

Table 11-2 PPG Registers

Name	Abbreviation	R/W	Initial Value	Address*1
PPG output control register	PCR	R/W	H'FF	H'FE26
PPG output mode register	PMR	R/W	H'F0	H'FE27
Next data enable register H	NDERH	R/W	H'00	H'FE28
Next data enable register L*4	NDERL	R/W	H'00	H'FE29
Output data register H	PODRH	R/(W)*2	H'00	H'FE2A
Output data register L*4	PODRL	R/(W)*2	H'00	H'FE2B
Next data register H	NDRH	R/W	H'00	H'FE2C*3 H'FE2E
Next data register L*4	NDRL	R/W	H'00	H'FE2D*3 H'FE2F
Port 1 data direction register	P1DDR	W	H'00	H'FE30
Module stop control register A	MSTPCRA	R/W	H'3F	H'FDE8

Notes: 1. Lower 16 bits of the address.
2. Bits used for pulse output cannot be written to.
3. When the same output trigger is selected for pulse output groups 2 and 3 by the PCR setting, the NDRH address is H'FE2C. When the output triggers are different, the NDRH address is H'FE2E for group 2 and H'FE2C for group 3.

   Similarly, when the same output trigger is selected for pulse output groups 0 and 1 by the PCR setting, the NDRL address is H'FE2D. When the output triggers are different, the NDRL address is H'FE2F for group 0 and H'FE2D for group 1.
4. The chip has no pins corresponding to pulse output groups 0 and 1.

- Reception

  Receive operation should be stopped (by clearing RE to 0) before making a module stop mode, software standby mode, watch mode, subactive mode, or subsleep mode transition. RSR, RDR, and SSR are reset. If a transition is made without stopping operation, the data being received will be invalid.

  To continue receiving without changing the reception mode after the relevant mode is cleared, set RE to 1 before starting reception. To receive with a different receive mode, the procedure must be started again from initialization.

  Figure 13-26 shows a sample flowchart for mode transition during reception.

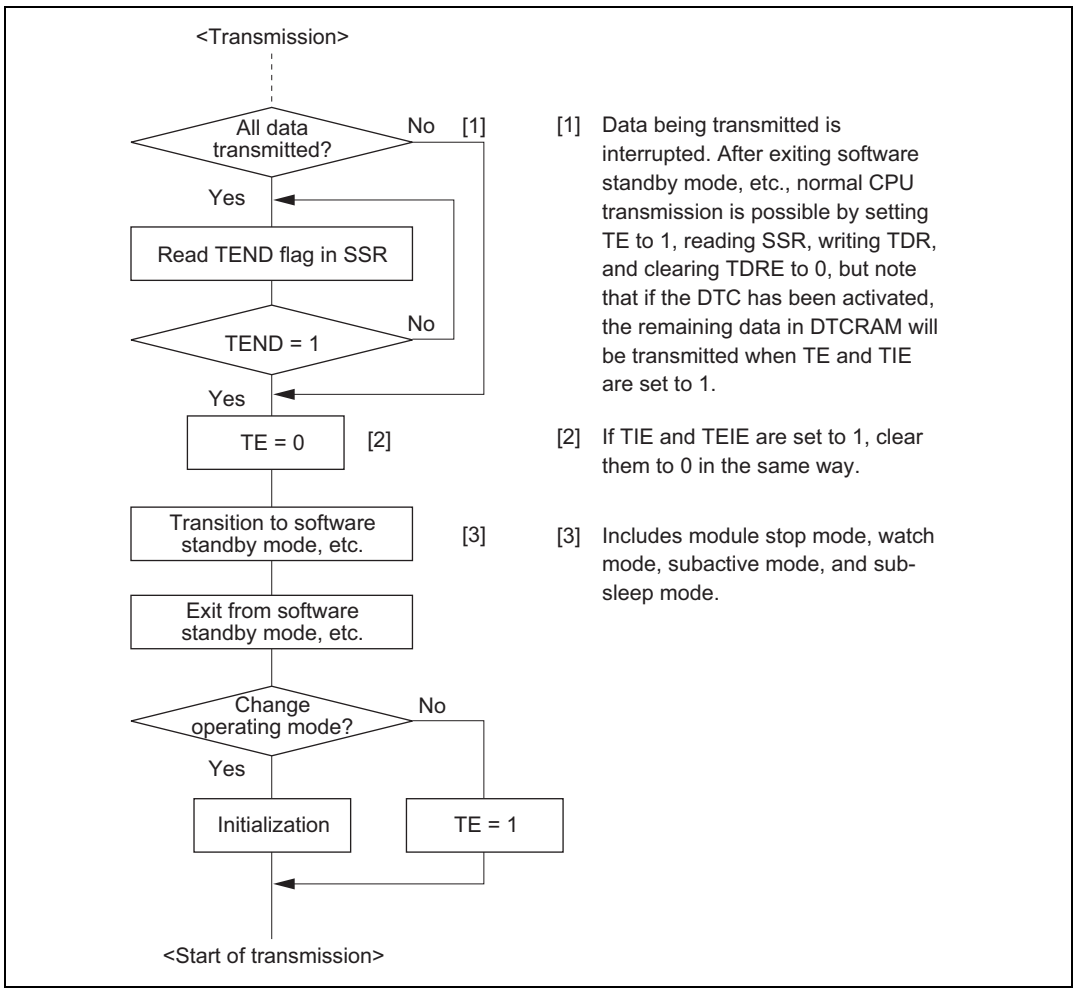


Figure 13-23 Sample Flowchart for Mode Transition during Transmission

In a receive operation, an RXI interrupt request is generated when the RDRF flag in SSR is set to 1. If the RXI request is designated beforehand as a DTC activation source, the DTC will be activated by the RXI request, and transfer of the receive data will be carried out. The RDRF flag is cleared to 0 automatically when data transfer is performed by the DTC. If an error occurs, an error flag is set but the RDRF flag is not. Consequently, the DTC is not activated, but instead, an ERI interrupt request is sent to the CPU. Therefore, the error flag should be cleared.

Notes: For block transfer mode, see section 13.4, SCI Interrupts.
* The DTC is not implemented in the H8S/2635 Group.

14.3.7 Operation in GSM Mode

Switching the Mode: When switching between smart card interface mode and software standby mode, the following switching procedure should be followed in order to maintain the clock duty.

- When changing from smart card interface mode to software standby mode

[1] Set the data register (DR) and data direction register (DDR) corresponding to the SCK pin to the value for the fixed output state in software standby mode.

[2] Write 0 to the TE bit and RE bit in the serial control register (SCR) to halt transmit/receive operation. At the same time, set the CKE1 bit to the value for the fixed output state in software standby mode.

[3] Write 0 to the CKE0 bit in SCR to halt the clock.

[4] Wait for one serial clock period.
During this interval, clock output is fixed at the specified level, with the duty preserved.

[5] Make the transition to the software standby state.

- When returning to smart card interface mode from software standby mode

[6] Exit the software standby state.

[7] Write 1 to the CKE0 bit in SCR and output the clock. Signal generation is started with the normal duty.

HCAN sleep mode is entered by setting the HCAN sleep mode bit (MCR5) to 1 in the master control register (MCR). If the CAN bus is operating, the transition to HCAN sleep mode is delayed until the bus becomes idle.

Either of the following methods of clearing HCAN sleep mode can be selected by making a setting in the MCR7 bit.

1. Clearing by software
2. Clearing by CAN bus operation

Eleven recessive bits must be received after HCAN sleep mode is cleared before CAN bus communication is enabled again.

Clearing by software: HCAN sleep mode is cleared by writing a 0 to MCR5 from the CPU.

Clearing by CAN bus operation: Clearing by CAN bus operation occurs automatically when the CAN bus performs an operation and this change is detected. In this case, the first message is not received in the mailbox, and normal reception starts from the next message. When a change is detected on the CAN bus in HCAN sleep mode, the bus operation interrupt flag (IRR12) is set in the interrupt register (IRR). If the bus interrupt mask (IMR12) in the interrupt mask register (IMR) is set to the interrupt enable value at this time, an interrupt can be sent to the CPU.

17.2.4 Module Stop Control Register A (MSTPCRA)

Bit	:	7	6	5	4	3	2	1	0
		MSTPA7	MSTPA6	MSTPA5	MSTPA4	MSTPA3	MSTPA2	MSTPA1	MSTPA0
Initial value	:	0	0	1	1	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MSTPCR is an 8-bit readable/writable register that performs module stop mode control.

When the MSTPA1 bit in MSTPCR is set to 1, A/D converter operation stops at the end of the bus cycle and a transition is made to module stop mode. Registers cannot be read or written to in module stop mode. For details, see section 23A.5, 23B.5, Module Stop Mode.

MSTPCRA is initialized to H'3F by a reset and in hardware standby mode. It is not initialized by a reset and in software standby mode.

Bit 1—Module Stop (MSTPA1): Specifies the A/D converter module stop mode.

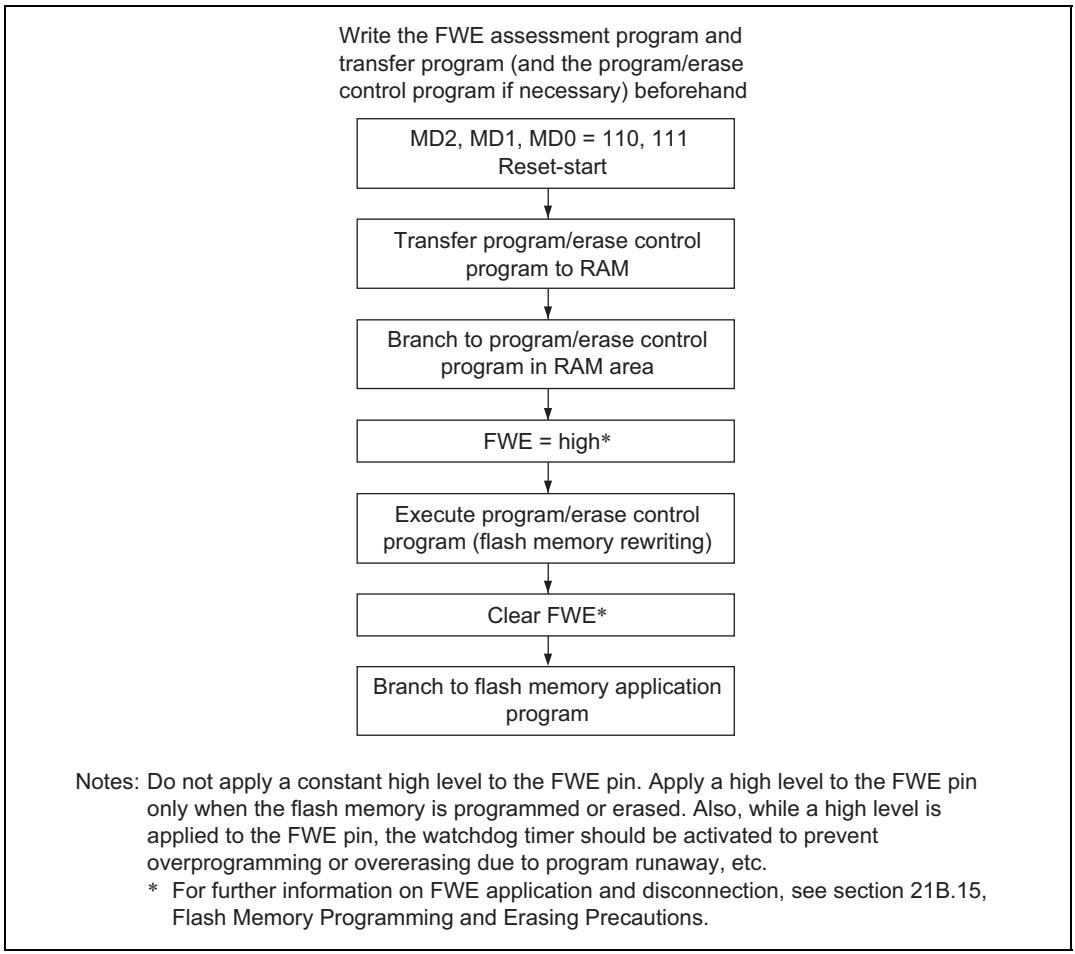
Bit 1

MSTPA1	Description	
0	A/D converter module stop mode cleared	
1	A/D converter module stop mode set	(Initial value)

To select user program mode, select a mode that enables the on-chip flash memory (mode 6 or 7), and apply a high level to the FWE pin. In this mode, on-chip supporting modules other than flash memory operate as they normally would in modes 6 and 7.

The flash memory itself cannot be read while the SWE bit is set to 1 to perform programming or erasing, so the control program that performs programming and erasing should be run in on-chip RAM or external memory. If the program is to be located in external memory, the instruction for writing to flash memory, and the following instruction, should be placed in on-chip RAM.

Figure 21C-10 shows the procedure for executing the program/erase control program when transferred to on-chip RAM.



Notes: Do not apply a constant high level to the FWE pin. Apply a high level to the FWE pin only when the flash memory is programmed or erased. Also, while a high level is applied to the FWE pin, the watchdog timer should be activated to prevent overprogramming or overerasing due to program runaway, etc.

* For further information on FWE application and disconnection, see section 21B.15, Flash Memory Programming and Erasing Precautions.

Figure 21C-10 User Program Mode Execution Procedure

Mnemonic		Operand Size	Addressing Mode/ Instruction Length (Bytes)									Operation	Branching Condition	Condition Code						No. of States*1
			#xx	Rn	@ERn	@(d,ERn)	@–ERn/@ERn+	@aa	@(d,PC)	@@aa	—			I	H	N	Z	V	C	Advanced
Bcc	BVS d:8	—							2			if condition is true then PC←PC+d else next;	V=1	—	—	—	—	—	—	2
	BVS d:16	—							4					—	—	—	—	—	—	3
	BPL d:8	—							2				N=0	—	—	—	—	—	—	2
	BPL d:16	—							4					—	—	—	—	—	—	3
	BMI d:8	—							2				N=1	—	—	—	—	—	—	2
	BMI d:16	—							4					—	—	—	—	—	—	3
	BGE d:8	—							2				N⊕V=0	—	—	—	—	—	—	2
	BGE d:16	—							4					—	—	—	—	—	—	3
	BLT d:8	—							2				N⊕V=1	—	—	—	—	—	—	2
	BLT d:16	—							4					—	—	—	—	—	—	3
	BGT d:8	—							2				Z∨(N⊕V)=0	—	—	—	—	—	—	2
	BGT d:16	—							4					—	—	—	—	—	—	3
	BLE d:8	—							2				Z∨(N⊕V)=1	—	—	—	—	—	—	2
	BLE d:16	—							4					—	—	—	—	—	—	3

Instruction	Mnemonic	Size	Instruction Format																	
			1st byte		2nd byte		3rd byte		4th byte		5th byte		6th byte		7th byte		8th byte		9th byte	10th byte
BTST	BTST Rn,@aa:8	B	7	E	abs		6	3	rn	0										
	BTST Rn,@aa:16	B	6	A	1	0	abs				6	3	rn	0						
	BTST Rn,@aa:32	B	6	A	3	0	abs								6	3	rn	0		
BXOR	BXOR #xx:3,Rd	B	7	5	0	IMM	rd													
	BXOR #xx:3,@ERd	B	7	C	0	erd	0	7	5	0	IMM	0								
	BXOR #xx:3,@aa:8	B	7	E	abs		7	5	0	IMM	0									
	BXOR #xx:3,@aa:16	B	6	A	1	0	abs				7	5	0	IMM	0					
	BXOR #xx:3,@aa:32	B	6	A	3	0	abs								7	5	0	IMM	0	
CLRMAC	CLRMAC	—	0	1	A	0														
CMP	CMP.B #xx:8,Rd	B	A	rd	IMM															
	CMP.B Rs,Rd	B	1	C	rs	rd														
	CMP.W #xx:16,Rd	W	7	9	2	rd	IMM													
	CMP.W Rs,Rd	W	1	D	rs	rd														
	CMP.L #xx:32,ERd	L	7	A	2	0	erd	IMM												
	CMP.L ERs,ERd	L	1	F	1	ers	0	erd												
DAA	DAA Rd	B	0	F	0	rd														
DAS	DAS Rd	B	1	F	0	rd														
DEC	DEC.B Rd	B	1	A	0	rd														
	DEC.W #1,Rd	W	1	B	5	rd														
	DEC.W #2,Rd	W	1	B	D	rd														
	DEC.L #1,ERd	L	1	B	7	0	erd													
	DEC.L #2,ERd	L	1	B	F	0	erd													
DIVXS	DIVXS.B Rs,Rd	B	0	1	D	0	5	1	rs	rd										
	DIVXS.W Rs,ERd	W	0	1	D	0	5	3	rs	0	erd									
DIVXU	DIVXU.B Rs,Rd	B	5	1	rs	rd														
	DIVXU.W Rs,ERd	W	5	3	rs	0	erd													
EEPMOV	EEPMOV.B	—	7	B	5	C	5	9	8	F										
	EEPMOV.W	—	7	B	D	4	5	9	8	F										

Figure A-1 shows timing waveforms for the address bus and the $\overline{RD}$, $\overline{HWR}$, and $\overline{LWR}$ signals during execution of the above instruction with an 8-bit bus, using three-state access with no wait states.

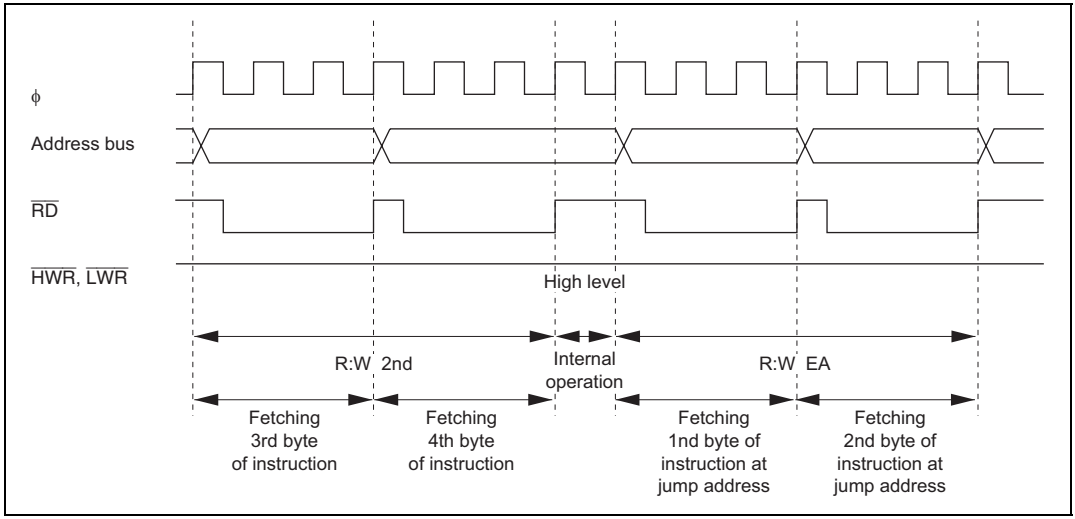


Figure A-1 Address Bus, $\overline{RD}$, $\overline{HWR}$, and $\overline{LWR}$ Timing (8-Bit Bus, Three-State Access, No Wait States)

MC8[4]

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MC8[5]

Bit	7	6	5	4	3	2	1	0
	STD_ID2	STD_ID1	STD_ID0	RTR	IDE	—	EXD_ID17	EXD_ID16
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Extended Identifier
Set the identifier (extended identifier) of data frames and remote frames

Identifier Extension

0	Standard format
1	Extended format

Remote Transmission Request

0	Data frame
1	Remote frame

Standard Identifier
Set the identifier (standard identifier) of data frames and remote frames

MC8[6]

Bit	7	6	5	4	3	2	1	0
	STD_ID10	STD_ID9	STD_ID8	STD_ID7	STD_ID6	STD_ID5	STD_ID4	STD_ID3
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Standard Identifier
Set the identifier (standard identifier) of data frames and remote frames

DDCSWR—DDC Switch Register H'FDB5 IIC

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	CLR3	CLR2	CLR1	CLR0
Initial value	:	0	0	0	0	1	1	1	1
R/W	:	R/(W)*1	R/(W)*1	R/(W)*1	R/(W)*1	W*2	W*2	W*2	W*2

Reserved bit

IIC clear 3 to 0

CLR3	CLR2	CLR1	CLR0	
0	0	—	—	Setting prohibited
	1	0	0	Setting prohibited
			1	IIC0 internal latch cleared
		1	0	IIC1 internal latch cleared
			1	IIC0 and IIC1 internal latches cleared
1	—	—	—	Invalid setting

Notes: This register is valid only when an I^2C bus interface has been added as an H8S/2638, H8S/2639, and H8S/2630 option.
1. Should always be written with 0.
2. Always read as 1.