Renesas Electronics America Inc - DF2638WF20JV Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2600
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, SCI, SmartCard
Peripherals	Motor Control PWM, POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-BFQFP
Supplier Device Package	128-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2638wf20jv

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T
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H</td><td>LWR</td></tr>
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LWR
[Otherwise]
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The package dimension that is shown in the Renesas Semiconductor Package Data Book has Priority.</td></tr>
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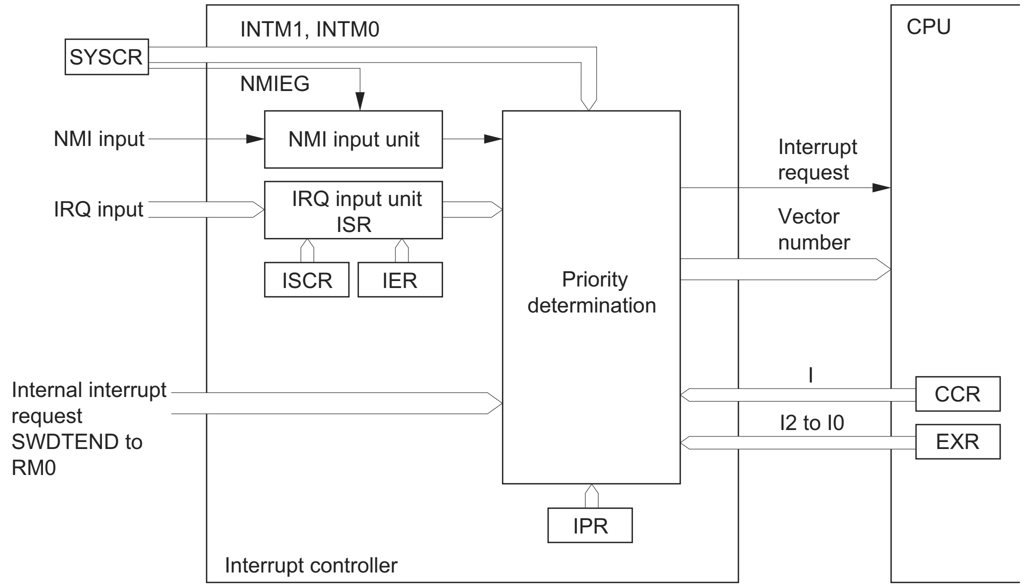
5.1.2 Block Diagram

A block diagram of the interrupt controller is shown in figure 5-1.



Legend:

ISCR: IRQ sense control register

IER: IRQ enable register

ISR: IRQ status register

IPR: Interrupt priority register

SYSCR: System control register

Figure 5-1 Block Diagram of Interrupt Controller

(2) Chain Transfer

An example of DTC chain transfer is shown in which pulse output is performed using the PPG. Chain transfer can be used to perform pulse output data transfer and PPG output trigger cycle updating. Repeat mode transfer to the PPG's NDR is performed in the first half of the chain transfer, and normal mode transfer to the TPU's TGR in the second half. This is because clearing of the activation source and interrupt generation at the end of the specified number of transfers are restricted to the second half of the chain transfer (transfer when CHNE = 0).

[1] Perform settings for transfer to the PPG's NDR. Set MRA to source address incrementing (SM1 = 1, SM0 = 0), fixed destination address (DM1 = DM0 = 0), repeat mode (MD1 = 0, MD0 = 1), and word size (Sz = 1). Set the source side as a repeat area (DTS = 1). Set MRB to chain mode (CHNE = 1, DISEL = 0). Set the data table start address in SAR, the NDRH address in DAR, and the data table size in CRAH and CRAL. CRB can be set to any value.

[2] Perform settings for transfer to the TPU's TGR. Set MRA to source address incrementing (SM1 = 1, SM0 = 0), fixed destination address (DM1 = DM0 = 0), normal mode (MD1 = MD0 = 0), and word size (Sz = 1). Set the data table start address in SAR, the TGRA address in DAR, and the data table size in CRA. CRB can be set to any value.

[3] Locate the TPU transfer register information consecutively after the NDR transfer register information.

[4] Set the start address of the NDR transfer register information to the DTC vector address.

[5] Set the bit corresponding to TGIA in DTCER to 1.

[6] Set TGRA as an output compare register (output disabled) with TIOR, and enable the TGIA interrupt with TIER.

[7] Set the initial output value in PODR, and the next output value in NDR. Set bits in DDR and NDER for which output is to be performed to 1. Using PCR, select the TPU compare match to be used as the output trigger.

[8] Set the CST bit in TSTR to 1, and start the TCNT count operation.

[9] Each time a TGRA compare match occurs, the next output value is transferred to NDR and the set value of the next output trigger period is transferred to TGRA. The activation source TGFA flag is cleared.

Pin	Selection Method and Pin Functions
PB6/A14/TIOCA5	The function of this pin changes according to the operating mode and the setting of bits AE3 to AE0 in PFCR; the TPU5 settings of bits MD3 to MD0 in TMDR5, bits IOA3 to IOA0 in TIOR5, and the CCLR1 and CCLR0 bits in TCR5; and the setting of the PB6DDR bit.

Operating Mode	Modes 4 to 6			
AE3 to AE0	B'0000 to B'0110			B'0111 to B'1111
TPU Channel 5 Setting	Table Below (1)	Table Below (2)		—
PB6DDR	—	0	1	—
Pin function	TIOCA5 output	PB6 input	PB6 output	A14 output
		TIOCA5 input *1		

Operating Mode	Mode 7		
TPU Channel 5 Setting	Table Below (1)	Table Below (2)	
PB6DDR	—	0	1
Pin function	TIOCA5 output	PB6 input	PB6 output
		TIOCA5 input *1	

TPU Channel 5 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output function	—	Output compare output	—	PWM mode 1 output*2	PWM mode 2 output	—

x: Don't care

Notes: 1. TIOCA5 input when MD3 to MD0 = B'0000 or B'01xx and IOA3 = 1.
2. TIOCB5 output is disabled.

- Phase counting mode 4

  Figure 10-32 shows an example of phase counting mode 4 operation, and table 10-12 summarizes the TCNT up/down-count conditions.

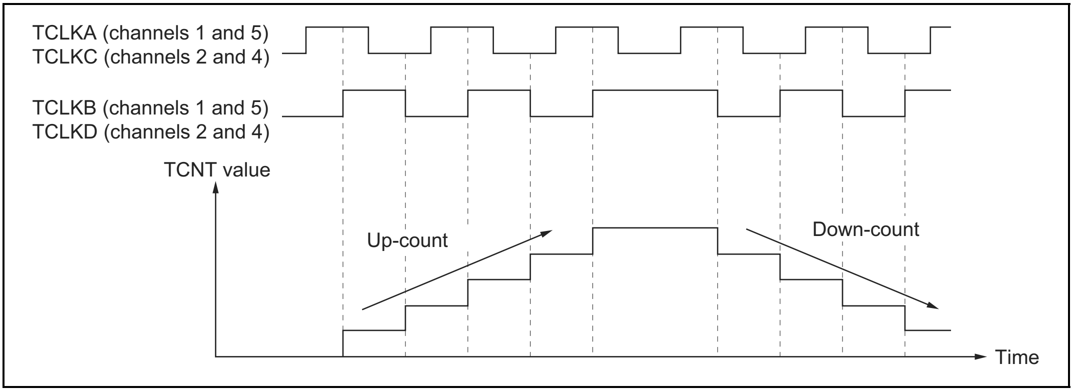


Figure 10-32 Example of Phase Counting Mode 4 Operation

Table 10-12 Up/Down-Count Conditions in Phase Counting Mode 4

TCLKA (Channels 1 and 5) TCLKC (Channels 2 and 4)	TCLKB (Channels 1 and 5) TCLKD (Channels 2 and 4)	Operation
High level	↑	Up-count
Low level	↓	
↑	Low level	Don’t care
↓	High level	
High level	↓	Down-count
Low level	↑	
↑	High level	Don’t care
↓	Low level	

Legend:

↑ : Rising edge

↓ : Falling edge

Table 13-5 shows the maximum bit rate for each frequency in asynchronous mode. Tables 13-6 and 13-7 show the maximum bit rates with external clock input.

Table 13-5 Maximum Bit Rate for Each Frequency (Asynchronous Mode)

φ (MHz)	**Maximum Bit Rate (bit/s)**	**n**	**N**
4	125000	0	0
4.9152	153600	0	0
5	156250	0	0
6	187500	0	0
6.144	192000	0	0
7.3728	230400	0	0
8	250000	0	0
9.8304	307200	0	0
10	312500	0	0
12	375000	0	0
12.288	384000	0	0
14	437500	0	0
14.7456	460800	0	0
16	500000	0	0
17.2032	537600	0	0
18	562500	0	0
19.6608	614400	0	0
20	625000	0	0

The reception procedure and operations in slave receive mode are described below.

[1] Set the ICE bit in ICCR to 1. Set the MLS bit in ICMR and the MST and TRS bits in ICCR according to the operating mode.

[2] When the start condition output by the master device is detected, the BBSY flag in ICCR is set to 1.

[3] When the slave address matches in the first frame following the start condition, the device operates as the slave device specified by the master device. If the 8th data bit ($R/\overline{W}$) is 0, the TRS bit in ICCR remains cleared to 0, and slave receive operation is performed.

[4] At the 9th clock pulse of the receive frame, the slave device drives SDA low and returns an acknowledge signal. At the same time, the IRIC flag in ICCR is set to 1. If the IEIC bit in ICCR has been set to 1, an interrupt request is sent to the CPU. If the RDRF internal flag has been cleared to 0, it is set to 1, and the receive operation continues. If the RDRF internal flag has been set to 1, the slave device drives SCL low from the fall of the receive clock until data is read into ICDR.

[5] Read ICDR and clear the IRIC flag in ICCR to 0. The RDRF flag is cleared to 0.

Receive operations can be performed continuously by repeating steps [4] and [5]. When SDA is changed from low to high when SCL is high, and the stop condition is detected, the BBSY flag in ICCR is cleared to 0.

17.1.2 Block Diagram

Figure 17-1 shows a block diagram of the A/D converter.

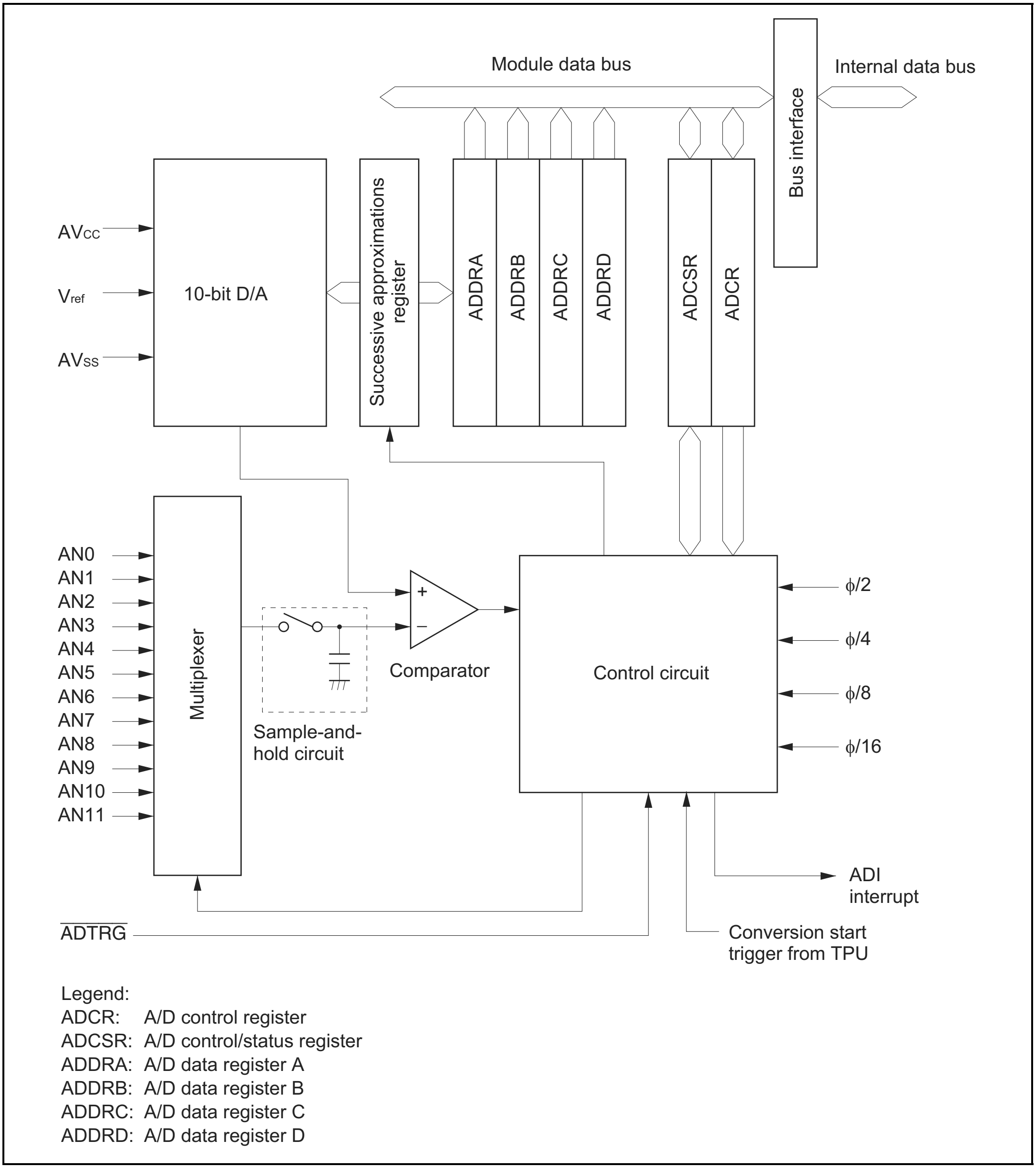


Figure 17-1 Block Diagram of A/D Converter

Table 17-4 A/D Conversion Time (Single Mode)

		CKS1 = 0						CKS1 = 0					
		CKS0 = 0			CKS0 = 1			CKS0 = 0			CKS0 = 1		
Item	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
A/D conversion start delay	t_D	18	—	33	10	—	17	6	—	9	4	—	5
Input sampling time	t_{SPL}	—	127	—	—	63	—	—	31	—	—	15	—
A/D conversion time	t_{CONV}	515	—	530	259	—	266	131	—	134	67	—	68

Note: Values in the table are the number of states.

Table 17-5 A/D Conversion Time (Scan Mode)

CKS1	CKS0	Conversion Time (State)
0	0	512 (Fixed)
	1	256 (Fixed)
1	0	128 (Fixed)
	1	64 (Fixed)

17.4.4 External Trigger Input Timing

A/D conversion can be externally triggered. When the TRGS1 and TRGS0 bits are set to 11 in ADCR, external trigger input is enabled at the $\overline{\text{ADTRG}}$ pin. A falling edge at the $\overline{\text{ADTRG}}$ pin sets the ADST bit to 1 in ADCSR, starting A/D conversion. Other operations, in both single and scan modes, are the same as if the ADST bit has been set to 1 by software. Figure 17-6 shows the timing.

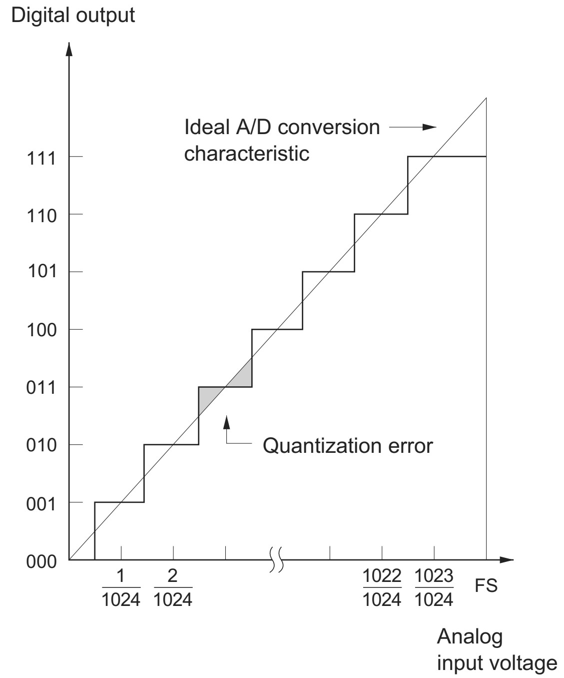


Figure 17-9 A/D Conversion Precision Definitions (1)

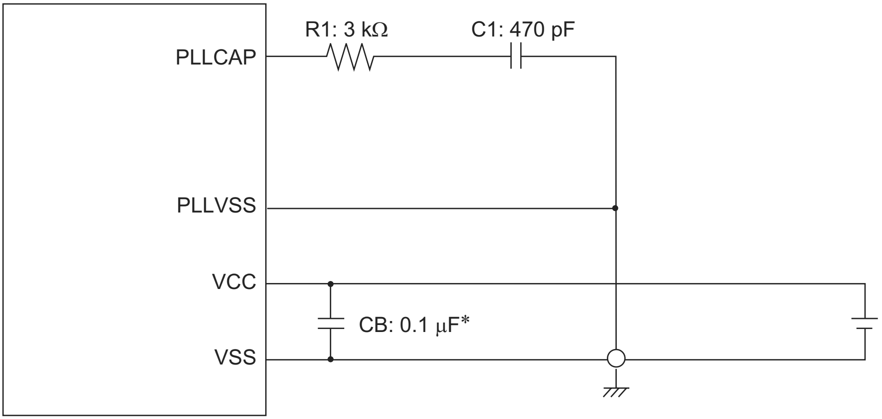
21B.10.2 Software Protection

Software protection can be implemented by setting the SWE bit in FLMCR1, erase block register 1 (EBR1), erase block register 2 (EBR2), and the RAMS bit in the RAM emulation register (RAMER). When software protection is in effect, setting the P or E bit in flash memory control register 1 (FLMCR1), does not cause a transition to program mode or erase mode (See table 21B-12).

Table 21B-12 Software Protection

		Functions	
Item	**Description**	**Program**	**Erase**
SWE bit protection	• Setting bit SWE in FLMCR1 to 0 will place area on-chip flash memory in the program/erase-protected state (Execute the program in the on-chip RAM, external memory).	Yes	Yes
Block specification protection	• Erase protection can be set for individual blocks by settings in erase block register 1 (EBR1) and erase block register 2 (EBR2). • Setting EBR1 and EBR2 to H'00 places all blocks in the erase-protected state.	—	Yes
Emulation protection	• Setting the RAMS bit to 1 in the RAM emulation register (RAMER) places all blocks in the program/erase-protected state.	Yes	Yes

External circuitry such as that shown below is recommended around the PLL.



(Values are preliminary recommended values.)

Note: * CB is laminated ceramic capacitors.

Figure 22A-5 Points for Attention when Using PLL Oscillation Circuit

Place oscillation stabilization capacitor C1 and resistor R1 close to the PLLCAP pin, and ensure that no other signal lines cross this line. Supply the C1 ground from PLLVSS.

Separate PLLVSS from the other VCC and VSS lines at the board power supply source, and be sure to insert bypass capacitors CB close to the pins.

23A.2 Register Descriptions

23A.2.1 Standby Control Register (SBYCR)

Bit :	7	6	5	4	3	2	1	0
	SSBY	STS2	STS1	STS0	OPE	—	—	—
Initial value :	0	1	0	1	1	0	0	0
R/W :	R/W	R/W	R/W	R/W	R/W	—	—	—

SBYCR is an 8-bit readable/writable register that performs power-down mode control.

SBYCR is initialized to H'58 by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bit 7—Software Standby (SSBY): When making a low power dissipation mode transition by executing the SLEEP instruction, the operating mode is determined in combination with other control bits.

Note that the value of the SSBY bit does not change even when shifting between modes using interrupts.

Bit 7 SSBY	Description
0	Shifts to sleep mode when the SLEEP instruction is executed in high-speed mode or medium-speed mode. (Initial value)
1	Shifts to software standby mode when the SLEEP instruction is executed in high-speed mode or medium-speed mode.

Bits 6 to 4—Standby Timer Select 2 to 0 (STS2 to STS0): These bits select the MCU wait time for clock stabilization when shifting to high-speed mode or medium-speed mode by using a specific interrupt or command to cancel software standby mode. With a quartz oscillator (Table 23A-5), select a wait time of 8ms (oscillation stabilization time) or more, depending on the operating frequency. With an external clock, select a standby time of 2 ms or more (PLL oscillator settling time), based on the operating frequency.

MC10[1]—Message Control 10[1]	**H'F870**	**HCAN0**
MC10[2]—Message Control 10[2]	**H'F871**	**HCAN0**
MC10[3]—Message Control 10[3]	**H'F872**	**HCAN0**
MC10[4]—Message Control 10[4]	**H'F873**	**HCAN0**
MC10[5]—Message Control 10[5]	**H'F874**	**HCAN0**
MC10[6]—Message Control 10[6]	**H'F875**	**HCAN0**
MC10[7]—Message Control 10[7]	**H'F876**	**HCAN0**
MC10[8]—Message Control 10[8]	**H'F877**	**HCAN0**

MC10[1]

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	DLC3	DLC2	DLC1	DLC0
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data Length Code

0	0	0	0	Data length = 0 bytes
			1	Data length = 1 byte
		1	0	Data length = 2 bytes
			1	Data length = 3 bytes
	1	0	0	Data length = 4 bytes
			1	Data length = 5 bytes
		1	0	Data length = 6 bytes
			1	Data length = 7 bytes
1	0/1	0/1	0/1	Data length = 8 bytes

MC10[2]

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MC10[3]

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD5[1]—Message Data 5[1]	**H'F8D8**	**HCAN0**
MD5[2]—Message Data 5[2]	**H'F8D9**	**HCAN0**
MD5[3]—Message Data 5[3]	**H'F8DA**	**HCAN0**
MD5[4]—Message Data 5[4]	**H'F8DB**	**HCAN0**
MD5[5]—Message Data 5[5]	**H'F8DC**	**HCAN0**
MD5[6]—Message Data 5[6]	**H'F8DD**	**HCAN0**
MD5[7]—Message Data 5[7]	**H'F8DE**	**HCAN0**
MD5[8]—Message Data 5[8]	**H'F8DF**	**HCAN0**

MDx[1]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MDx[2]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MDx[3]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MDx[4]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MDx[5]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MDx[6]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MDx[7]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MDx[8]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

*: Undefined
x = 0 to 15

MD8[1]—Message Data 8[1]	**H'FAF0**	**HCAN1**
MD8[2]—Message Data 8[2]	**H'FAF1**	**HCAN1**
MD8[3]—Message Data 8[3]	**H'FAF2**	**HCAN1**
MD8[4]—Message Data 8[4]	**H'FAF3**	**HCAN1**
MD8[5]—Message Data 8[5]	**H'FAF4**	**HCAN1**
MD8[6]—Message Data 8[6]	**H'FAF5**	**HCAN1**
MD8[7]—Message Data 8[7]	**H'FAF6**	**HCAN1**
MD8[8]—Message Data 8[8]	**H'FAF7**	**HCAN1**

Note: These registers are not available in the H8S/2635 Group.

MDx[1]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MDx[2]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MDx[3]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MDx[4]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MDx[5]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MDx[6]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MDx[7]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MDx[8]	Bit	7	6	5	4	3	2	1	0
	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

*: Undefined
x = 0 to 15

Notes:
1. TXI interrupt request cancellation can be performed by reading 1 from the TDRE flag, then clearing it to 0, or clearing the TIE bit to 0.
2. RXI and ERI interrupt request cancellation can be performed by reading 1 from the RDRF flag, or the FER, PER, or ORER flag, then clearing the flag to 0, or clearing the RIE bit to 0.
3. The TDRE flag in SSR is fixed at 1.
4. In this state, serial transmission is started when transmit data is written to TDR and the TDRE flag in SSR is cleared to 0.

   SMR setting must be performed to decide the transfer format before setting the TE bit to 1.
5. Clearing the RE bit to 0 does not affect the RDRF, FER, PER, and ORER flags, which retain their states.
6. Serial reception is started in this state when a start bit is detected in asynchronous mode or serial clock input is detected in clocked synchronous mode.

   SMR setting must be performed to decide the transfer format before setting the RE bit to 1.
7. When receive data including MPB = 0 is received, receive data transfer from RSR to RDR, receive error detection, and setting of the RDRF, FER, and ORER flags in SSR , is not performed. When receive data including MPB = 1 is received, the MPB bit in SSR is set to 1, the MPIE bit is cleared to 0 automatically, and generation of RXI and ERI interrupts (when the TIE and RIE bits in SCR are set to 1) and FER and ORER flag setting is enabled.
8. TEI cancellation can be performed by reading 1 from the TDRE flag in SSR, then clearing it to 0 and clearing the TEND flag to 0, or clearing the TEIE bit to 0.

TDR0—Transmit Data Register 0 H'FF7B SCI0, Smart Card Interface 0

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Store serial transmit data

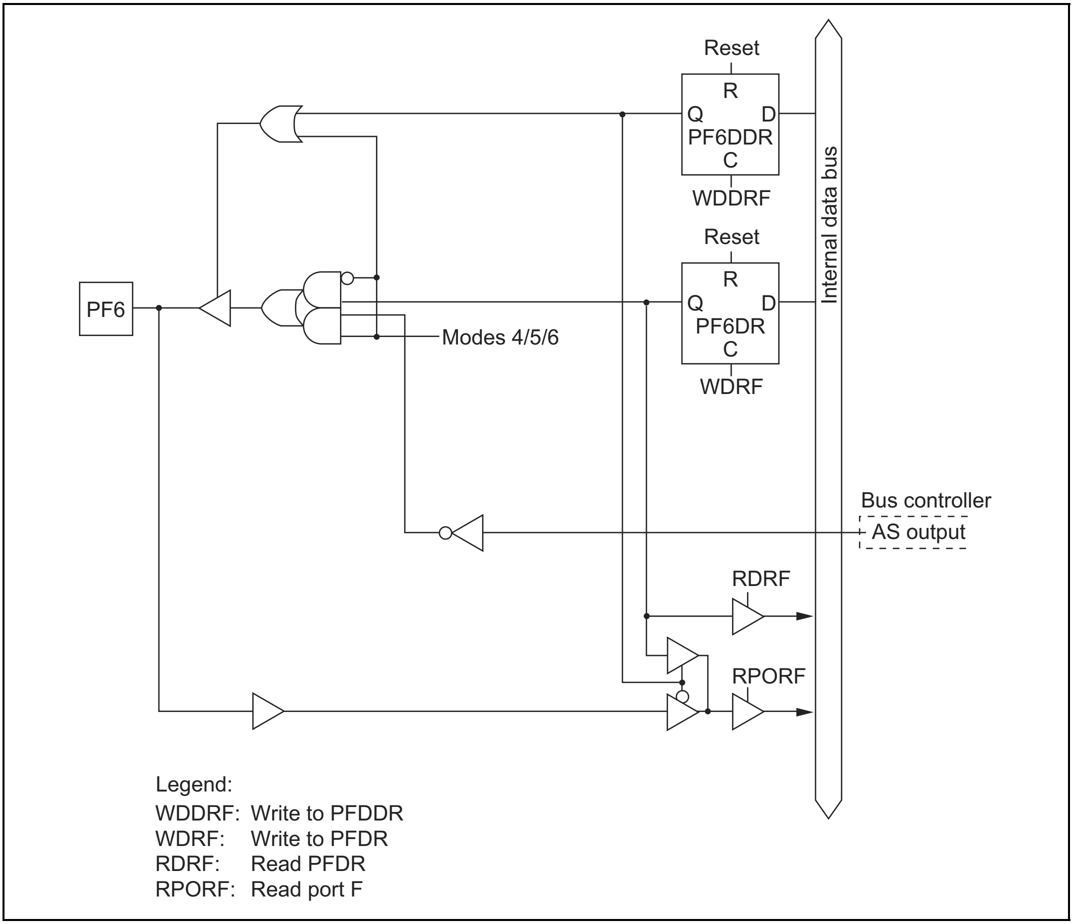


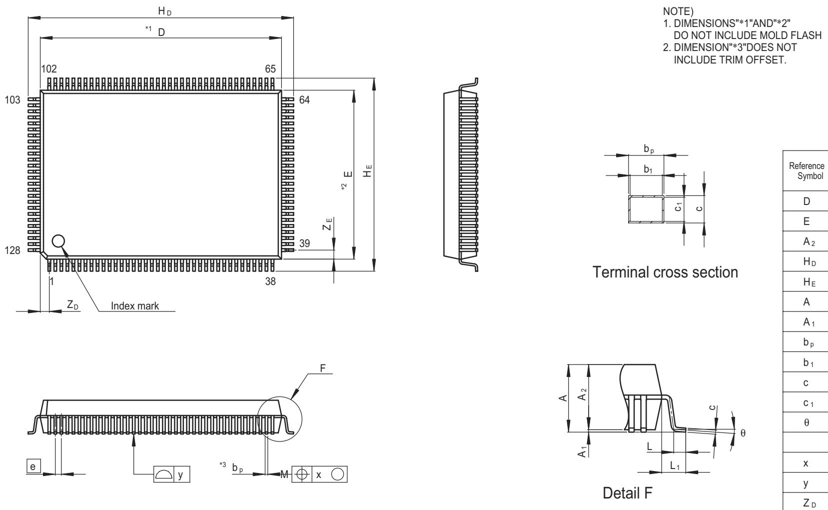
Figure C-10 (e) Port F Block Diagram (Pin PF6)

Appendix G Package Dimensions

The package dimension that is shown in the Renesas Semiconductor Package Data Book has Priority.

Figure G-1 shows the package dimensions of the H8S/2636, H8S/2638, H8S/2639, H8S/2630, H8S/2635, and H8S/2634.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP128-14x20-0.50	PRQP0128KB-A	FP-128B/FP-128BV	1.7g



NOTE)
1. DIMENSIONS"*1"AND"*2"
DO NOT INCLUDE MOLD FLASH
2. DIMENSION"*3"DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	20	——
E	——	14	——
A_2	——	2.70	——
H_D	21.8	22.0	22.2
H_E	15.8	16.0	16.2
A	——	——	3.15
A_1	0.00	0.10	0.25
b_p	0.17	0.22	0.27
b_1	——	0.20	——
c	0.12	0.17	0.22
c_1	——	0.15	——
θ	0°	——	8°
	——	0.5	——
x	——	——	0.10
y	——	——	0.10
Z_D	——	0.75	——
Z_E	——	0.75	——
L	0.3	0.5	0.7
L_1	——	1.0	——

Figure G-1 FP-128B Package Dimensions