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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2600
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, SCI, SmartCard
Peripherals	Motor Control PWM, POR, PWM, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	128-BFQFP
Supplier Device Package	128-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2638wf20v

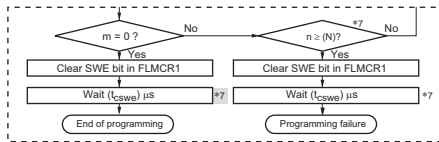
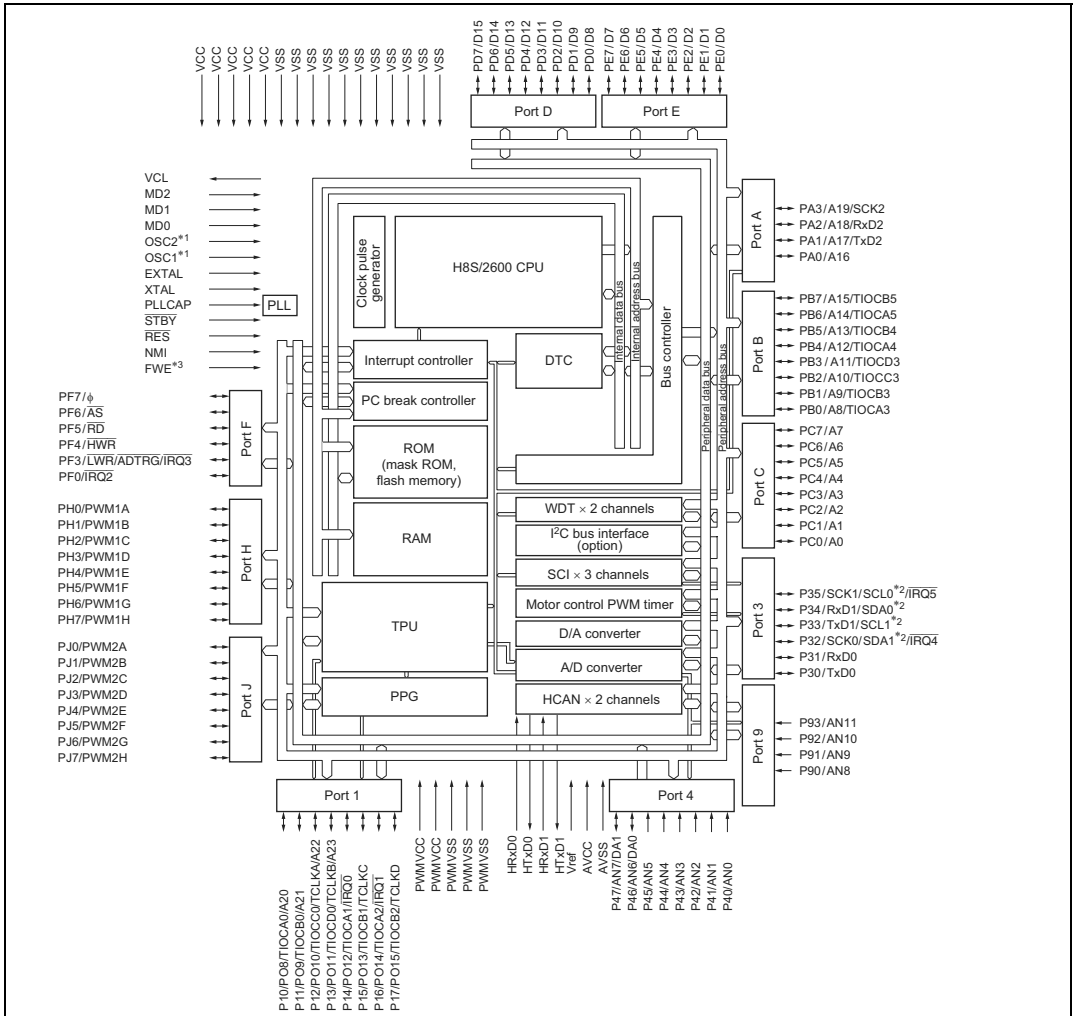
Item	Page	Revision (See Manual for Details)
21C.4.3 Mode Transitions Figure 21C-3 Flash Memory State Transitions	855	Notes amended Notes: 2. This LSI transits to programmer mode by using the dedicated PROM programmer.
21C.9.1 Program Mode	880	Description amended The wait times after bits are set or cleared in the flash memory control register 1 (FLMCR1) and the maximum number of programming operations (N) are shown in section 24.2.7, 24.3.7, and 24.4.7, Flash Memory Characteristics.
21C.9.2 Program-Verify Mode Figure 21C-12 Program/Program-Verify Flowchart	884	Figure amended 
21C.9.3 Erase Mode	885	Description amended The wait times after bits are set or cleared in the flash memory control register 1 (FLMCR1) and the maximum number of erase operations (N) are shown in section 24.2.7 and 24.3.7, Flash Memory Characteristics. … Next, the watchdog timer (WDT) is set to prevent overerasing due to program runaway, etc. Set a value of about 19.8 ms as the WDT overflow period.

Figure 1-1 (b) shows an internal block diagram of the H8S/2638, H8S/2639, and H8S/2630.



Notes: 1. Subclock functions (subactive mode, subsleep mode, and watch mode) are available in the U-mask and W-mask versions. These functions cannot be used with the other versions.
See section 22A.7, Subclock Oscillator, for the method of fixing pins OSC1 and OSC2.
The H8S/2639 has no OSC1 and OSC2 pins.
2. These pins are used for the I²C bus interface.
The I²C bus interface is available as an option. The product equipped with the I²C bus interface is the W-mask version.
3. The FWE pin is for compatibility with the flash memory version.
The FWE pin is a NC pin in the mask ROM versions.
In the mask ROM version, the FWE pin must be left open or be connected to Vss.

Figure 1-1 (b) Internal Block Diagram of H8S/2638, H8S/2639, and H8S/2630

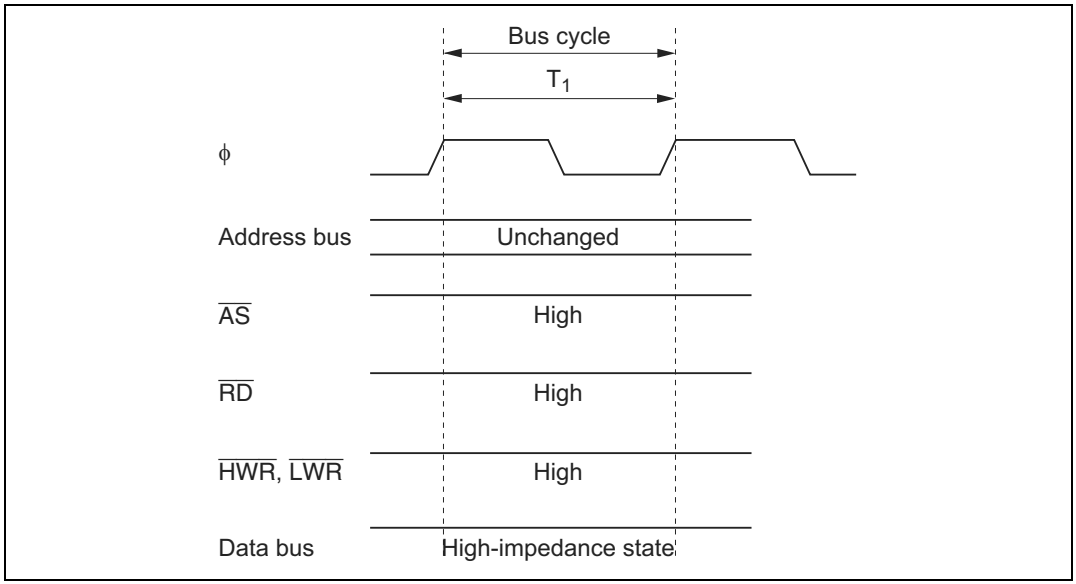


Figure 2-18 Pin States during On-Chip Memory Access

7.3.4 Interface Specifications for Each Area

The initial state of each area is basic bus interface, 3-state access space. The initial bus width is selected according to the operating mode. The bus specifications described here cover basic items only, and the sections on each memory interface (7.4, Basic Bus Interface, and 7.5, Burst ROM Interface) should be referred to for further details.

Area 0: Area 0 includes on-chip ROM, and in ROM-disabled expansion mode, all of area 0 is external space. In ROM-enabled expansion mode, the space excluding on-chip ROM is external space.

Either basic bus interface or burst ROM interface can be selected for area 0.

Areas 1 to 6: In external expansion mode, all of areas 1 to 6 is external space.

Only the basic bus interface can be used for areas 1 to 6.

Area 7: Area 7 includes the on-chip RAM and internal I/O registers. In external expansion mode, the space excluding the on-chip RAM and internal I/O registers is external space. The on-chip RAM is enabled when the RAME bit in the system control register (SYSCR) is set to 1; when the RAME bit is cleared to 0, the on-chip RAM is disabled and the corresponding space becomes external space.

Only the basic bus interface can be used for the area 7.

Pin	Selection Method and Pin Functions
PB0/A8/TIOCA3	The function of this pin changes according to the operating mode and the setting of bits AE3 to AE0 in PFCR; the TPU3 settings of bits MD3 to MD0 in TMDR3, bits IOA3 to IOA0 in TIORH3, and bits CCLR2 to CCLR0 in TCR3; and the setting of the PB0DDR bit.

Operating Mode	Modes 4 to 6			
AE3 to AE0	B'0000			B'0001 to B'1111
TPU Channel 3 Setting	Table Below (1)	Table Below (2)		—
PB0DDR	—	0	1	—
Pin function	TIOCA3 output	PB0 input	PB0 output	A8 output
		TIOCA3 input *1		

Operating Mode	Mode 7		
TPU Channel 3 Setting	Table Below (1)	Table Below (2)	
PB0DDR	—	0	1
Pin function	TIOCA3 output	PB0 input	PB0 output
		TIOCA3 input *1	

TPU Channel 3 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'001x	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'001	B'001
Output function	—	Output compare output	—	PWM mode 1 output*2	PWM mode 2 output	—

x: Don't care

Notes: 1. TIOCA3 input when MD3 to MD0 = B'0000 and IOA3 to IOA0 = B'10xx.
2. TIOCB3 output is disabled.

9.12.2 Register Configuration

Table 9-22 shows the port H register configuration.

Table 9-22 Port H Registers

Name	Abbreviation	R/W	Initial Value	Address*
Port H data direction register	PHDDR	W	H'00	H'FC20
Port H data register	PHDR	RW	H'00	H'FC24
Port H register	PORTH	R	Undefined	H'FC28

Note: * Lower 16 bits of the address.

Port H Data Direction Register (PHDDR)

Bit	:	7	6	5	4	3	2	1	0
		PH7DDR	PH6DDR	PH5DDR	PH4DDR	PH3DDR	PH2DDR	PH1DDR	PH0DDR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	W	W	W	W	W	W	W	W

PHDDR is an 8-bit write-only register, the individual bits of which specify input or output for the pins of port H. PHDDR cannot be read. If it is, an undefined value will be read.

PHDDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Port H Data Register (PHDR)

Bit	:	7	6	5	4	3	2	1	0
		PH7DR	PH6DR	PH5DR	PH4DR	PH3DR	PH2DR	PH1DR	PH0DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PHDR is an 8-bit readable/writeable register that stores output data for the port H pins (PH7 to PH0).

PHDR is initialized to H'00 by a reset and in hardware standby mode. It retains its prior state in software standby mode.

Contention between Buffer Register Write and Compare Match: If a compare match occurs in the T_2 state of a TGR write cycle, the data transferred to TGR by the buffer operation will be the data prior to the write.

Figure 10-52 shows the timing in this case.

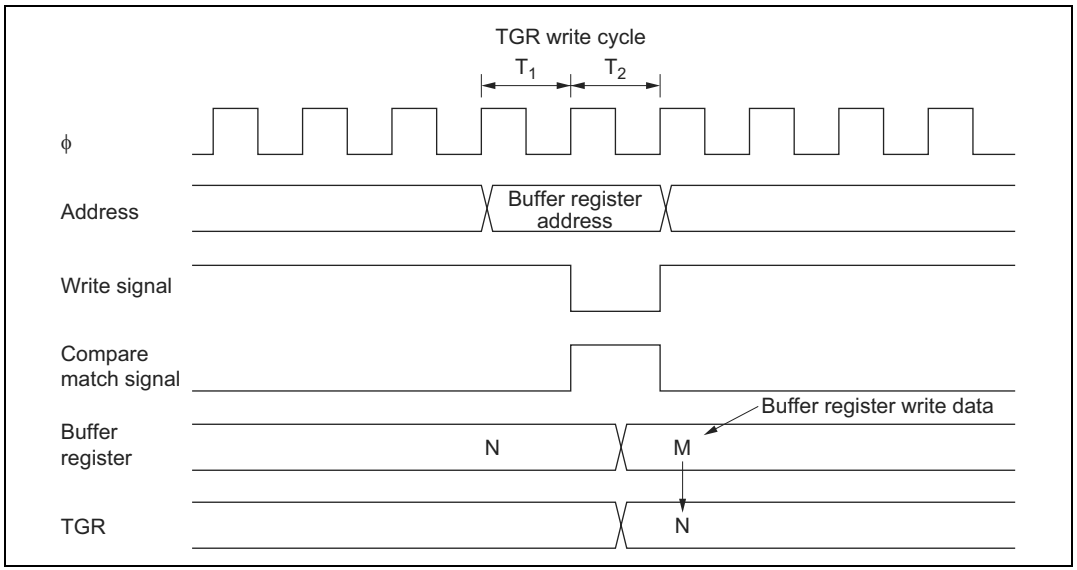


Figure 10-52 Contention between Buffer Register Write and Compare Match

13.2.7 Serial Status Register (SSR)

Bit	:	7	6	5	4	3	2	1	0
		TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Initial value	:	1	0	0	0	0	1	0	0
R/W	:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Note: * Only 0 can be written, to clear the flag.

SSR is an 8-bit register containing status flags that indicate the operating status of the SCI, and multiprocessor bits.

SSR can be read or written to by the CPU at all times. However, 1 cannot be written to flags TDRE, RDRF, ORER, PER, and FER. Also note that in order to clear these flags they must be read as 1 beforehand. The TEND flag and MPB flag are read-only flags and cannot be modified.

SSR is initialized to H'84 by a reset, in standby mode, watch mode*, subactive mode*, and subsleep mode* or module stop mode.

Note: * Subclock functions (subactive mode, subsleep mode, and watch mode) are available in the U-mask and W-mask versions, and H8S/2635 Group only.
These functions cannot be used with the other versions.

Bit 7—Transmit Data Register Empty (TDRE): Indicates that data has been transferred from TDR to TSR and the next serial data can be written to TDR.

Bit 7

TDRE	Description
0	[Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DTC is activated by a TXI interrupt and writes data to TDR
1	[Setting conditions] (Initial value) • When the TE bit in SCR is 0 • When data is transferred from TDR to TSR and data can be written to TDR

16.2.9 Receive Complete Register (RXPR)

The receive complete register (RXPR) is a 16-bit readable/writable register containing status flags that indicate normal reception of messages (data frame or remote frame) in mailboxes (buffers).

In the case of remote frame reception, the corresponding remote request register (RFPR) is also set simultaneously.

RXPR

Bit:	15	14	13	12	11	10	9	8
	RXPR7	RXPR6	RXPR5	RXPR4	RXPR3	RXPR2	RXPR1	RXPR0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Bit:	7	6	5	4	3	2	1	0
	RXPR15	RXPR14	RXPR13	RXPR12	RXPR11	RXPR10	RXPR9	RXPR8
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: * Only a write of 1 is permitted, to clear the flag.

Bits 15 to 0—Receive Complete Register (RXPR7 to RXPR0, RXPR15 to RXPR8): These bits indicate that a receive message has been received normally in the corresponding mailbox.

Bit x: RXPRx	Description
0	[Clearing condition] • Writing 1 (Initial value)
1	Completion of message (data frame or remote frame) reception in corresponding mailbox

(x = 15 to 0)

21A.9 Flash Memory Programming/Erasing

A software method, using the CPU, is employed to program and erase flash memory in the on-board programming modes. There are four flash memory operating modes: program mode, erase mode, program-verify mode, and erase-verify mode. Transitions to these modes for on-chip flash memory are made by setting the PSU, ESU, P, E, PV, and EV bits in FLMCR1.

The flash memory cannot be read while being programmed or erased. Therefore, the program (user program) that controls flash memory programming/erasing should be located and executed in on-chip RAM or external memory. If the program is to be located in external memory, the instruction for writing to flash memory, and the following instruction, should be placed in on-chip RAM. Also ensure that the DTC is not activated before or after execution of the flash memory write instruction.

In the following operation descriptions, wait times after setting or clearing individual bits in FLMCR1 are given as parameters; for details of the wait times, see section 24.1.7, Flash Memory Characteristics.

Notes: 1. Operation is not guaranteed if setting/resetting of the SWE, ESU, PSU, EV, PV, E, and P bits in FLMCR1 is executed by a program in flash memory.
2. When programming or erasing, set FWE to 1 (programming/erasing will not be executed if FWE = 0).
3. Programming must be executed in the erased state. Do not perform additional programming on addresses that have already been programmed.

21B.12 Interrupt Handling when Programming/Erasing Flash Memory

All interrupts, including NMI interrupt is disabled when flash memory is being programmed or erased (when the P or E bit is set in FLMCR1), and while the boot program is executing in boot mode*1, to give priority to the program or erase operation. There are three reasons for this:

1. Interrupt during programming or erasing might cause a violation of the programming or erasing algorithm, with the result that normal operation could not be assured.
2. In the interrupt exception handling sequence during programming or erasing, the vector would not be read correctly*2, possibly resulting in MCU runaway.
3. If interrupt occurred during boot program execution, it would not be possible to execute the normal boot mode sequence.

For these reasons, in on-board programming mode alone there are conditions for disabling interrupt, as an exception to the general rule. However, this provision does not guarantee normal erasing and programming or MCU operation. All requests, including NMI interrupt, must therefore be restricted inside and outside the MCU when programming or erasing flash memory. NMI interrupt is also disabled in the error-protection state while the P or E bit remains set in FLMCR1.

Notes: 1. Interrupt requests must be disabled inside and outside the MCU until the programming control program has completed programming.
2. The vector may not be read correctly in this case for the following two reasons:
   - If flash memory is read while being programmed or erased (while the P or E bit is set in FLMCR1), correct read data will not be obtained (undetermined values will be returned).
   - If the interrupt entry in the vector table has not been programmed yet, interrupt exception handling will not be executed correctly.

On-Chip Supporting Module Interrupt: Relevant interrupt operations cannot be performed in module stop mode. Consequently, if module stop mode is entered when an interrupt has been requested, it will not be possible to clear the CPU interrupt source or the DTC activation source. Interrupts should therefore be disabled before entering module stop mode.

Writing to MSTPCR: MSTPCR should only be written to by the CPU.

23A.6 Software Standby Mode

23A.6.1 Software Standby Mode

A transition is made to software standby mode when the SLEEP instruction is executed when the SBYCR SSBY bit = 1 and the LPWRCR LSON bit = 0, and the TCSR (WDT1) PSS bit = 0. In this mode, the CPU, on-chip supporting modules, and oscillator all stop. However, the contents of the CPU's internal registers, RAM data, and the states of on-chip supporting modules other than the SCI, A/D converter, Motor control, PWM, HCAN and I/O ports, are retained. Whether the address bus and bus control signals are placed in the high-impedance state.

In this mode the oscillator stops, and therefore power dissipation is significantly reduced.

23A.6.2 Clearing Software Standby Mode

Software standby mode is cleared by an external interrupt (NMI pin, or pins $\overline{\text{IRQ0}}$ to $\overline{\text{IRQ5}}$), or by means of the $\overline{\text{RES}}$ pin or $\overline{\text{STBY}}$ pin.

- Clearing with an interrupt

  When an NMI or IRQ0 to IRQ5 interrupt request signal is input, clock oscillation starts, and after the elapse of the time set in bits STS2 to STS0 in SYSCR, stable clocks are supplied to the entire chip, software standby mode is cleared, and interrupt exception handling is started.

  When clearing software standby mode with an IRQ0 to IRQ5 interrupt, set the corresponding enable bit to 1 and ensure that no interrupt with a higher priority than interrupts IRQ0 to IRQ5 is generated. Software standby mode cannot be cleared if the interrupt has been masked on the CPU side or has been designated as a DTC activation source.

- Clearing with the $\overline{\text{RES}}$ pin

  When the $\overline{\text{RES}}$ pin is driven low, clock oscillation is started. At the same time as clock oscillation starts, clocks are supplied to the entire chip. Note that the $\overline{\text{RES}}$ pin must be held low until clock oscillation stabilizes. When the $\overline{\text{RES}}$ pin goes high, the CPU begins reset exception handling.

Table 23B.3 Low Power Dissipation Mode Transition Conditions

Pre-Transition State	Status of Control Bit at Transition				State after Transition Invoked by SLEEP Command	State after Transition Back from Low Power Mode Invoked by Interrupt
	SSBY	PSS	LSON	DTON		
High-speed/ Medium-speed	0	*	0	*	Sleep	High-speed/Medium-speed
	0	*	1	*	—	—
	1	0	0	*	Software standby	High-speed/Medium-speed
	1	0	1	*	—	—
	1	1	0	0	Watch	High-speed
	1	1	1	0	Watch	Subactive
	1	1	0	1	—	—
	1	1	1	1	Subactive	—
Subactive	0	0	*	*	—	—
	0	1	0	*	—	—
	0	1	1	*	Subsleep	Subactive
	1	0	*	*	—	—
	1	1	0	0	Watch	High-speed
	1	1	1	0	Watch	Subactive
	1	1	0	1	High-speed	—
	1	1	1	1	—	—

Legend:

*: Don’t care

—: Do not set

Section 24 Electrical Characteristics

24.1 H8S/2636 Group Electrical Characteristics

24.1.1 Absolute Maximum Ratings

Table 24-1 lists the absolute maximum ratings.

Table 24-1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage (OSC1, OSC2)	V_{in}	–0.3 +4.3	V
Input voltage (XTAL, EXTAL)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (ports 4 and 9)	V_{in}	–0.3 to AV_{CC} +0.3	V
Input voltage (ports H and J)	V_{in}	–0.3 to $PWMV_{CC}$ +0.3	V
Input voltage (except XTAL, EXTAL, OSC1, OSC2, ports 4, 9, H and J)	V_{in}	–0.3 to V_{CC} +0.3	V
Reference voltage	V_{ref}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum rating are exceeded.

24.3.7 Flash Memory Characteristics

Table 24-34 shows the flash memory characteristics.

Table 24-34 Flash Memory Characteristics

Conditions: V_{CC} =4.5 V to 5.5 V, $PWMV_{CC}$ = 4.5 V to 5.5 V, AV_{CC} = 4.5 V to 5.5 V, V_{ref} = 4.5 V to AV_{CC}, V_{SS} = $PWMV_{SS}$ = $PLLV_{SS}$, AV_{SS} = 0 V
T_a = 0 to +75°C (Programming/erasing operating temperature range: regular specification)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Condition
Programming time*1 *2 *4		t_P	—	10	200	ms/ 128 bytes	
Erase time*1 *3 *5		t_E	—	100	1200	ms/block	
Reprogramming count		N_{WEC}	—	—	100	Times	
Programming	Wait time after SWE bit setting*1	t_{sswe}	1	1	—	µs	
	Wait time after PSU bit setting*1	t_{spsu}	50	50	—	µs	
	Wait time after P bit setting*1 *4	t_{sp30}	28	30	32	µs	Programming time wait
		t_{sp200}	198	200	202	µs	Programming time wait
		t_{sp10}	8	10	12	µs	Additional-programming time wait
	Wait time after P bit clear*1	t_{cp}	5	5	—	µs	
	Wait time after PSU bit clear*1	t_{cpsu}	5	5	—	µs	
	Wait time after PV bit setting*1	t_{spv}	4	4	—	µs	
	Wait time after H'FF dummy write*1	t_{spvr}	2	2	—	µs	
	Wait time after PV bit clear*1	t_{cpv}	2	2	—	µs	
	Wait time after SWE bit clear*1	t_{cswe}	100	100	—	µs	
	Maximum programming count*1 *4	N	—	—	1000	Times	
Erase	Wait time after SWE bit setting*1	t_{sswe}	1	1	—	µs	
	Wait time after ESU bit setting*1	t_{sesu}	100	100	—	µs	
	Wait time after E bit setting*1 *5	t_{se}	10	10	100	ms	Erase time wait
	Wait time after E bit clear*1	t_{ce}	10	10	—	µs	
	Wait time after ESU bit clear*1	t_{cesu}	10	10	—	µs	
	Wait time after EV bit setting*1	t_{sev}	20	20	—	µs	

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	Ports 1, 3, A to F, H,J HTxD0, HTxD1 (excluding P34 and P35*7)	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
	P34, P35*7		V_{CC} – 2.5	—	—		I_{OH} = –100 µA
	Ports 1, 3, A to F, H, J HTxD0, HTxD1 (excluding P34 and P35*7)		3.5	—	—		I_{OH} = –1 mA
	PWM1A to PWM1H, PWM2A to PWM2H		PWMV_{CC} – 0.5	—	—		I_{OH} = –15 mA
Output low voltage	All output pins except PWM1A to PWM1H, PWM2A to PWM2H	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	PWM1A to PWM1H, PWM2A to PWM2H		—	—	0.5	V	I_{OL} = 15 mA
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0.5 V to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD2 to MD0		—	—	1.0		
	HRxD0, HRxD1, FWE		—	—	1.0		
	Ports 4, 9		—	—	1.0		V_{in} = 0.5 V to AV_{CC} – 0.5 V
Three-state leakage current (off state)	Ports 1, 3, A to F, H, J HTxD0, HTxD1	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 V to V_{CC} – 0.5 V

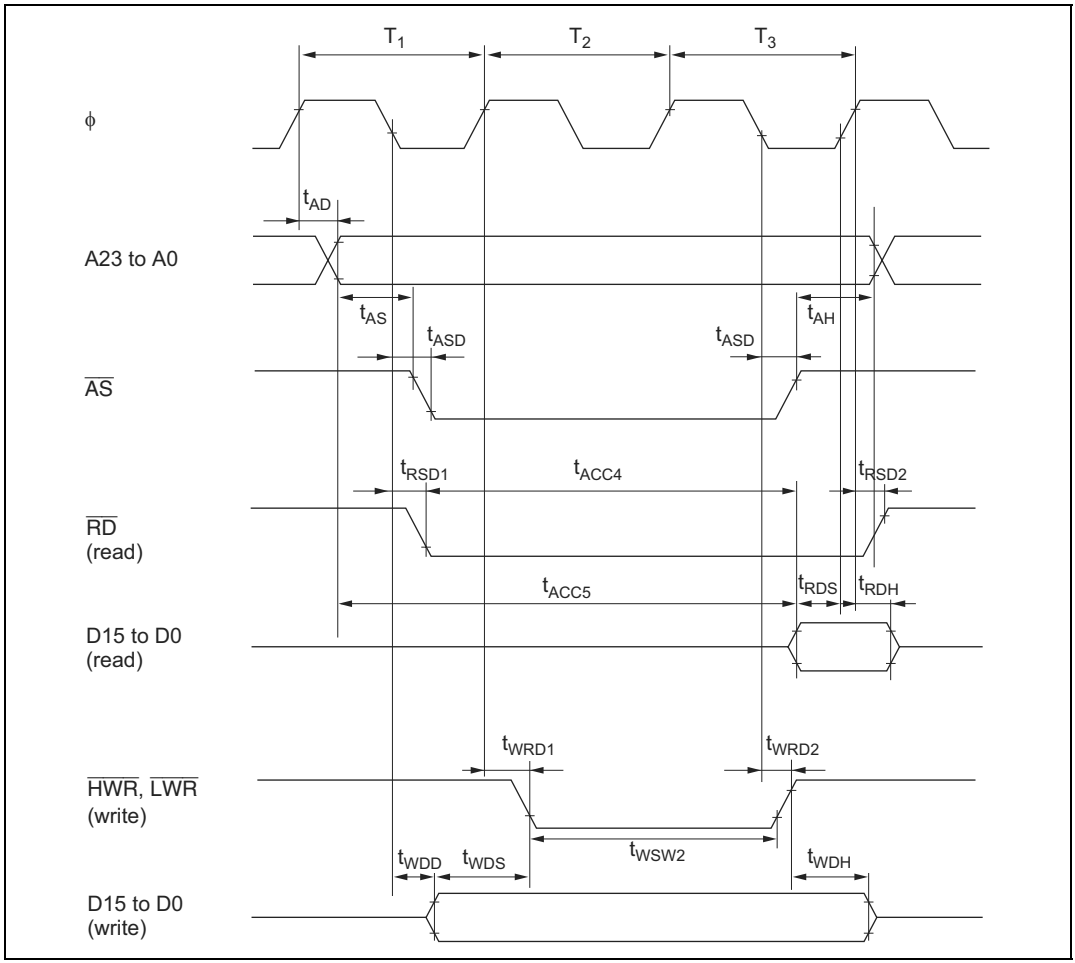


Figure 24-14 Basic Bus Timing (Three-State Access)

(5) Bit-Manipulation Instructions

Mnemonic	Operand Size	Addressing Mode/ Instruction Length (Bytes)							Operation	Condition Code					No. of States*1
		#xx	Rn	@ERn	@(d,ERn)	@–ERn/@ERn+	@aa	@@aa		I	H	N	Z	V	C	Advanced
BSET	BSET #xx:3,Rd	B	2						(#xx:3 of Rd8)←1	—	—	—	—	—	—	1
	BSET #xx:3,@ERd	B		4					(#xx:3 of @ERd)←1	—	—	—	—	—	—	4
	BSET #xx:3,@aa:8	B					4		(#xx:3 of @aa:8)←1	—	—	—	—	—	—	4
	BSET #xx:3,@aa:16	B					6		(#xx:3 of @aa:16)←1	—	—	—	—	—	—	5
	BSET #xx:3,@aa:32	B					8		(#xx:3 of @aa:32)←1	—	—	—	—	—	—	6
	BSET Rn,Rd	B	2						(Rn8 of Rd8)←1	—	—	—	—	—	—	1
	BSET Rn,@ERd	B		4					(Rn8 of @ERd)←1	—	—	—	—	—	—	4
	BSET Rn,@aa:8	B					4		(Rn8 of @aa:8)←1	—	—	—	—	—	—	4
	BSET Rn,@aa:16	B					6		(Rn8 of @aa:16)←1	—	—	—	—	—	—	5
	BSET Rn,@aa:32	B					8		(Rn8 of @aa:32)←1	—	—	—	—	—	—	6
BCLR	BCLR #xx:3,Rd	B	2						(#xx:3 of Rd8)←0	—	—	—	—	—	—	1
	BCLR #xx:3,@ERd	B		4					(#xx:3 of @ERd)←0	—	—	—	—	—	—	4
	BCLR #xx:3,@aa:8	B					4		(#xx:3 of @aa:8)←0	—	—	—	—	—	—	4
	BCLR #xx:3,@aa:16	B					6		(#xx:3 of @aa:16)←0	—	—	—	—	—	—	5
	BCLR #xx:3,@aa:32	B					8		(#xx:3 of @aa:32)←0	—	—	—	—	—	—	6
	BCLR Rn,Rd	B	2						(Rn8 of Rd8)←0	—	—	—	—	—	—	1
	BCLR Rn,@ERd	B		4					(Rn8 of @ERd)←0	—	—	—	—	—	—	4
	BCLR Rn,@aa:8	B					4		(Rn8 of @aa:8)←0	—	—	—	—	—	—	4
	BCLR Rn,@aa:16	B					6		(Rn8 of @aa:16)←0	—	—	—	—	—	—	5

MC6[1]—Message Control 6[1]	**H'F850**	**HCAN0**
MC6[2]—Message Control 6[2]	**H'F851**	**HCAN0**
MC6[3]—Message Control 6[3]	**H'F852**	**HCAN0**
MC6[4]—Message Control 6[4]	**H'F853**	**HCAN0**
MC6[5]—Message Control 6[5]	**H'F854**	**HCAN0**
MC6[6]—Message Control 6[6]	**H'F855**	**HCAN0**
MC6[7]—Message Control 6[7]	**H'F856**	**HCAN0**
MC6[8]—Message Control 6[8]	**H'F857**	**HCAN0**

MC6[1]

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	DLC3	DLC2	DLC1	DLC0
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data Length Code

0	0	0	0	Data length = 0 bytes
			1	Data length = 1 byte
		1	0	Data length = 2 bytes
			1	Data length = 3 bytes
	1	0	0	Data length = 4 bytes
			1	Data length = 5 bytes
		1	0	Data length = 6 bytes
			1	Data length = 7 bytes
1	0/1	0/1	0/1	Data length = 8 bytes

MC6[2]

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MC6[3]

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MD9[1]—Message Data 9[1]	**H'F8F8**	**HCAN0**
MD9[2]—Message Data 9[2]	**H'F8F9**	**HCAN0**
MD9[3]—Message Data 9[3]	**H'F8FA**	**HCAN0**
MD9[4]—Message Data 9[4]	**H'F8FB**	**HCAN0**
MD9[5]—Message Data 9[5]	**H'F8FC**	**HCAN0**
MD9[6]—Message Data 9[6]	**H'F8FD**	**HCAN0**
MD9[7]—Message Data 9[7]	**H'F8FE**	**HCAN0**
MD9[8]—Message Data 9[8]	**H'F8FF**	**HCAN0**

	Bit	7	6	5	4	3	2	1	0
MDx[1]	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MDx[2]	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MDx[3]	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MDx[4]	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MDx[5]	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MDx[6]	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MDx[7]	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MDx[8]	Initial value	*	*	*	*	*	*	*	*
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

*: Undefined
x = 0 to 15