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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78l051a24dl

1. GENERAL DESCRIPTION

The W78L051 is an 8-bit microcontroller which can accommodate a wide supply voltage range with low power consumption. The instruction set for the W78L051 is fully compatible with the standard 8051. The W78L051 contains an 4K bytes Flash EPROM; a 128 bytes RAM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 4-bit I/O port P4; two 16-bit timer/counters; a hardware watchdog timer and a serial port. These peripherals are supported by seven sources two-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W78L051 allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

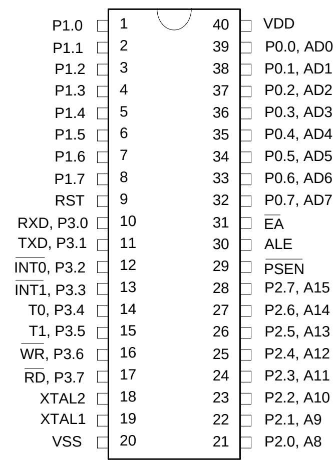
The W78L051 microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

2. FEATURES

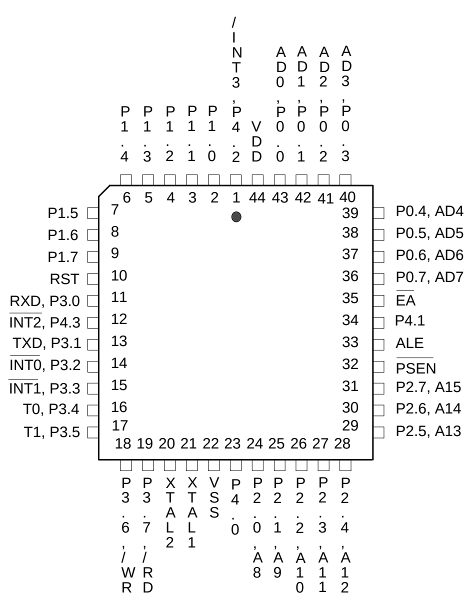
- Fully static design 8-bit CMOS microcontroller
- Wide supply voltage of 2.4V to 5.5V
- 128 bytes of on-chip scratchpad RAM
- 4 KB electrically erasable/programmable Flash EPROM
- 64 KB program memory address space
- 64 KB data memory address space
- Four 8-bit bi-directional ports
- One extra 4-bit bit-addressable I/O port, additional $\overline{\text{INT2}}$ / $\overline{\text{INT3}}$ *(available on 44-pin PLCC/QFP package)*
- Two 16-bit timer/counters
- One full duplex serial port (UART)
- Watchdog Timer
- seven sources, two-level interrupt capability
- EMI reduction mode
- Built-in power management
- Code protection mechanism
- Packages:
  - Lead Free (RoHS) DIP 40: W78L051A24DL
  - Lead Free (RoHS) PLCC 44: W78L051A24PL
  - Lead Free (RoHS) PQFP 44: W78L051A24FL

3. PIN CONFIGURATIONS

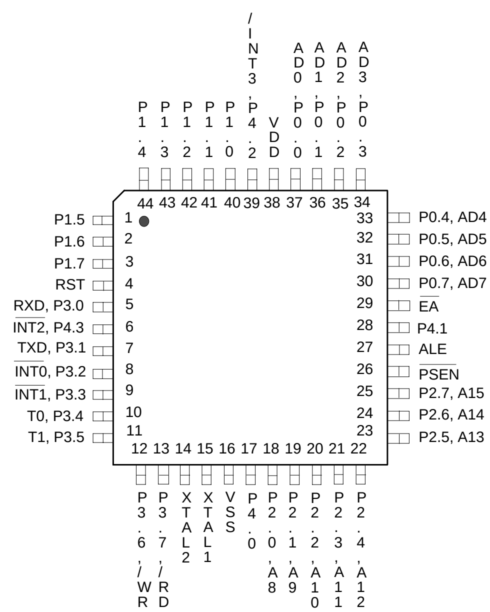
40-Pin DIP



44-Pin PLCC



44-Pin QFP



4. PIN DESCRIPTION

SYMBOL	DESCRIPTIONS
$\overline{EA}$	**EXTERNAL ACCESS ENABLE**: This pin forces the processor to execute out of external ROM. It should be kept high to access internal ROM. The ROM address and data will not be presented on the bus if $\overline{EA}$ pin is high and the program counter is within on-chip ROM area.
$\overline{PSEN}$	**PROGRAM STORE ENABLE**: $\overline{PSEN}$ enables the external ROM data onto the Port 0 address/ data bus during fetch and MOVC operations. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs from this pin.
ALE	**ADDRESS LATCH ENABLE**: ALE is used to enable the address latch that separates the address from the data on Port 0.
RST	**RESET**: A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	**CRYSTAL1**: This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	**CRYSTAL2**: This is the crystal oscillator output. It is the inversion of XTAL1.
VSS	**GROUND**: Ground potential
VDD	**POWER SUPPLY**: Supply voltage for operation.
P0.0–P0.7	**PORT 0**: Port 0 is a bi-directional I/O port which also provides a multiplexed low order address/data bus during accesses to external memory. The Port 0 is also an open-drain port and external pull-ups need to be connected while in programming.
P1.0–P1.7	**PORT 1**: Port 1 is a bi-directional I/O port with internal pull-ups. The bits have alternate functions which are described below: T2(P1.0): Timer/Counter 2 external count input T2EX(P1.1): Timer/Counter 2 Reload/Capture control
P2.0–P2.7	**PORT 2**: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.
P3.0–P3.7	**PORT 3**: Port 3 is a bi-directional I/O port with internal pull-ups. All bits have alternate functions, which are described below: RXD(P3.0) : Serial Port receiver input TXD(P3.1) : Serial Port transmitter output $\overline{INT0}$ (P3.2) : External Interrupt 0 $\overline{INT1}$(P3.3) : External Interrupt 1 T0(P3.4) : Timer 0 External Input T1(P3.5) : Timer 1 External Input $\overline{WR}$ (P3.6) :External Data Memory Write Strobe $\overline{RD}$ (P3.7) : External Data Memory Read Strobe
P4.0–P4.3	**PORT 4:** Another bit-addressable bidirectional I/O port P4. P4.3 and P4.2 are alternative function pins. It can be used as general I/O port or external interrupt input sources ($\overline{INT2}$ / $\overline{INT3}$).

5. FUNCTIONAL DESCRIPTION

The W78L051 architecture consists of a core controller surrounded by various registers, five general purpose I/O ports, 128 bytes of RAM, two timer/counters, and a serial port. The processor supports 111 different opcodes and references both a 64K program address space and a 64K data storage space.

New Defined Peripheral

In order to be more suitable for I/O, an extra 4-bit bit-addressable port P4 and two external interrupt $\overline{INT2}$, $\overline{INT3}$ has been added to either the PLCC or QFP 44 pin package. And description follows:

1. $\overline{INT2}$ / $\overline{INT3}$

Two additional external interrupts, $\overline{INT2}$ and $\overline{INT3}$, whose functions are similar to those of external interrupt 0 and 1 in the standard 80C52. The functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the standard 80C52. Its address is at 0C0H. To set/clear bits in the XICON register, one can use the "SETB (/CLR) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON.

XICON - external interrupt control (C0H)

PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

PX3: External interrupt 3 priority high if set
EX3: External interrupt 3 enable if set
IE3: If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced
IT3: External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software
PX2: External interrupt 2 priority high if set
EX2: External interrupt 2 enable if set
IE2: If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced
IT2: External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

Seven-source interrupt informations:

INTERRUPT SOURCE	VECTOR ADDRESS	POLLING SEQUENCE WITHIN PRIORITY LEVEL	ENABLE REQUIRED SETTINGS	INTERRUPT TYPE EDGE/LEVEL
External Interrupt 0	03H	0 (highest)	IE.0	TCON.0
Timer/Counter 0	0BH	1	IE.1	-
External Interrupt 1	13H	2	IE.2	TCON.2
Timer/Counter 1	1BH	3	IE.3	-
Serial Port	23H	4	IE.4	-
External Interrupt 2	33H	5	XICON.2	XICON.0
External Interrupt 3	3BH	6 (lowest)	XICON.6	XICON.3

Watchdog Timer

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a system reset can also be caused if it is enabled. The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. The watchdog time-out selection will result in different time-out values depending on the clock speed. The Watchdog timer will de disabled on reset. In general, software should restart the Watchdog timer to put it into a known state. The control bits that support the Watchdog timer are discussed below.

Watchdog Timer Control Register

Bit:	7	6	5	4	3	2	1	0
	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0

Mnemonic: WDTC Address: 8FH

ENW : Enable watch-dog if set.

CLRW: Clear watch-dog timer and prescaler if set. This flag will be cleared automatically

WIDL : If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is disabled under IDLE mode. Default is cleared.

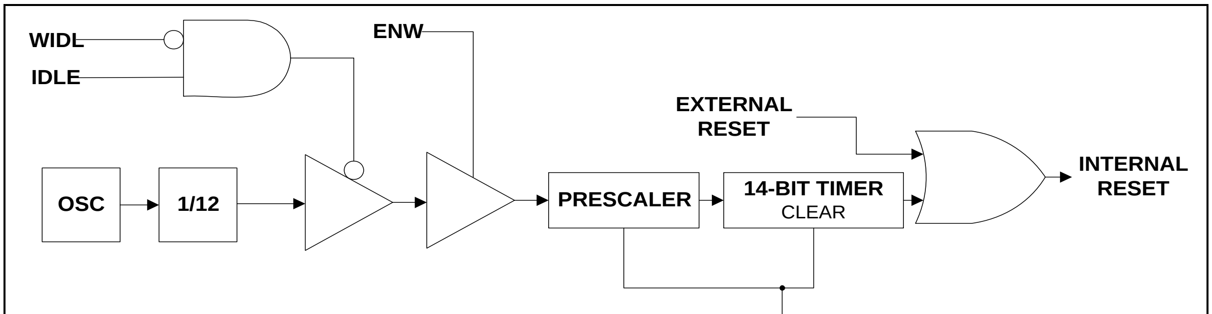
PS2, PS1, PS0: Watch-dog prescaler timer select. Prescaler is selected when set PS2–0 as follows:

PS2 PS1 PS0	PRESCALER SELECT
0 0 0	2
0 1 0	4
0 0 1	8
0 1 1	16
1 0 0	32
1 0 1	64
1 1 0	128
1 1 1	256

The time-out period is obtained using the following equation:

$$\frac{1}{OSC} \times 2^{14} \times \text{PRESCALER} \times 1000 \times 12 \text{ mS}$$

Before Watchdog time-out occurs, the program must clear the 14-bit timer by writing 1 to WDTC.6 (CLRW). After 1 is written to this bit, the 14-bit timer, prescaler and this bit will be reset on the next instruction cycle. The Watchdog timer is cleared on reset.



Watchdog Timer Block Diagram

Typical Watch-Dog time-out period when OSC = 20 MHz

PS2 PS1 PS0	WATCHDOG TIME-OUT PERIOD
0 0 0	19.66 mS
0 1 0	39.32 mS
0 0 1	78.64 mS
0 1 1	157.28 mS
1 0 0	314.57mS
1 0 1	629.14 mS
1 1 0	1.25 S
1 1 1	2.50 S

Clock

The W78L051 is designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used. This makes the W78L051 relatively insensitive to duty cycle variations in the clock. The W78L051 incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground. An external clock source should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator.

Power Management

Idle Mode

The idle mode is entered by setting the IDL bit in the PCON register. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

Power-down Mode

When the PD bit of the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator. The only way to exit power-down mode is by a reset.

Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the W78L051 is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

6. ON-CHIP FLASH EPROM CHARACTERISTICS

The W78L051 has several modes to program the on-chip Flash EPROM. All these operations are configured by the pins RST, ALE, $\overline{PSEN}$, A9CTRL(P3.0), A13CTRL(P3.1), A14CTRL(P3.2), OECTRL(P3.3), $\overline{CE}$ (P3.6), $\overline{OE}$ (P3.7), A0(P1.0) and V_{PP}($\overline{EA}$). Moreover, the A15–A0(P2.7–P2.0, P1.7–P1.0) and the D7–D0(P0.7–P0.0) serve as the address and data bus respectively for these operations.

Read Operation

This operation is supported for customer to read their code and the Security bits. The data will not be valid if the Lock bit is programmed to low.

Output Disable Condition

When the $\overline{OE}$ is set to high, no data output appears on the D7... D0.

Program Operation

This operation is used to program the data to Flash EPROM and the security bits. Program operation is done when the V_{PP} is reach to V_{CP} (12.5V) level, $\overline{CE}$ set to low, and $\overline{OE}$ set to high.

Program Verify Operation

All the programming data must be checked after program operations. This operation should be performed after each byte is programmed; it will ensure a substantial program margin.

Erase Operation

An erase operation is the only way to change data from 0 to 1. This operation will erase all the Flash EPROM cells and the security bits from 0 to 1. This erase operation is done when the V_{PP} is reach to V_{EP} level, $\overline{CE}$ set to low, and $\overline{OE}$ set to high.

Erase Verify Operation

After an erase operation, all of the bytes in the chip must be verified to check whether they have been successfully erased to 1 or not. The erase verify operation automatically ensures a substantial erase margin. This operation will be done after the erase operation if V_{PP} = V_{EP} (14.5V), $\overline{CE}$ is high and $\overline{OE}$ is low.

Program/Erase Inhibit Operation

This operation allows parallel erasing or programming of multiple chips with different data. When P3.6($\overline{CE}$) = V_{IH}, P3.7($\overline{OE}$) = V_{IH}, erasing or programming of non-targeted chips is inhibited. So, except for the P3.6 and P3.7 pins, the individual chips may have common inputs.

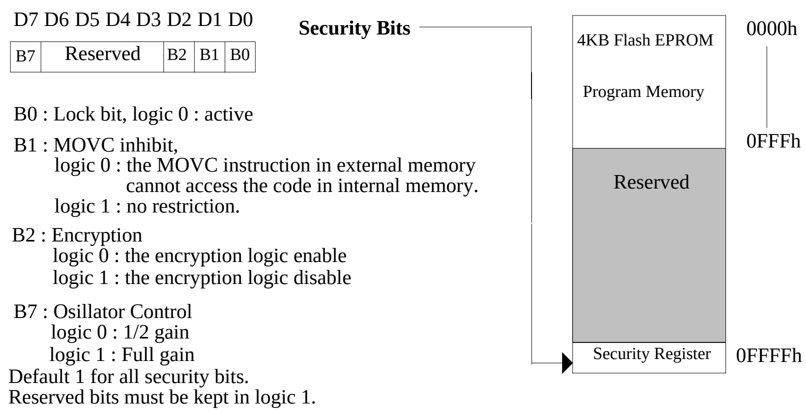
OPERATIONS	P3.0 (A9 CTRL)	P3.1 (A13 CTRL)	P3.2 (A14 CTRL)	P3.3 (OE CTRL)	P3.6 ($\overline{CE}$)	P3.7 ($\overline{OE}$)	$\overline{EA}$ (VPP)	P2, P1 (A15..A0)	P0 (D7..D0)	NOTE
Read	0	0	0	0	0	0	1	Address	Data Out	
Output Disable	0	0	0	0	0	1	1	X	Hi-Z	
Program	0	0	0	0	0	1	V_{CP}	Address	Data In	
Program Verify	0	0	0	0	1	0	V_{CP}	Address	Data Out	@3
Erase	1	0	0	0	0	1	V_{EP}	A0:0, others: X	Data In 0FFH	@4
Erase Verify	1	0	0	0	1	0	V_{EP}	Address	Data Out	@5
Program/Erase Inhibit	X	0	0	0	1	1	V_{CP}/ V_{EP}	X	X	

Notes:

1. All these operations happen in RST = V_{IH}, ALE = V_{IL} and $\overline{PSEN}$ = V_{IH}.
2. V_{CP} = 12.5V, V_{EP} = 14.5V, V_{IH} = V_{DD}, V_{IL} = Vss.
3. The program verify operation follows behind the program operation.
4. This erase operation will erase all the on-chip Flash EPROM cells and the Security bits.
5. The erase verify operation follows behind the erase operation.

7. SECURITY BITS

During the on-chip Flash EPROM operation mode, the Flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of Flash EPROM and those operations on it are described below. The W78L051 has a Special Setting Register, the Security Register, which can not be accessed in normal mode. The Security register can only be accessed from the Flash EPROM operation mode. Those bits of the Security Registers can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The Security Register is addressed in the Flash EPROM operation mode by address #0FFFFh.



Special Setting Register

9. DC CHARACTERISTICS

V_{SS} = 0V, T_A = 25° C, unless otherwise specified.

PARAMETER	SYM.	SPECIFICATION		UNIT	TEST CONDITIONS
		MIN.	MAX.		
Operating Voltage	V_{DD}	2.4	5.5	V	
Operating Current	I_{DD}	-	20	mA	No load V_{DD} = 5.5V
		-	3	mA	No load V_{DD} = 2.4V
Idle Current	I_{IDLE}	-	6	mA	V_{DD} = 5.5V, F_{OSC} = 20 MHz
		-	1.5	mA	V_{DD} = 2.4V, F_{OSC} = 12 MHz
Power Down Current	I_{PWDN}	-	50	μA	V_{DD} = 5.5V, F_{OSC} = 20 MHz
		-	20	μA	V_{DD} = 2.4V, F_{OSC} = 12 MHz
Input Current P1, P2, P3, P4	I_{IN1}	-50	+10	μA	V_{DD} = 5.5V V_{IN} = 0V or V_{DD}
Input Current RST	I_{IN2}	-10	+300	μA	V_{DD} = 5.5V 0 < V_{IN} < V_{DD}
Input Leakage Current P0, $\overline{EA}$	I_{LK}	-10	+10	μA	V_{DD} = 5.5V 0V < V_{IN} < V_{DD}
Logic 1 to 0 Transition Current P1, P2, P3, P4	I_{TL} [*4]	-500	-	μA	V_{DD} = 5.5V V_{IN} = 2.0V
Input Low Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IL1}	0	0.8	V	V_{DD} = 4.5V
		0	0.5	V	V_{DD} = 2.4V
Input Low Voltage RST[*1]	V_{IL2}	0	0.8	V	V_{DD} = 4.5V
		0	0.3	V	V_{DD} = 2.4V
Input Low Voltage XTAL1 [*3]	V_{IL3}	0	0.8	V	V_{DD} = 4.5V
		0	0.6	V	V_{DD} = 2.4V
Input High Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IH1}	2.4	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.4	V_{DD} +0.2	V	V_{DD} = 2.4V
Input High Voltage RST[*1]	V_{IH2}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.7	V_{DD} +0.2	V	V_{DD} = 2.4V
Input High Voltage XTAL1 [*3]	V_{IH3}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.6	V_{DD} +0.2	V	V_{DD} = 2.4V
Output Low Voltage P1, P2, P3, P4	V_{OL1}	-	0.45	V	V_{DD} = 4.5V, I_{OL} = +2 mA
		-	0.25	V	V_{DD} = 2.4V, I_{OL} = +1 mA
Output Low Voltage P0, ALE, $\overline{PSEN}$ [*2]	V_{OL2}	-	0.45	V	V_{DD} = 4.5V, I_{OL} = +4 mA
		-	0.25	V	V_{DD} = 2.4V, I_{OL} = +2 mA

DC Characteristics, continued

PARAMETER	SYM.	SPECIFICATION		UNIT	TEST CONDITIONS
		MIN.	MAX.		
Sink Current P1, P2, P3, P4	I_{SK1}	4	12	mA	V_{DD} = 4.5V, Vin = 0.45V
		1.8	5.4	mA	V_{DD} = 2.4V, Vin = 0.45V
Sink Current P0, ALE, $\overline{PSEN}$	I_{SK2}	8	16	mA	V_{DD} = 4.5V, Vin = 0.45V
		4.5	9	mA	V_{DD} = 2.4V, Vin = 0.45V
Output High Voltage P1, P2, P3, P4	V_{OH1}	2.4	-	V	V_{DD} = 4.5V, I_{OH} = -100 μA
		1.4	-	V	V_{DD} = 2.4V, I_{OH} = -8 μA
Output High Voltage P0, ALE, $\overline{PSEN}$ [*2]	V_{OH2}	2.4	-	V	V_{DD} = 4.5V, I_{OH} = -400 μA
		1.4	-	V	V_{DD} = 2.4V, I_{OH} = -200 μA
Source Current P1, P2, P3, P4	I_{SR1}	-100	-250	μA	V_{DD} = 4.5V, Vin = 2.4V
		-20	-50	μA	V_{DD} = 2.4V, Vin = 1.4V
Source Current P0, ALE, $\overline{PSEN}$	I_{SR2}	-8	-14	mA	V_{DD} = 4.5V, Vin = 2.4V
		-1.9	-3.8	mA	V_{DD} = 2.4V, Vin = 1.4V

Notes:
*1. RST pin is a Schmitt trigger input.
*2. P0, ALE and /PSEN are tested in the external access mode.
*3. XTAL1 is a CMOS input.
*4. Pins of P1, P2, P3, P4 can source a transition current when they are being externally driven from 1 to 0.

Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{RD}$ Low	TDAR	3 TCP -Δ	-	3 TCP +Δ	nS	1, 2
$\overline{RD}$ Low to Data Valid	TDDA	-	-	4 TCP	nS	1
Data Hold from $\overline{RD}$ High	TDDH	0	-	2 TCP	nS	
Data Float from $\overline{RD}$ High	TDDZ	0	-	2 TCP	nS	
$\overline{RD}$ Pulse Width	TDRD	6 TCP -Δ	6 TCP	-	nS	2

Notes:

1. Data memory access time is 8 TCP.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Write Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{WR}$ Low	TDAW	3 TCP -Δ	-	3 TCP +Δ	nS
Data Valid to $\overline{WR}$ Low	TDAD	1 TCP -Δ	-	-	nS
Data Hold from $\overline{WR}$ High	TDWD	1 TCP -Δ	-	-	nS
$\overline{WR}$ Pulse Width	TDWR	6 TCP -Δ	6 TCP	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	TPDS	1 TCP	-	-	nS
Port Input Hold from ALE Low	TPDH	0	-	-	nS
Port Output to ALE	TPDA	1 TCP	-	-	nS

Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

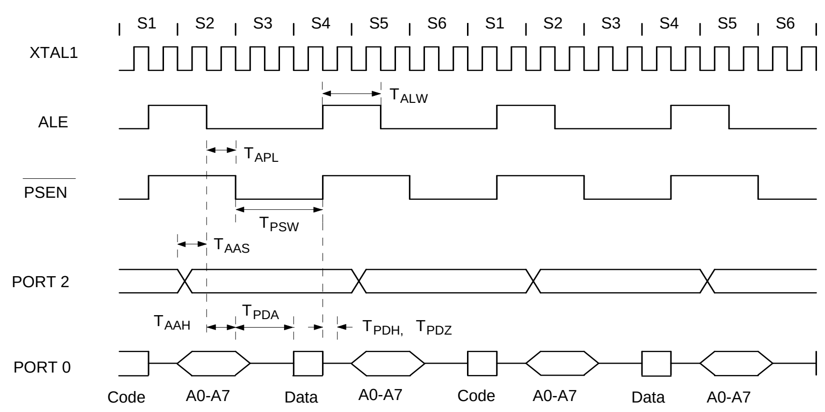
Program Operation

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
VPP Setup Time	TVPS	2.0	-	-	µS
Data Setup Time	TDS	2.0	-	-	µS
Data Hold Time	TDH	2.0	-	-	µS
Address Setup Time	TAS	2.0	-	-	µS
Address Hold Time	TAH	0	-	-	µS
$\overline{CE}$ Program Pulse Width for Program Operation	TPWP	290	300	310	µS
OECTRL Setup Time	TOCS	2.0	-	-	µS
OECTRL Hold Time	TOCH	2.0	-	-	µS
$\overline{OE}$ Setup Time	TOES	2.0	-	-	µS
$\overline{OE}$ High to Output Float	TDFP	0	-	130	nS
Data Valid from $\overline{OE}$	TOEV	-	-	150	nS

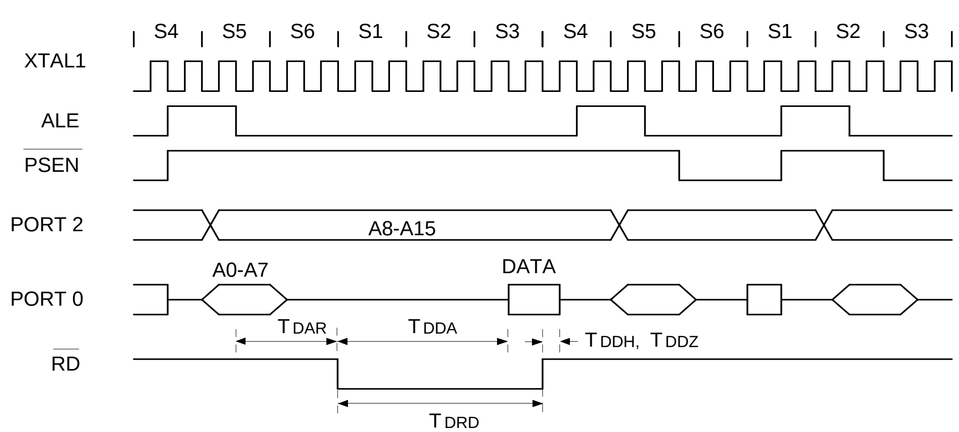
Note: Flash data can be accessed only in flash mode. The RST pin must pull in VIH status, the ALE pin must pull in VIL status, and the $\overline{PSEN}$ pin must pull in VIH status.

11. TIMING WAVEFORMS

Program Fetch Cycle

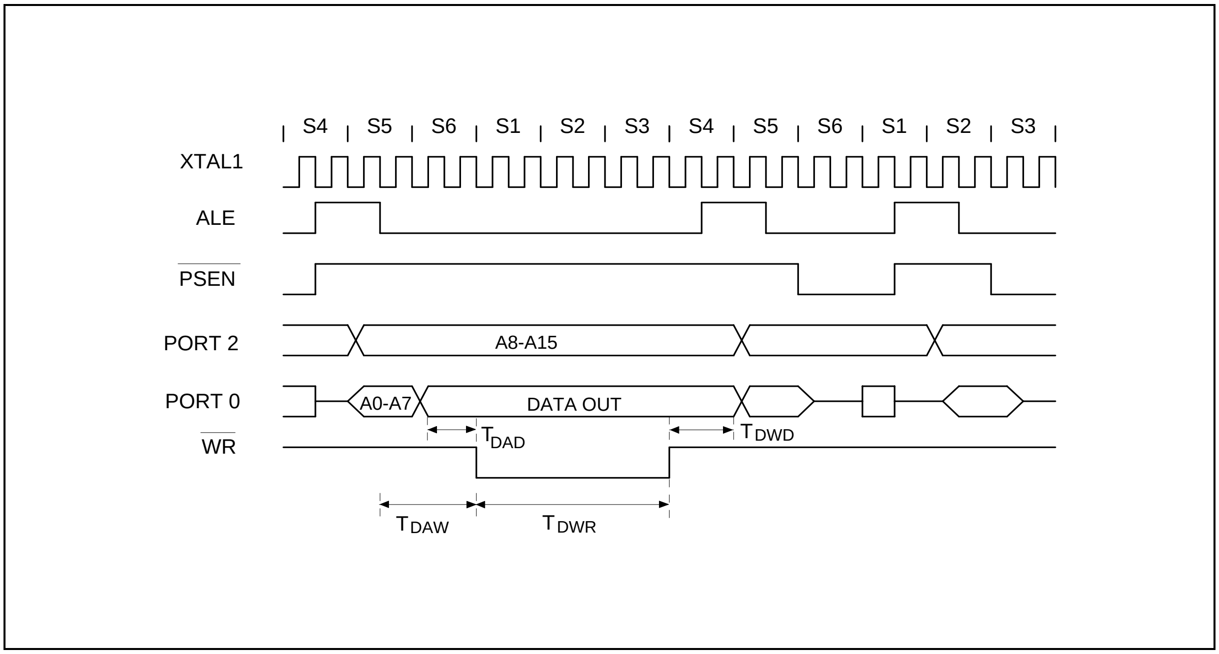


Data Read Cycle

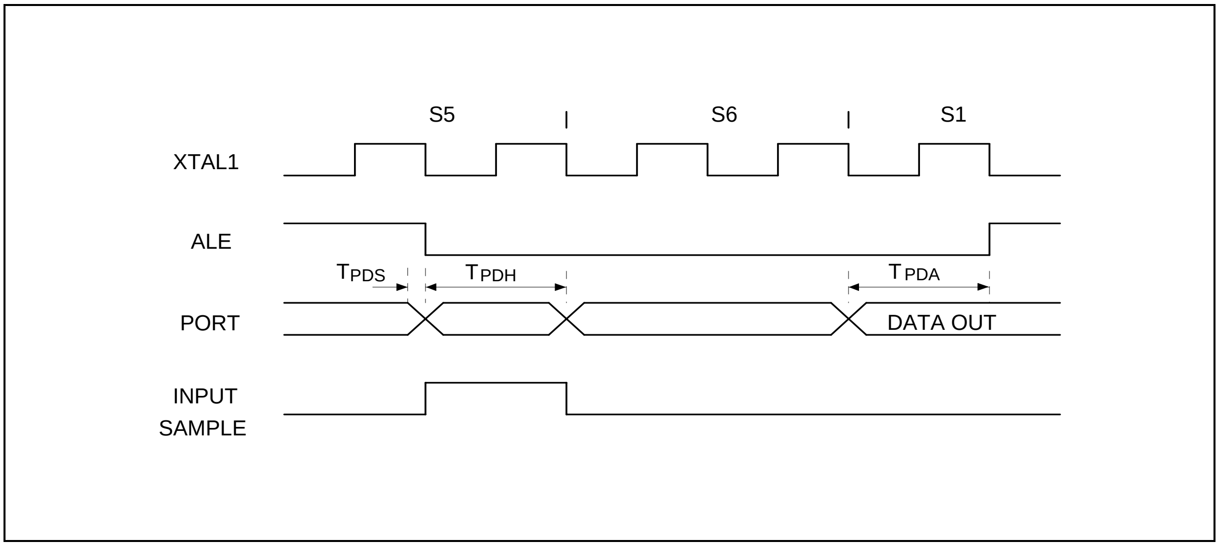


Timing Waveforms, continued

Data Write Cycle

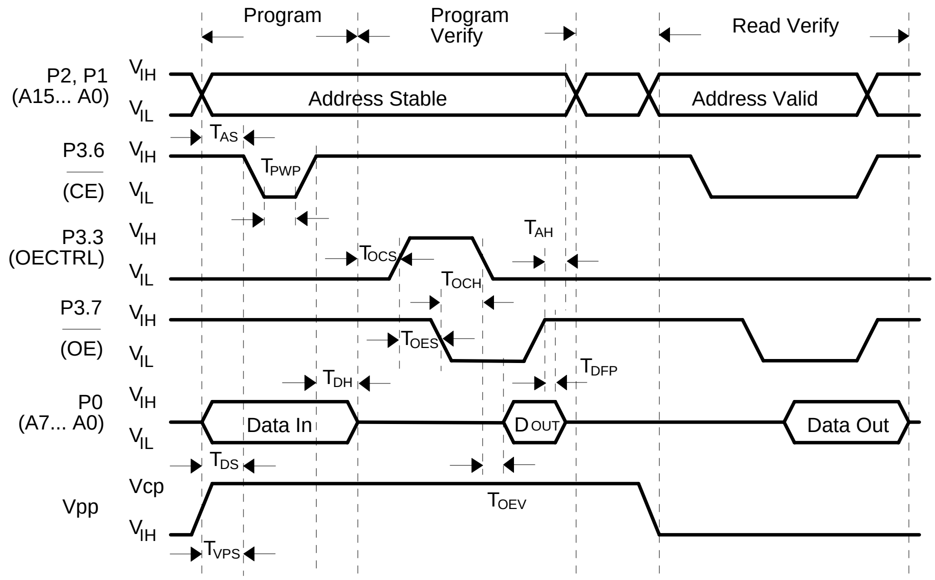


Port Access Cycle



Timing Waveforms, continued

Program Operation



Typical Application Circuits, continued

Expanded External Data Memory and Oscillator

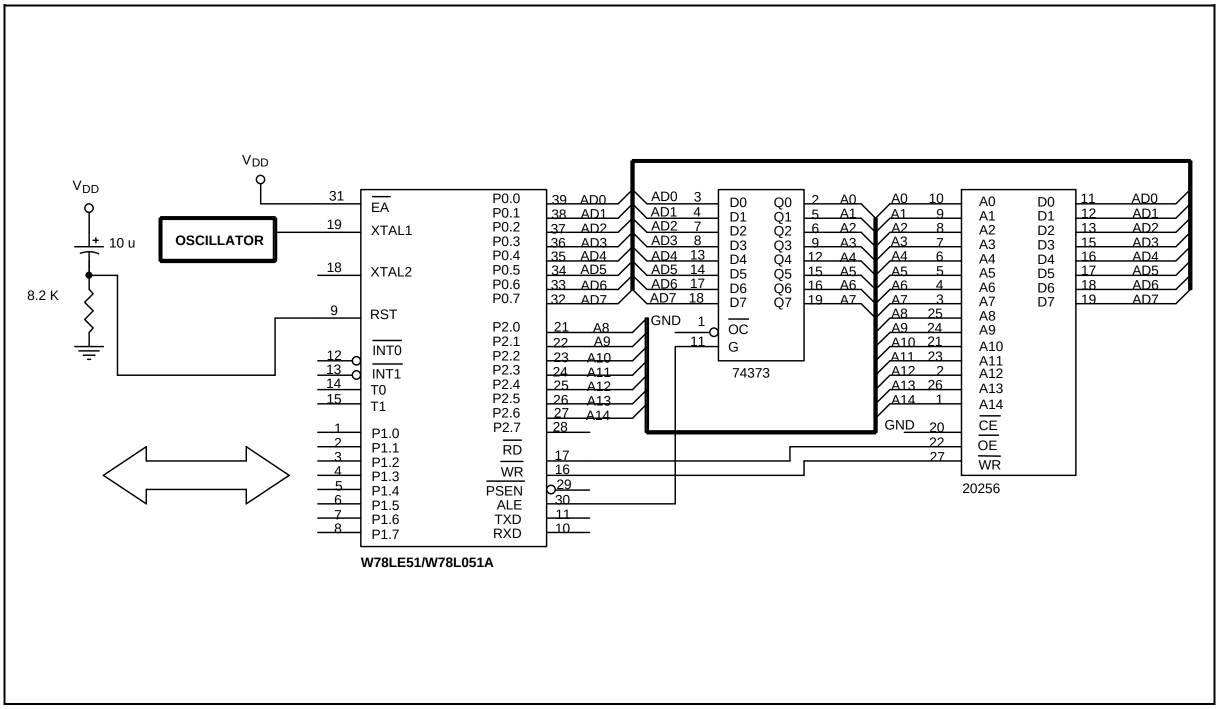
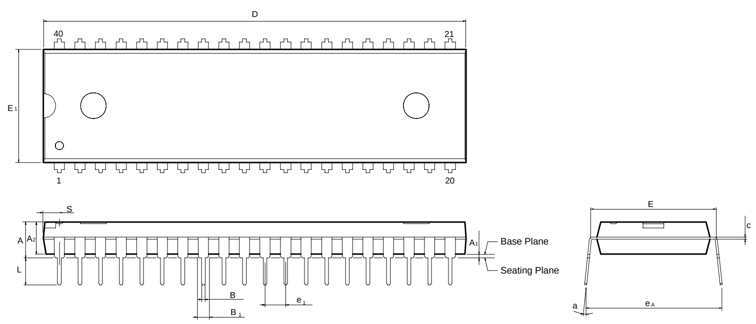


Figure B

13. PACKAGE DIMENSIONS

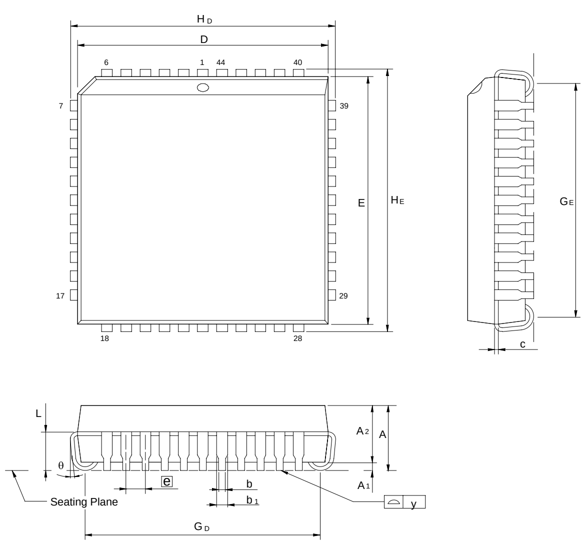
40-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.334
A_1	0.010	—	—	0.254	—	—
A_2	0.150	0.155	0.160	3.81	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.048	0.050	0.054	1.219	1.27	1.372
c	0.008	0.010	0.014	0.203	0.254	0.356
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.986	15.24	15.494
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.286	2.54	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.01
S	—	—	0.090	—	—	2.286

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

44-pin PLCC

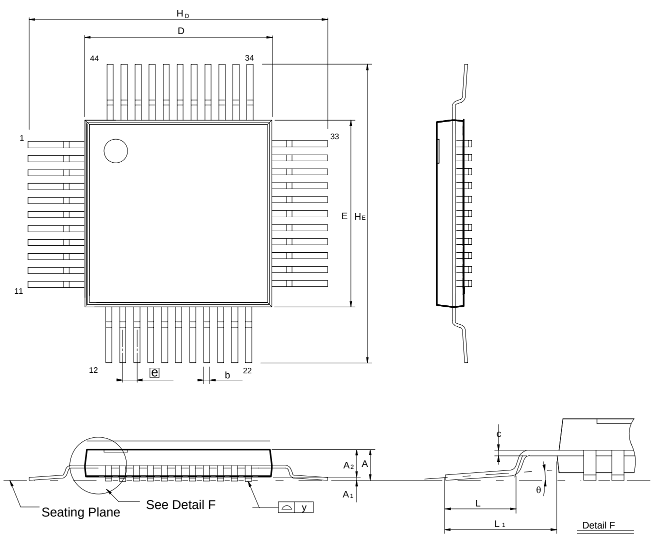


Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

Package Dimensions, continued

44-pin PQFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

14. REVISION HISTORY

VERSION	DATE	PAGE	REASONS FOR CHANGE
A3	December 2000		-
A4	April 19, 2005	22	Add Important Notice
A5	March 7, 2006	2	Add lead-free parts
A6	November 6, 2006		Remove block diagram
		2	Remove all Leaded parts
		16	Revise Operating speed to 20MHz

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