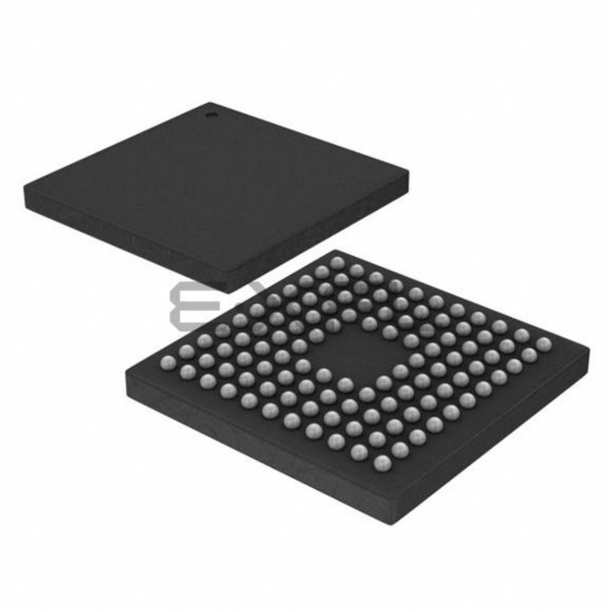
Silicon Labs - EFM32GG890F1024G-E-BGA112 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	90
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-BGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg890f1024g-e-bga112

2.1.19 Backup Real Time Counter (BURTC)

The Backup Real Time Counter (BURTC) contains a 32-bit counter and is clocked either by a 32.768 kHz crystal oscillator, a 32.768 kHz RC oscillator or a 1 kHz ULFRCO. The BURTC is available in all Energy Modes and it can also run in backup mode, making it operational even if the main power should drain out.

2.1.20 Low Energy Timer (LETIMER)

The unique LETIMER^{TM}, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

2.1.21 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

2.1.22 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.23 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.24 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

2.1.25 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

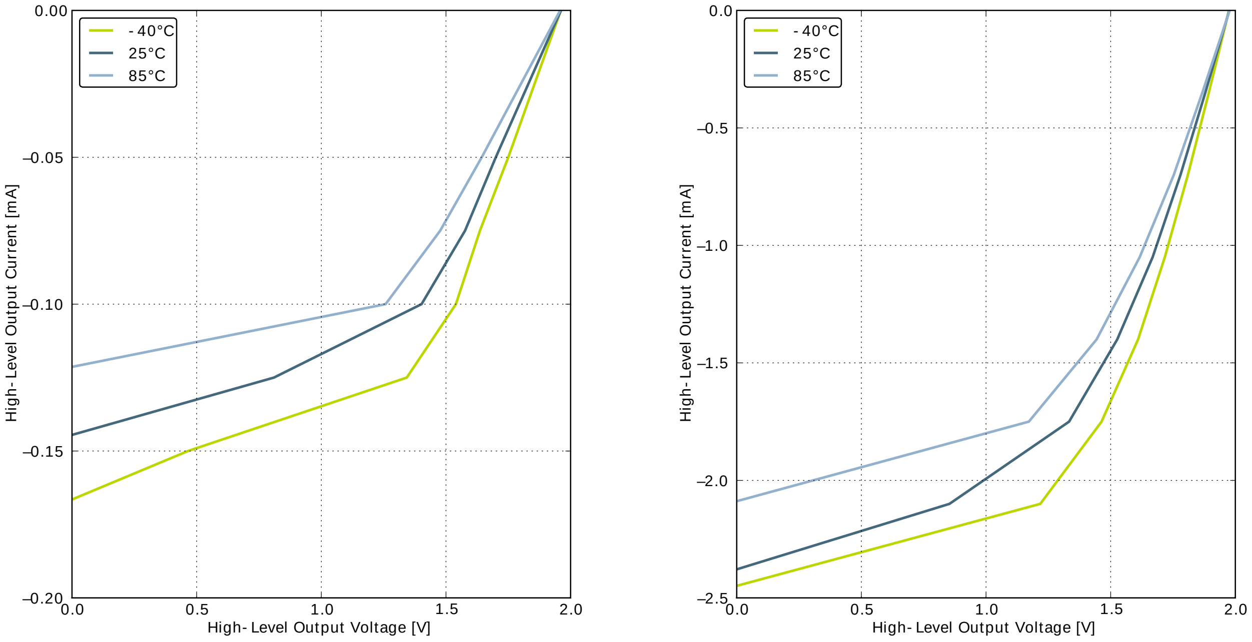
2.1.26 Operational Amplifier (OPAMP)

The EFM32GG890 features 3 Operational Amplifiers. The Operational Amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors etc.

2.1.27 Low Energy Sensor Interface (LESENSE)

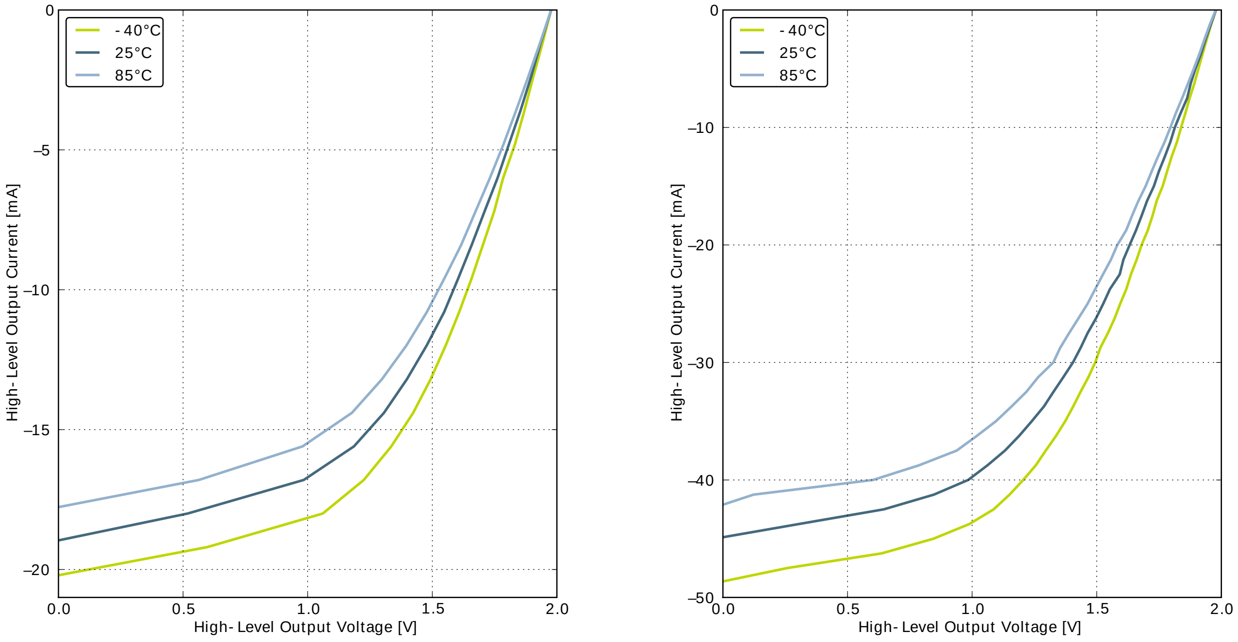
The Low Energy Sensor Interface (LESENSE^{TM}), is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators and DAC, LESENSE

Figure 3.5. Typical High-Level Output Current, 2V Supply Voltage



GPIO_Px_CTRL DRIVEMODE = LOWEST

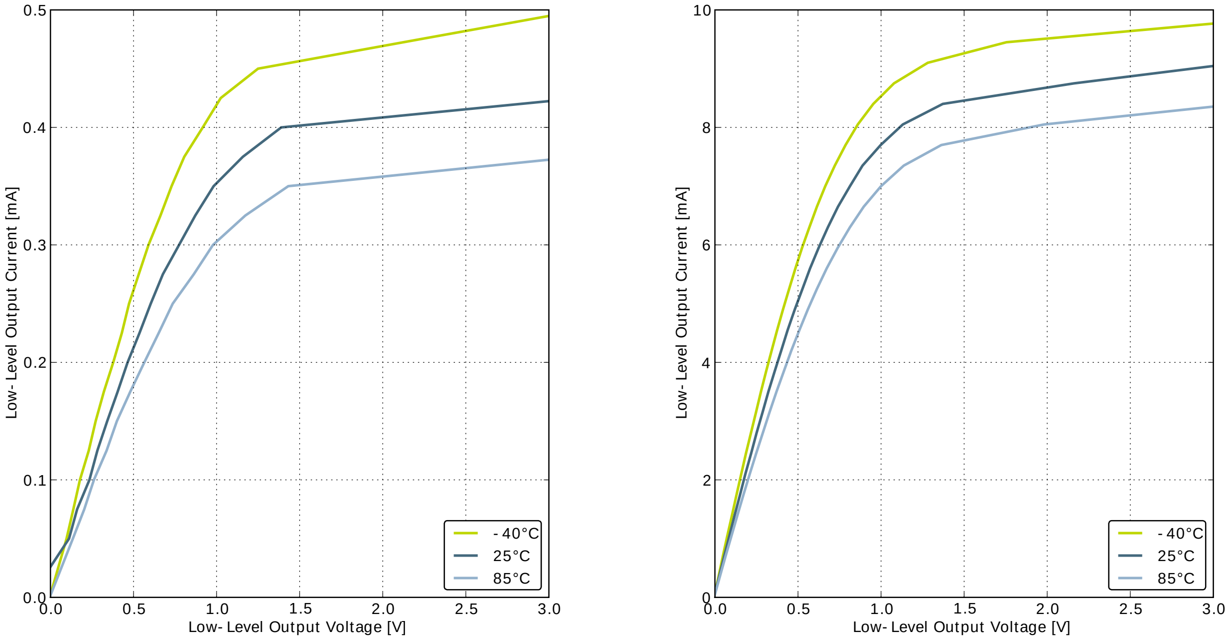
GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

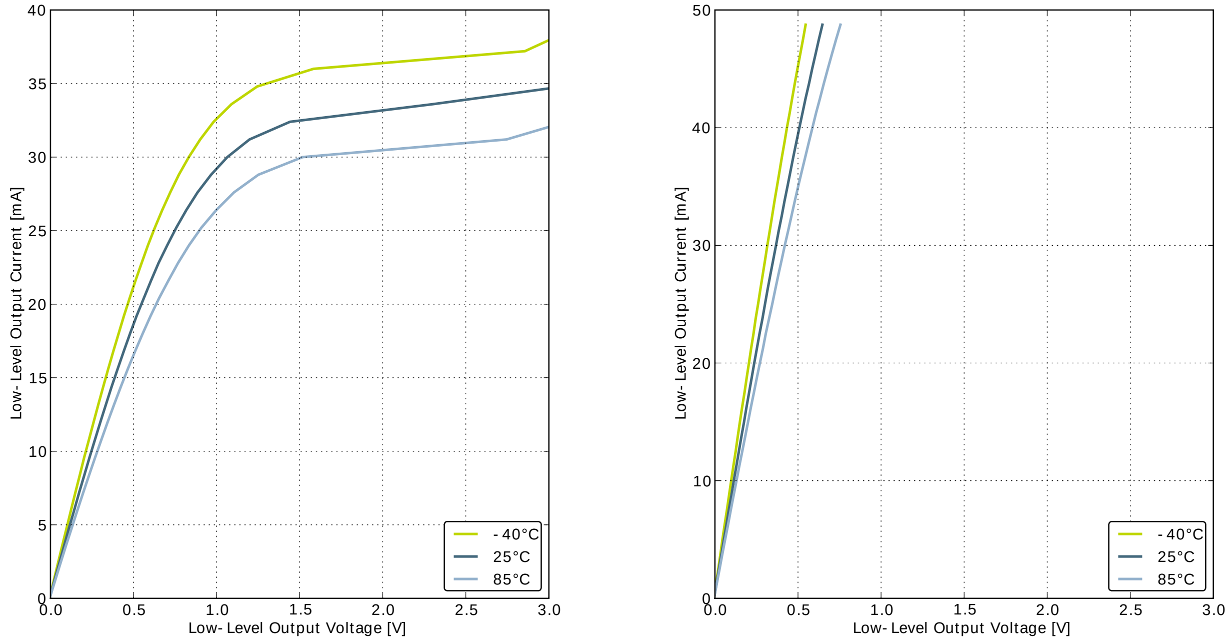
GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.6. Typical Low-Level Output Current, 3V Supply Voltage



GPIO_Px_CTRL DRIVEMODE = LOWEST

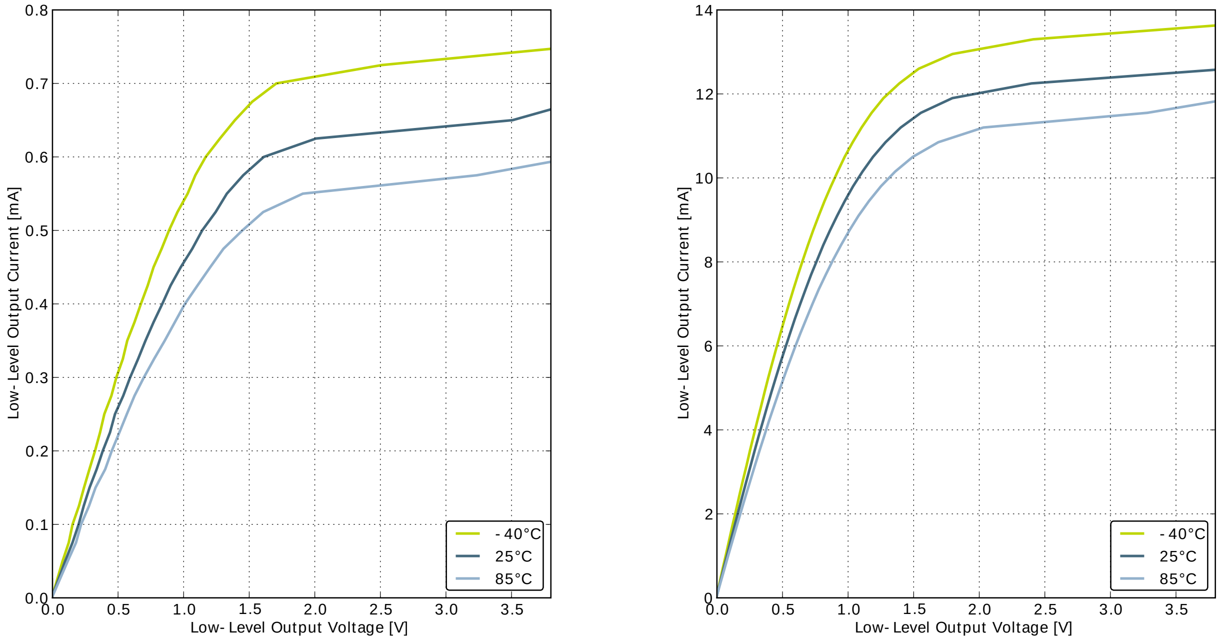
GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

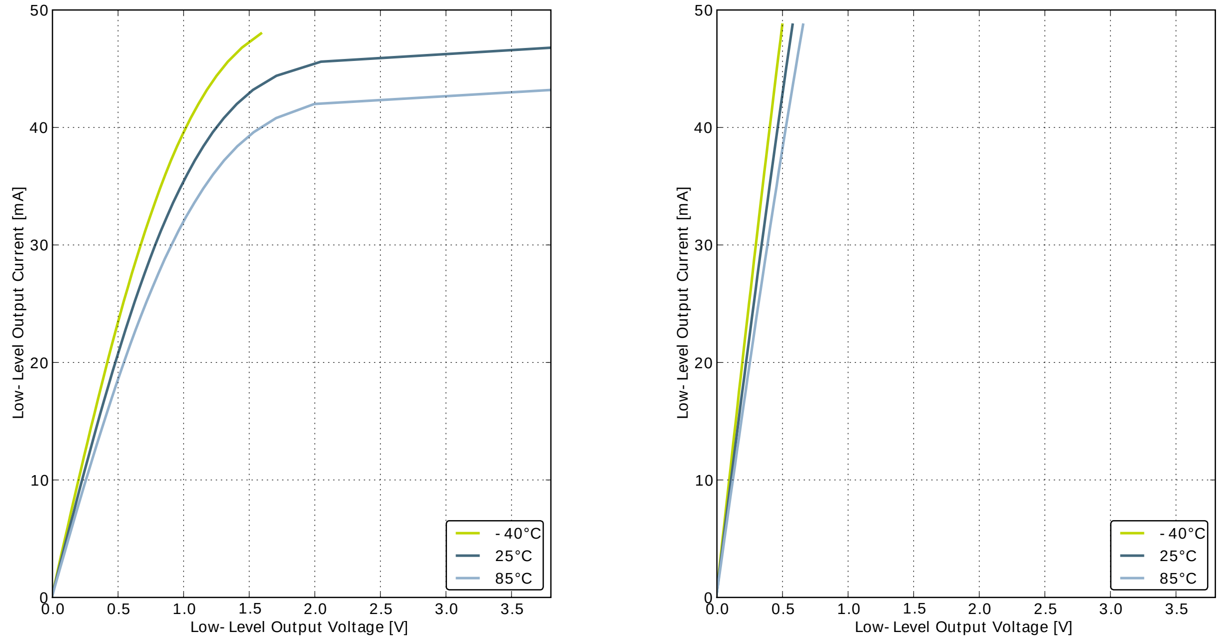
GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.8. Typical Low-Level Output Current, 3.8V Supply Voltage



GPIO_Px_CTRL DRIVEMODE = LOWEST

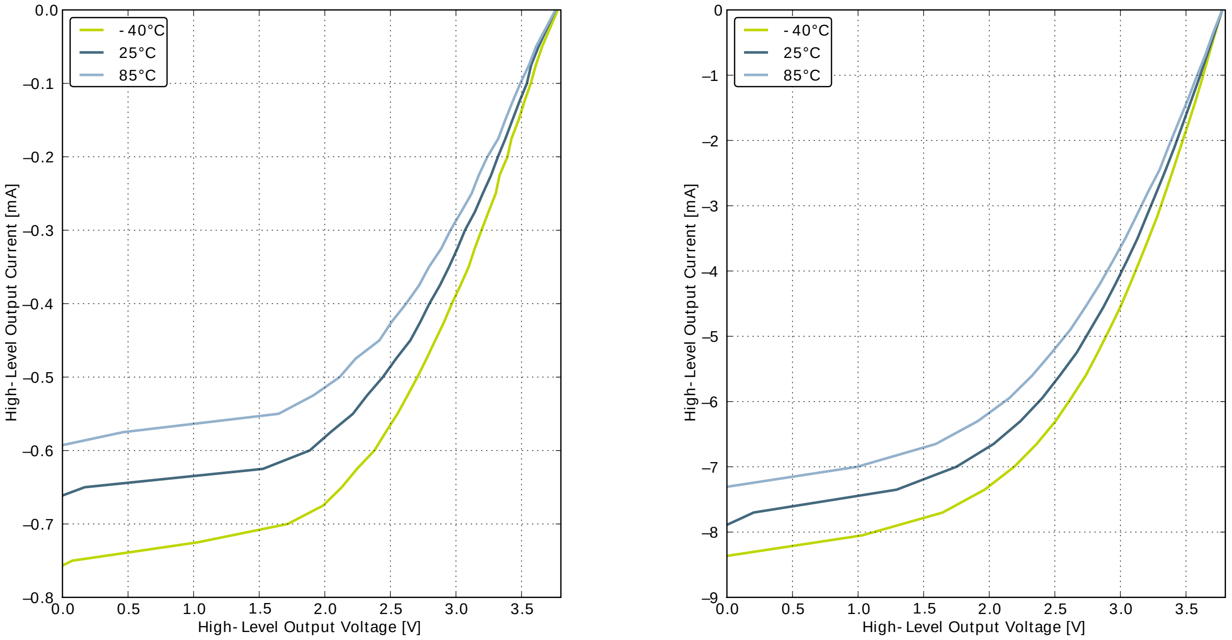
GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

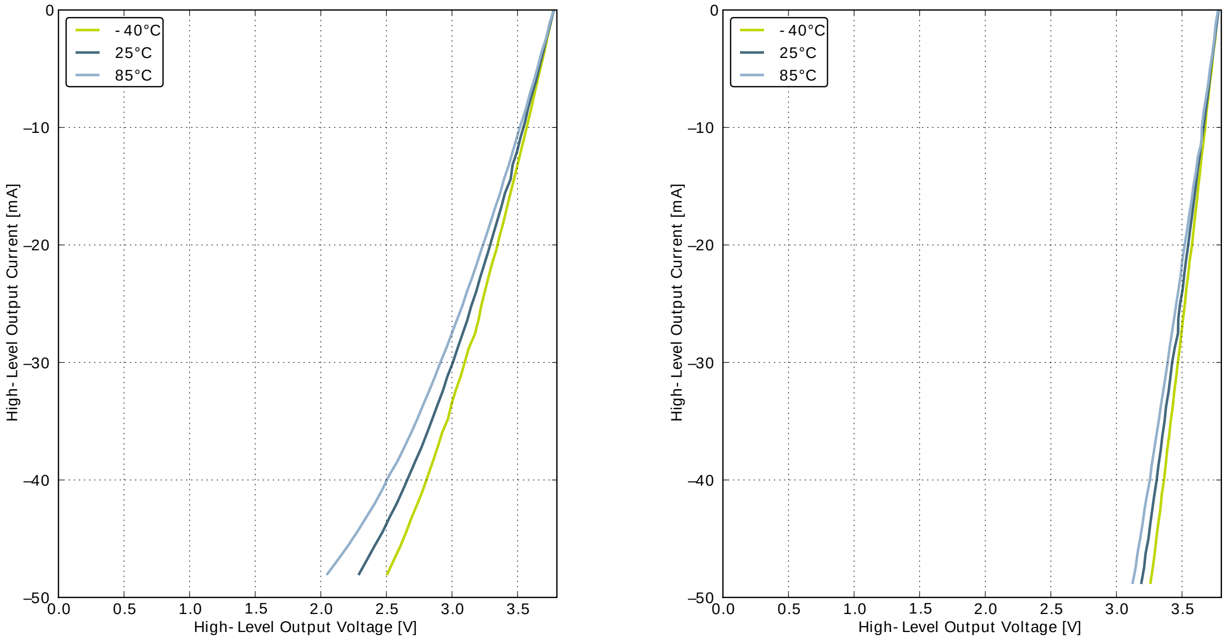
GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.9. Typical High-Level Output Current, 3.8V Supply Voltage



GPIO_Px_CTRL DRIVEMODE = LOWEST

GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

GPIO_Px_CTRL DRIVEMODE = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.8. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		X[1]		25	pF
DC_{LFXO}	Duty cycle		48	50	53.5	%
I_{LFXO}	Current consumption for core and buffer after startup.	ESR=30 kOhm, C_L=10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

[1] See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup in energyAware Designer in Simplicity Studio

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

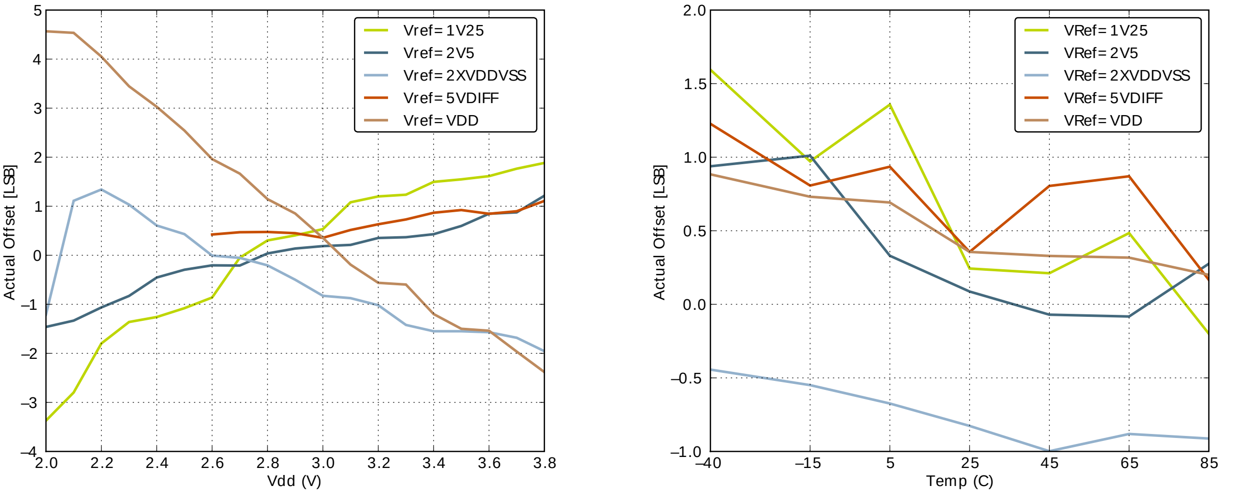
3.9.2 HFXO

Table 3.9. HFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Supported nominal crystal Frequency		4		48	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 48 MHz			50	Ohm
		Crystal frequency 32 MHz		30	60	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		µA
		32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		µA
t_{HFXO}	Startup time	32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		400		µs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_{ADCIN}	Input capacitance			2		pF
R_{ADCIN}	Input ON resistance		1			MOhm
$R_{ADCFILT}$	Input RC filter resistance			10		kOhm
$C_{ADCFILT}$	Input RC filter/decoupling capacitance			250		fF
f_{ADCCLK}	ADC Clock Frequency				13	MHz
$t_{ADCCONV}$	Conversion time	6 bit	7			ADC-CLK Cycles
		8 bit	11			ADC-CLK Cycles
		12 bit	13			ADC-CLK Cycles
t_{ADCACQ}	Acquisition time	Programmable	1		256	ADC-CLK Cycles
$t_{ADCACQVDD3}$	Required acquisition time for VDD/3 reference		2			µs
$t_{ADCSTART}$	Startup time of reference generator and ADC core in NORMAL mode			5		µs
	Startup time of reference generator and ADC core in KEEPADCWARM mode			1		µs
SNR_{ADC}	Signal to Noise Ratio (SNR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		59		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		65		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		65		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		67		dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		69		dB

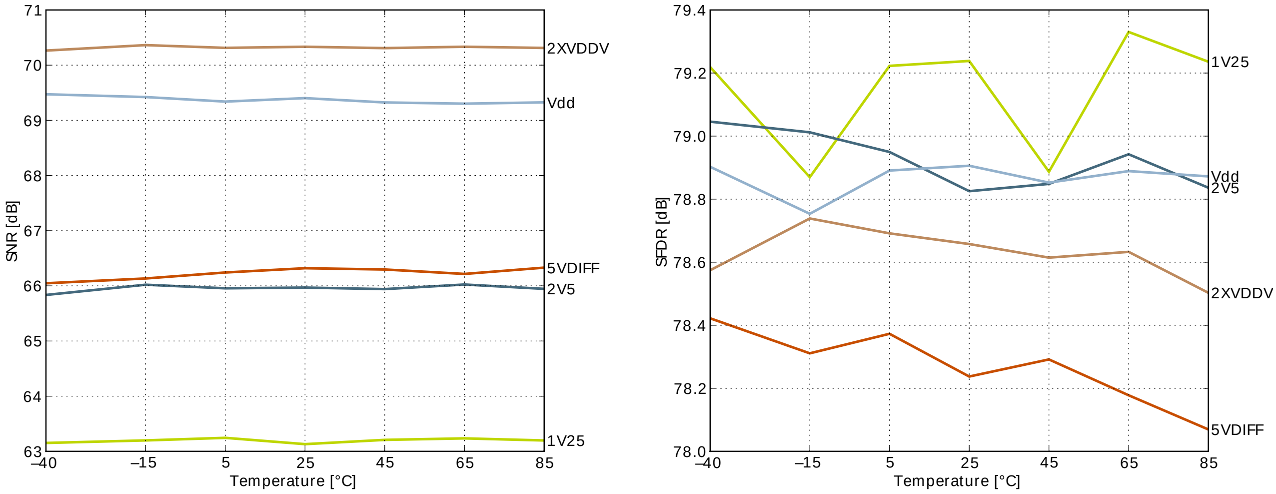
Figure 3.22. ADC Absolute Offset, Common Mode = Vdd /2



Offset vs Supply Voltage, Temp = 25°C

Offset vs Temperature, Vdd = 3V

Figure 3.23. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V



Signal to Noise Ratio (SNR)

Spurious-Free Dynamic Range (SFDR)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, Unity Gain		13	17	µA
G_{OL}	Open Loop Gain	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		101		dB
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		98		dB
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		91		dB
GBW_{OPAMP}	Gain Bandwidth Product	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		6.1		MHz
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		1.8		MHz
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		0.25		MHz
PM_{OPAMP}	Phase Margin	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, C_L=75 pF		64		°
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, C_L=75 pF		58		°
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, C_L=75 pF		58		°
R_{INPUT}	Input Resistance			100		Mohm
R_{LOAD}	Load Resistance		200			Ohm
I_{LOAD_DC}	DC Load Current				11	mA
V_{INPUT}	Input Voltage	OPAxHCMDIS=0	V_{SS}		V_{DD}	V
		OPAxHCMDIS=1	V_{SS}		V_{DD}-1.2	V
V_{OUTPUT}	Output Voltage		V_{SS}		V_{DD}	V
V_{OFFSET}	Input Offset Voltage	Unity Gain, V_{SS}<V_{in}<V_{DD}, OPAxHCMDIS=0	-13	0	11	mV
		Unity Gain, V_{SS}<V_{in}<V_{DD}-1.2, OPAxHCMDIS=1		1		mV
V_{OFFSET_DRIFT}	Input Offset Voltage Drift				0.02	mV/°C
SR_{OPAMP}	Slew Rate	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		3.2		V/µs
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		0.8		V/µs
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		0.1		V/µs
N_{OPAMP}	Voltage Noise	V_{out}=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx-HCMDIS=0		101		μV_{RMS}
		V_{out}=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx-HCMDIS=1		141		μV_{RMS}

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		V_{out}=1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAxHCMDIS=0		196		µV_{RMS}
		V_{out}=1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAxHCMDIS=1		229		µV_{RMS}
		RESSEL=7, 0.1 Hz<f<10 kHz, OPAxHCMDIS=0		1230		µV_{RMS}
		RESSEL=7, 0.1 Hz<f<10 kHz, OPAxHCMDIS=1		2130		µV_{RMS}
		RESSEL=7, 0.1 Hz<f<1 MHz, OPAxHCMDIS=0		1630		µV_{RMS}
		RESSEL=7, 0.1 Hz<f<1 MHz, OPAxHCMDIS=1		2590		µV_{RMS}

Figure 3.25. OPAMP Common Mode Rejection Ratio

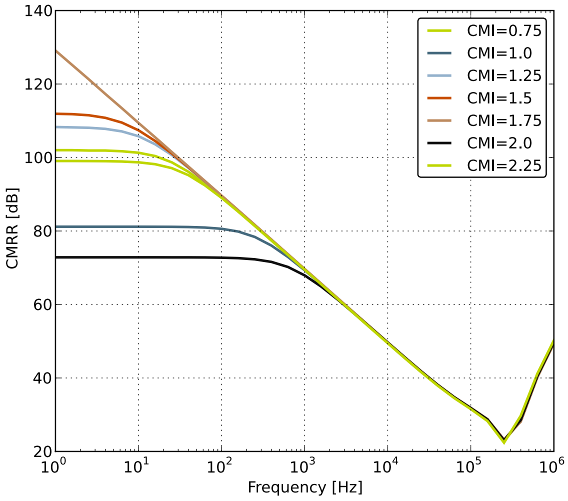


Figure 3.26. OPAMP Positive Power Supply Rejection Ratio

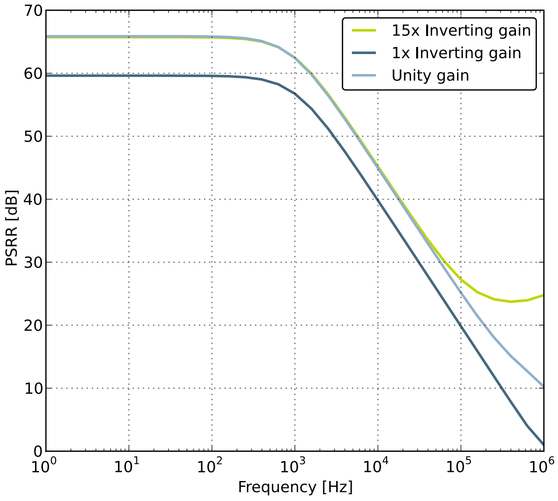


Table 3.19. EBI Write Enable Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{OH_WEn} [1] [2] [3] [4]	Output hold time, from trailing EBI_WEn/ EBI_NANDWEn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid	-6.00 + (WRHOLD * $t_{HFCORECLK}$)			ns
t_{OSU_WEn} [1] [2] [3] [4] [5]	Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_WEn/ EBI_NANDWEn edge	-14.00 + (WRSETUP * $t_{HFCORECLK}$)			ns
t_{WIDTH_WEn} [1] [2] [3] [4] [5]	EBI_WEn/EBI_NANDWEn pulse width	-7.00 + ((WRSTRB +1) * $t_{HFCORECLK}$)			ns

[1] Applies for all addressing modes (figure only shows D16 addressing mode)

[2] Applies for both EBI_WEn and EBI_NANWEn (figure only shows EBI_WEn)

[3] Applies for all polarities (figure only shows active low signals)

[4] Measurement done at 10% and 90% of V_{DD} (figure shows 50% of $_{VDD}$)

[5] The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFWE=0. The leading edge of EBI_WEn can be moved to the right by setting HALFWE=1. This decreases the length of t_{WIDTH_WEn} and increases the length of t_{OSU_WEn} by 1/2 * $t_{HFCLKNODIV}$.

Figure 3.32. EBI Address Latch Enable Related Output Timing

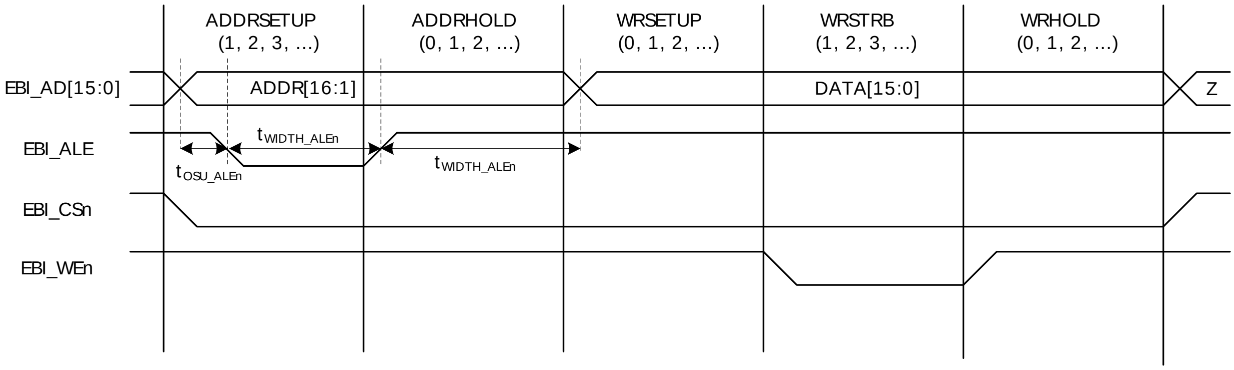


Table 3.20. EBI Address Latch Enable Related Output Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{OH_ALEn} [1] [2] [3] [4]	Output hold time, from trailing EBI_ALE edge to EBI_AD invalid	-6.00 + (ADDRHOLD[5] * $t_{HFCORECLK}$)			ns
t_{OSU_ALEn} [1] [2] [4]	Output setup time, from EBI_AD valid to leading EBI_ALE edge	-13.00 + (0 * $t_{HFCORECLK}$)			ns
t_{WIDTH_ALEn} [1] [2] [3] [4]	EBI_ALEn pulse width	-7.00 + (ADDRSETUP+1) * $t_{HFCORECLK}$)			ns

[1] Applies to addressing modes D8A24ALE and D16A16ALE (figure only shows D16A16ALE)

[2] Applies for all polarities (figure only shows active low signals)

[3] The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFALE=0. The trailing edge of EBI_ALE can be moved to the left by setting HALFALE=1. This decreases the length of t_{WIDTH_ALEn} and increases the length of tOH_ALEn by $t_{HFCORECLK}$ - 1/2 * $t_{HFCLKNODIV}$.

[4] Measurement done at 10% and 90% of V_{DD} (figure shows 50% of $_{VDD}$)

[5] Figure only shows a write operation. For a multiplexed read operation the address hold time is controlled via the RDSETUP state instead of via the ADDRHOLD state.

Figure 3.33. EBI Read Enable Related Output Timing

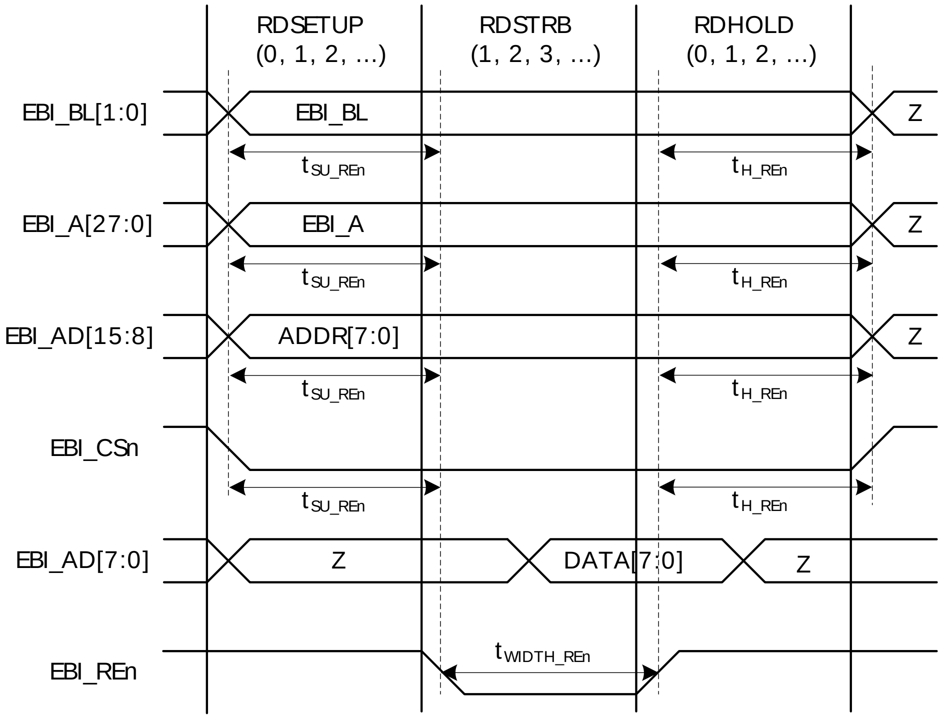


Table 3.21. EBI Read Enable Related Output Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{OH_REn} [1,2,3,4]	Output hold time, from trailing EBI_REn/ EBI_NANDREn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid	-10.00 + (RDHOLD * $t_{HFCORECLK}$)			ns
t_{OSU_REn} [1,2,3,4,5]	Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_REn/EBI_NANDREn edge	-10.00 + (RDSETUP * $t_{HFCORECLK}$)			ns
t_{WIDTH_REn} [1,2,3,4,5,6]	EBI_REn pulse width	-9.00 + ((RDSTRB+1) * $t_{HFCORECLK}$)			ns

[1] Applies for all addressing modes (figure only shows D8A8. Output timing for EBI_AD only applies to multiplexed addressing modes D8A24ALE and D16A16ALE)

[2] Applies for both EBI_REn and EBI_NANDREn (figure only shows EBI_REn)

[3] Applies for all polarities (figure only shows active low signals)

[4] Measurement done at 10% and 90% of V_{DD} (figure shows 50% of $_{VDD}$)

[5] The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFRE=0. The leading edge of EBI_REn can be moved to the right by setting HALFRE=1. This decreases the length of t_{WIDTH_REn} and increases the length of t_{OSU_REn} by 1/2 * $t_{HFCLKNODIV}$.

[6] When page mode is used, RDSTRB is replaced by RDPA for page hits.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{PCNT}	PCNT current	PCNT idle current, clock enabled		54		nA
I_{RTC}	RTC current	RTC idle current, clock enabled		54		nA
I_{LCD}	LCD current	LCD idle current, clock enabled		68		nA
I_{AES}	AES current	AES idle current, clock enabled		3.2		µA/MHz
I_{GPIO}	GPIO current	GPIO idle current, clock enabled		3.7		µA/MHz
I_{EBI}	EBI current	EBI idle current, clock enabled		11.8		µA/MHz
I_{PRS}	PRS current	PRS idle current		3.5		µA/MHz
I_{DMA}	DMA current	Clock enable		11.0		µA/MHz

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
						ETM_TD1 #3
D2	PA2	LCD_SEG15	EBI_AD11 #0/1/2	TIM0_CC2 #0/1		CMU_CLK0 #0 ETM_TD0 #3
D3	PB15					ETM_TD2 #1
D4	VSS	Ground.				
D5	IOVDD_6	Digital IO power supply 6.				
D6	PD9	LCD_SEG28	EBI_CS0 #0/1/2			
D7	IOVDD_5	Digital IO power supply 5.				
D8	PF1			TIM0_CC1 #5 LETIM0_OUT1 #2	US1_CS #2 I2C0_SCL #5 LEU0_RX #3	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
D9	PE7	LCD_COM3	EBI_A14 #0/1/2		US0_TX #1	
D10	PC8	ACMP1_CH0	EBI_A15 #0/1/2	TIM2_CC0 #2	US0_CS #2	LES_CH8 #0
D11	PC9	ACMP1_CH1	EBI_A09 #1/2	TIM2_CC1 #2	US0_CLK #2	LES_CH9 #0 GPIO_EM4WU2
E1	PA6	LCD_SEG19	EBI_AD15 #0/1/2		LEU1_RX #1	ETM_TCLK #3 GPIO_EM4WU1
E2	PA5	LCD_SEG18	EBI_AD14 #0/1/2	TIM0_CDTI2 #0	LEU1_TX #1	LES_ALTEX4 #0 ETM_TD3 #3
E3	PA4	LCD_SEG17	EBI_AD13 #0/1/2	TIM0_CDTI1 #0	U0_RX #2	LES_ALTEX3 #0 ETM_TD2 #3
E4	PB0	LCD_SEG32	EBI_A16 #0/1/2	TIM1_CC0 #2		
E8	PF0			TIM0_CC0 #5 LETIM0_OUT0 #2	US1_CLK #2 I2C0_SDA #5 LEU0_TX #3	DBG_SWCLK #0/1/2/3
E9	PE0		EBI_A07 #0/1/2	TIM3_CC0 #1 PCNT0_S0IN #1	U0_TX #1 I2C1_SDA #2	
E10	PE1		EBI_A08 #0/1/2	TIM3_CC1 #1 PCNT0_S1IN #1	U0_RX #1 I2C1_SCL #2	
E11	PE3	BU_STAT	EBI_A10 #0		U1_RX #3	ACMP1_O #1
F1	PB1	LCD_SEG33	EBI_A17 #0/1/2	TIM1_CC1 #2		
F2	PB2	LCD_SEG34	EBI_A18 #0/1/2	TIM1_CC2 #2		
F3	PB3	LCD_SEG20/ LCD_COM4	EBI_A19 #0/1/2	PCNT1_S0IN #1	US2_TX #1	
F4	PB4	LCD_SEG21/ LCD_COM5	EBI_A20 #0/1/2	PCNT1_S1IN #1	US2_RX #1	
F8	VDD_DREG	Power supply for on-chip voltage regulator.				
F9	VSS_DREG	Ground for on-chip voltage regulator.				
F10	PE2	BU_VOUT	EBI_A09 #0	TIM3_CC2 #1	U1_TX #3	ACMP0_O #1
F11	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.				
G1	PB5	LCD_SEG22/ LCD_COM6	EBI_A21 #0/1/2		US2_CLK #1	
G2	PB6	LCD_SEG23/ LCD_COM7	EBI_A22 #0/1/2		US2_CS #1	
G3	VSS	Ground.				
G4	IOVDD_0	Digital IO power supply 0.				
G8	IOVDD_4	Digital IO power supply 4.				

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ETM_TD1	PD3	PD13	PD3	PA3				Embedded Trace Module ETM data 1.
ETM_TD2	PD4	PB15	PD4	PA4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5	PF3	PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12	PE1					I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11	PE0					I2C1 Serial Data input / output.
LCD_BCAP_N	PA13							LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12							LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14							LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4							LCD driver common line number 0.
LCD_COM1	PE5							LCD driver common line number 1.
LCD_COM2	PE6							LCD driver common line number 2.
LCD_COM3	PE7							LCD driver common line number 3.
LCD_SEG0	PF2							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG1	PF3							LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG2	PF4							LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5							LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG4	PE8							LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG5	PE9							LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG6	PE10							LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG7	PE11							LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG8	PE12							LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2.

7 Revision History

7.1 Revision 1.40

March 21st, 2016

Added clarification on conditions for INL_{ADC} and DNL_{ADC} parameters.

Reduced maximum and typical current consumption for all EM0 entries except 48 MHz in the Current Consumption table in the Electrical Characteristics section.

Increased maximum specifications for EM2 current, EM3 current, and EM4 current in the Current Consumption table in the Electrical Characteristics section.

Increased typical specification for EM2 and EM3 current at 85 C in the Current Consumption table in the Electrical Characteristics section.

Added EM2, EM3, and EM4 current consumption vs. temperature graphs.

Added a new EM2 entry and specified the existing specification is for EM0 for the BOD threshold on falling external supply voltage in the Power Management table in the Electrical Characteristics section.

Reduced maximum input leakage current in the GPIO table in the Electrical Characteristics section.

Added a maximum current consumption specification to the LFRCO table in the Electrical Characteristics section.

Added maximum specifications for the active current including references for two channels to the DAC table in the Electrical Characteristics section.

Increased the maximum specification for DAC offset voltage in the DAC table in the Electrical Characteristics section.

Increased the typical specifications for active current with FULLBIAS=1 and capacitive sense internal resistance in the ACMP table in the Electrical Characteristics section.

Added minimum and maximum specifications and updated the typical value for the VCMP offset voltage in the VCMP table in the Electrical Characteristics section.

Removed the maximum specification and reduced the typical value for hysteresis in the VCMP table in the Electrical Characteristics section.

Updated all graphs in the Electrical Characteristics section to display data for 2.0 V as the minimum voltage.

7.2 Revision 1.30

May 23rd, 2014

Removed "preliminary" markings

Updated HFRCO figures.

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Updated Current Consumption information.

Updated Power Management information.

Updated GPIO information.

Updated LFRCO information.

Updated HFRCO information.

Updated ULFRCO information.

Updated ADC information.

Updated DAC information.

Updated OPAMP information.

Updated ACMP information.

Updated VCMP information.

Added AUXHFRCO information.

7.3 Revision 1.21

November 21st, 2013

Updated figures.

Updated errata-link.

Updated chip marking.

Added link to Environmental and Quality information.

Re-added missing DAC-data.

7.4 Revision 1.20

September 30th, 2013

Added I2C characterization data.

Added SPI characterization data.

Added EBI characterization data.

Corrected the DAC and OPAMP2 pin sharing information in the Alternate Functionality Pinout section.

Corrected GPIO operating voltage from 1.8 V to 1.85 V.

Updated that the EM2 current consumption test was carried out with only one RAM block enabled.

Corrected the ADC resolution from 12, 10 and 6 bit to 12, 8 and 6 bit.

Updated Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

7.5 Revision 1.10

June 28th, 2013

7.10 Revision 0.91

March 21th, 2011

Added new alternative locations for EBI and SWO.

Corrected slew rate data for Opamps.

7.11 Revision 0.90

February 4th, 2011

Initial preliminary release.

B Contact Information

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701

Please visit the Silicon Labs Technical Support web page:
http://www.silabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.

List of Figures