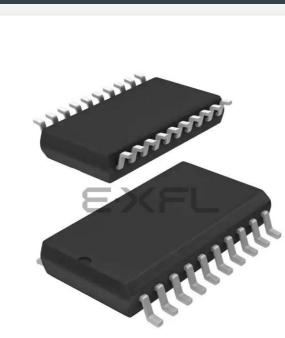
Microchip Technology - ATTINY2313V-10SU Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	10MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	2KB (1K x 16)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/attiny2313v-10su

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Features

- Utilizes the AVR[®] RISC Architecture
- AVR High-performance and Low-power RISC Architecture
 - 120 Powerful Instructions Most Single Clock Cycle Execution
 - 32 x 8 General Purpose Working Registers
 - Fully Static Operation
- Up to 20 MIPS Throughput at 20 MHz
- Data and Non-volatile Program and Data Memories
 - 2K Bytes of In-System Self Programmable Flash Endurance 10,000 Write/Erase Cycles
 - 128 Bytes In-System Programmable EEPROM Endurance: 100,000 Write/Erase Cycles
 - 128 Bytes Internal SRAM
 - Programming Lock for Flash Program and EEPROM Data Security
- Peripheral Features
 - One 8-bit Timer/Counter with Separate Prescaler and Compare Mode
 - One 16-bit Timer/Counter with Separate Prescaler, Compare and Capture Modes
 - Four PWM Channels
 - On-chip Analog Comparator
 - Programmable Watchdog Timer with On-chip Oscillator
 - USI Universal Serial Interface
 - Full Duplex USART
- Special Microcontroller Features
 - debugWIRE On-chip Debugging
 - In-System Programmable via SPI Port
 - External and Internal Interrupt Sources
 - Low-power Idle, Power-down, and Standby Modes
 - Enhanced Power-on Reset Circuit
 - Programmable Brown-out Detection Circuit
 - Internal Calibrated Oscillator
- I/O and Packages
 - 18 Programmable I/O Lines
 - 20-pin PDIP, 20-pin SOIC, 20-pad QFN/MLF
- Operating Voltages
 - 1.8 5.5V (ATtiny2313V)
 - 2.7 5.5V (ATtiny2313)
- Speed Grades
 - ATtiny2313V: 0 4 MHz @ 1.8 5.5V, 0 10 MHz @ 2.7 5.5V
 - ATtiny2313: 0 10 MHz @ 2.7 5.5V, 0 20 MHz @ 4.5 5.5V
- Typical Power Consumption
 - Active Mode
 - 1 MHz, 1.8V: 230 μA
 - 32 kHz, 1.8V: 20 µA (including oscillator)
 - Power-down Mode
 - < 0.1 µA at 1.8V



8-bit **AVR**[®] Microcontroller with 2K Bytes In-System Programmable Flash

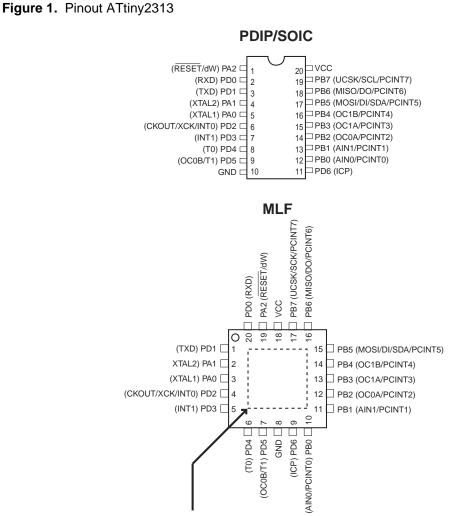
ATtiny2313/V

Summary









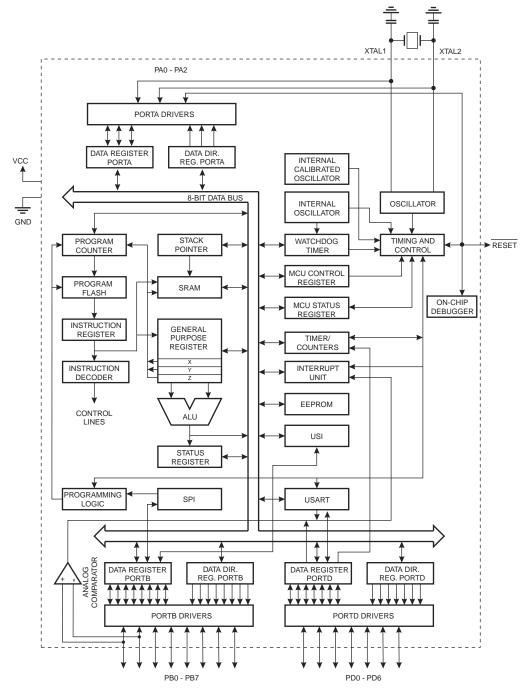
NOTE: Bottom pad should be soldered to ground.

Overview The ATtiny2313 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny2313 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

² ATtiny2313

Block Diagram









The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATtiny2313 provides the following features: 2K bytes of In-System Programmable Flash, 128 bytes EEPROM, 128 bytes SRAM, 18 general purpose I/O lines, 32 general purpose working registers, a single-wire Interface for On-chip Debugging, two flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, Universal Serial Interface with Start Condition Detector, a programmable Watchdog Timer with internal Oscillator, and three software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, or by a conventional non-volatile memory programmer. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATtiny2313 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATtiny2313 AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

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Pin Descriptions

VCC	Digital supply voltage.

GND Ground.

Port A (PA2..PA0) Port A is a 3-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the ATtiny2313 as listed on page 53.

Port B (PB7..PB0) Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATtiny2313 as listed on page 53.

Port D (PD6..PD0) Port D is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATtiny2313 as listed on page 56.

- **RESET** Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 34. Shorter pulses are not guaranteed to generate a reset. The Reset Input is an alternate function for PA2 and dW.
- **XTAL1** Input to the inverting Oscillator amplifier and input to the internal clock operating circuit. XTAL1 is an alternate function for PA0.
- **XTAL2** Output from the inverting Oscillator amplifier. XTAL2 is an alternate function for PA1.





General Information	
Resources	A comprehensive set of development tools, application notes and datasheets are available for download at http://www.atmel.com/avr.
Code Examples	This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.
Data Retention	Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

Register Summary

DATE SHEG 1 T H S V H Z C I 0x00 0x00 SPL SPL <t< th=""><th>Address</th><th>Name</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th><th>Page</th></t<>	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
Instrum <					Н			N			
0.62C (06.5) 0.CR86 PF Thm Thm Control P			-	-		-			_		
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	11
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Order (ess) TMSK TOTEL OCEFA COCEA FILE OCEGA TYR TOTU OCEAA TR 0x8 (6x6) SPUCSR - - CTPR SR LPR ROT SILPR ROT SILPR ROT TT TO SILPR ROT SILPR ROT SILPR ROT SILPR ROT TT TO SILPR ROT SILPR ROT SILPR ROT SILPR ROT SILPR ROT TT TO SILPR ROT	0x3B (0x5B)	GIMSK	INT1	INT0	PCIE	-	-	-	-	-	60
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0.47 (0.57) SPMCSR CTP3 PC/MT											
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Ords (0.55) MCU2R PUD SM1 SE SM0 SC11 ISC10 ISC11 ISC10 <thisc11< th=""> <thisc11< th=""> <thisc11<< td=""><td></td><td></td><td>-</td><td>_</td><td></td><td></td><td></td><td></td><td>PGERS</td><td>SELFPRGEN</td><td></td></thisc11<<></thisc11<></thisc11<>			-	_					PGERS	SELFPRGEN	
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0x00000000000000000000000000000000000	0x32 (0x52)	TCNT0				Timer/Co	unter0 (8-bit)		•	•	77
Out COM1A COM1A0 COM1B0 Image Image <th< td=""><td>0x31 (0x51)</td><td>OSCCAL</td><td>-</td><td>CAL6</td><td>CAL5</td><td>CAL4</td><td>CAL3</td><td>CAL2</td><td>CAL1</td><td>CAL0</td><td>26</td></th<>	0x31 (0x51)	OSCCAL	-	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	26
Date Date Description CS10 CS10 D07 DateD (node) TGKTH TemerCounter1 - Counter Register Not Byte 108 DateD (node) TGKTH TemerCounter1 - Counter Register Not Byte 108 DateD (node) OCR1AH TemerCounter1 - Compare Register AL one Byte 108 DateD (node) OCR1AH TimerCounter1 - Compare Register AL one Byte 109 DateD (node) OCR1AH TimerCounter1 - Compare Register BLone Byte 109 DateD (node) OCR1AH TimerCounter1 - Compare Register Hole Byte 109 DateD (node) OLCR - - - - DateD (node) OLCR - - - - - DateD (node) OLCR - - - - - 109 DateD (node) OLCR FOC1A FOC1B - - - - 108 DateD (node) VODE VODE VODE VODE VODE VODE VODP 42 Dat	0x30 (0x50)	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	-	-	WGM01	WGM00	73
0x02 (msd) TXNTH ImmeCounter1 - Compare Register Mp Byte 108 0x26 (msd) OCR1MH TimerCounter1 - Compare Register A Hot Byte 108 0x26 (msd) OCR1MH TimerCounter1 - Compare Register A Hot Byte 108 0x26 (msd) OCR1MH TimerCounter1 - Compare Register A Hot Byte 109 0x26 (msd) OCR1ML TimerCounter1 - Compare Register B High Byte 109 0x26 (msd) OCR1ML TimerCounter1 - Compare Register Low Byte 109 0x26 (msd) OCR1ML TimerCounter1 - Compare Register Low Byte 109 0x26 (msd) ICR1M TimerCounter1 - Input Cepture Register Low Byte 100 0x26 (msd) ICR1M TimerCounter1 - Input Cepture Register Low Byte 100 0x26 (msd) ICR1M TimerCounter1 - Input Cepture Register Low Byte 100 0x26 (msd) ICR1M TimerCounter1 - Input Cepture Register Low Byte 100 0x26 (msd) ICR1M FOC18 - - - - - - - - - - - - - -	0x2F (0x4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1BO	-	-	WGM11	WGM10	104
0x2C (0xC) TONTL Timer/Counter1 - Compare Register Alue byte 108 0x2B (0xB) OCR1AH Timer/Counter1 - Compare Register Alue byte 109 0x2B (0xB) OCR1BH Timer/Counter1 - Compare Register Blue byte 109 0x2B (0xB) OCR1BH Timer/Counter1 - Compare Register Blue byte 109 0xB (0xB) OCR1BH Timer/Counter1 - Input Counter1 - Register Blue byte 109 0xB (0xB) CLKPR CLKPCE - - - - - - - 109 0xB (0xB) ICIKR CLKPCE - - - - - 109 100	. ,		ICNC1	ICES1					CS11	CS10	
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0x23 (0x43) GTCCR - - - - - - PSR10 81 0x22 (0x42) TCCR1C FOC1A FOC1B - - - - - - - - - - - 108 0x21 (0x44) WDTCS WDF WDF WDF WDF WDF WDF 42 0x0 0x1 0x41 WDF PCINT3 PCINT3 PCINT4					Timer/	Counter1 - Input (Capture Register	High Byte			109
0x22 (ox42) TCCR1C FOC1A FOC1B 108 0x21 (0x41) WDTCSR WDIF WDIF WD2 WD2 WD2 WDP1 WDP0 422 0x20 (0x40) PCMRKS PCINTS PCITS PCINTS <td< td=""><td>0x24 (0x44)</td><td>ICR1L</td><td></td><td></td><td>Timer/</td><td>Counter1 - Input</td><td>Capture Register</td><td>Low Byte</td><td></td><td></td><td>109</td></td<>	0x24 (0x44)	ICR1L			Timer/	Counter1 - Input	Capture Register	Low Byte			109
Op/10x40 PD/FS WD/F WD/F WD/F PD/F2 WD/F2 WD/F2 WD/F1 WD/F0 42 0x20 (0x40) PCMSK PCINT7 PCINT6 PCINT5 PCINT3 PCINT3 PCINT1 PCINT0 61 0x1F (0x3F) EEAR - PORTA - - - - PORTA PORTA - - - - PORTA PORTB </td <td>0x23 (0x43)</td> <td>GTCCR</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>PSR10</td> <td>81</td>	0x23 (0x43)	GTCCR	-	-	-	-	-	-	-	PSR10	81
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0x05 (0x25) Reserved -											
0x04 (0x24) Reserved - 0	, ,			1							
0x03 (0x23) UCSRC - UMSEL UPM1 UPM0 USBS UCSZ1 UCSZ0 UCPOL 132 0x02 (0x22) UBRH - - - - UBRRH - 133 0x01 (0x21) DIDR - - - - AIN1D AIN0D 150						1	1			1	
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0x01 (0x21) DIDR AIN1D AIN0D 150	. ,									· · · ·	
0x00 (0x20) Reserved	0x01 (0x21)	DIDR	-	-	-	-	-	-	AIN1D	AIN0D	150
	0x00 (0x20)	Reserved	-	-	-	-	-	-	-	-	





- Note: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 - 2. I/O Registers within the address range 0x00 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
 - Some of the status flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such status flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
 - 4. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses.

ATtiny2313

Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND L	OGIC INSTRUCTION	S		•	•
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \gets Rd \bullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \lor K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow 0xFF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← 0x00 – Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \lor K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (0xFF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	Rd ← 0xFF	None	1
BRANCH INSTRUC			1		
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP	ĸ	Indirect Jump to (Z)	PC ← Z	None	2
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL	ĸ	Indirect Call to (Z)	$PC \leftarrow Z$	None	3
RET		Subroutine Return	$PC \leftarrow STACK$	None	4
RETI		Interrupt Return	PC ← STACK	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if $(Rd = Rr) PC \leftarrow PC + 2 \text{ or } 3$	None	1/2/3
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Rd,K		Rd – K		1
SBRC		Compare Register with Immediate		Z, N,V,C,H	1/2/3
	Rr, b	Skip if Bit in Register Cleared	if $(\operatorname{Rr}(b)=0)$ PC \leftarrow PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if $(\text{Rr}(b)=1) \text{PC} \leftarrow \text{PC} + 2 \text{ or } 3$	None	
SBIC	P, b	Skip if Bit in I/O Register Cleared	if $(P(b)=0) PC \leftarrow PC + 2 \text{ or } 3$	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if $(P(b)=1) PC \leftarrow PC + 2 \text{ or } 3$	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC \leftarrow PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC \leftarrow PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC \leftarrow PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC \leftarrow PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC \leftarrow PC + k + 1	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC \leftarrow PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC \leftarrow PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N \oplus V= 0) then PC \leftarrow PC + k + 1	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N \oplus V= 1) then PC \leftarrow PC + k + 1	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC \leftarrow PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC \leftarrow PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC \leftarrow PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC \leftarrow PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC \leftarrow PC + k + 1	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC \leftarrow PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC \leftarrow PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC \leftarrow PC + k + 1	None	1/2
BIT AND BIT-TEST	INSTRUCTIONS				
	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
SBI				T	
SBI CBI	P,b	Clear Bit in I/O Register	$I/O(P,b) \leftarrow 0$	None	2
	P,b Rd	Clear Bit in I/O Register Logical Shift Left	$I/O(P,b) \leftarrow 0$ Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0	None Z,C,N,V	2
СВІ					





Mnemonics	Operands	Description	Operation	Flags	#Clocks
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=06	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(30)←Rd(74),Rd(74)←Rd(30)	None	1
BSET	s	Flag Set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	Т	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	C ← 1	С	1
CLC		Clear Carry	$C \leftarrow 0$	С	1
SEN		Set Negative Flag	N ← 1	Ν	1
CLN		Clear Negative Flag	N ← 0	Ν	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	l ← 1	1	1
CLI		Global Interrupt Disable	l ← 0	1	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	V ← 1	V	1
CLV		Clear Twos Complement Overflow	$V \leftarrow 0$	V	1
SET		Set T in SREG	T ← 1	Т	1
CLT		Clear T in SREG	T ← 0	Т	1
SEH		Set Half Carry Flag in SREG	H ← 1	Н	1
CLH	1	Clear Half Carry Flag in SREG	H ← 0	Н	1
DATA TRANSFER I	NSTRUCTIONS				·
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Word	$Rd+1:Rd \leftarrow Rr+1:Rr$	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	$Rd \leftarrow (X), X \leftarrow X + 1$	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	$X \leftarrow X - 1, Rd \leftarrow (X)$	None	2
LD	Rd, Y	Load Indirect	$Rd \leftarrow (Y)$	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	$Rd \leftarrow (Y), Y \leftarrow Y + 1$	None	2
LD	Rd, - Y	Load Indirect and Pre-Dec.	$Y \leftarrow Y - 1, Rd \leftarrow (Y)$	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	$Rd \leftarrow (Y + q)$	None	2
LD	Rd, Z	Load Indirect	$Rd \leftarrow (Z)$	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	$Rd \leftarrow (Z), Z \leftarrow Z+1$	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	$Z \leftarrow Z - 1, Rd \leftarrow (Z)$	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	2
LDS	Rd, k	Load Direct from SRAM	$Rd \leftarrow (k)$	None	2
ST	X, Rr	Store Indirect	$(X) \leftarrow Rr$	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	$(X) \leftarrow \operatorname{Rr}, X \leftarrow X + 1$	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	$X \leftarrow X - 1, (X) \leftarrow Rr$	None	2
ST	Y, Rr	Store Indirect	$(Y) \leftarrow Rr$	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	$(Y) \leftarrow Rr, Y \leftarrow Y + 1$	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	$Y \leftarrow Y - 1, (Y) \leftarrow Rr$	None	2
STD	Y+q,Rr	Store Indirect with Displacement	$(Y + q) \leftarrow Rr$	None	2
ST	Z, Rr	Store Indirect	$(Z) \leftarrow Rr$	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	$(Z) \leftarrow Rr, Z \leftarrow Z + 1$	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	$Z \leftarrow Z - 1, (Z) \leftarrow Rr$	None	2
STD	Z+q,Rr	Store Indirect and Pie-Dec.	$(Z+q) \leftarrow Rr$	None	2
STS	k, Rr	Store Direct to SRAM	$(2+q) \leftarrow Rr$ $(k) \leftarrow Rr$	None	2
LPM	N, NI	Load Program Memory	$(k) \leftarrow Kl$ $R0 \leftarrow (Z)$	None	3
LPM	Rd, Z	Load Program Memory	$RU \leftarrow (Z)$ $Rd \leftarrow (Z)$		3
LPM	Rd, Z+	Load Program Memory Load Program Memory and Post-Inc	$Rd \leftarrow (Z)$ $Rd \leftarrow (Z), Z \leftarrow Z+1$	None	3
SPM	κu, ∠+	Load Program Memory and Post-Inc Store Program Memory	$(Z) \leftarrow R1:R0$	None None	-
	Pd D				
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	$P \leftarrow Rr$	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	$Rd \leftarrow STACK$	None	2
MCU CONTROL INS	STRUCTIONS	No On continu		New	
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

ATtiny2313

Ordering Information

Speed (MHz) ⁽³⁾	Power Supply (V)	Ordering Code ⁽⁴⁾	Package ⁽²⁾	Operation Range
10	1.8 - 5.5	ATtiny2313V-10PU ATtiny2313V-10SU ATtiny2313V-10SUR ATtiny2313V-10MU ATtiny2313V-10MUR	20P3 20S 20S 20M1 20M1	Industrial (-40°C to +85°C) ⁽¹⁾
20	2.7 - 5.5	ATtiny2313-20PU ATtiny2313-20SU ATtiny2313-20SUR ATtiny2313-20MU ATtiny2313-20MUR	20P3 20S 20S 20M1 20M1	Industrial (-40°C to +85°C) ⁽¹⁾

Notes: 1. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging alternative, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

- 3. For Speed vs. V_{CC} see Figure 82 on page 180 and Figure 83 on page 180.
- 4. Code Indicators:

U: matte tin

- R: tape & reel

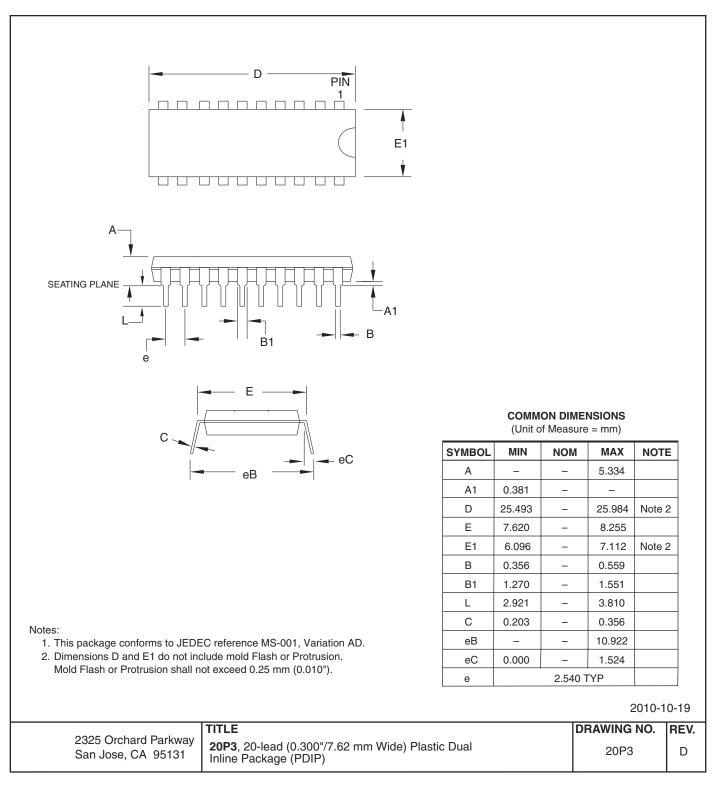
Package Type		
20P3	20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)	
20S	20-lead, 0.300" Wide, Plastic Gull Wing Small Outline Package (SOIC)	
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (MLF)	



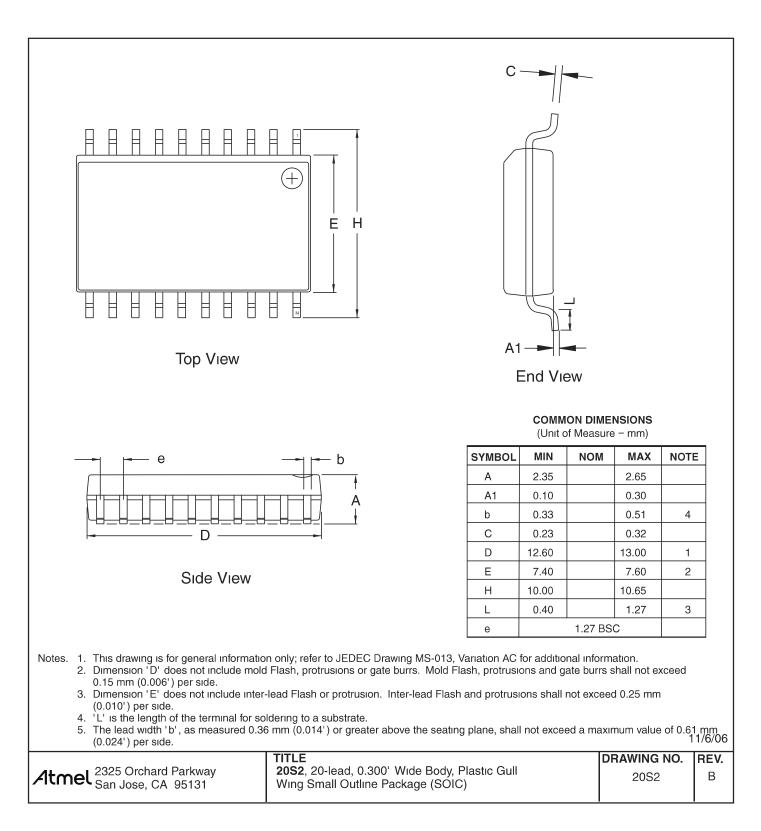


Packaging Information

20P3



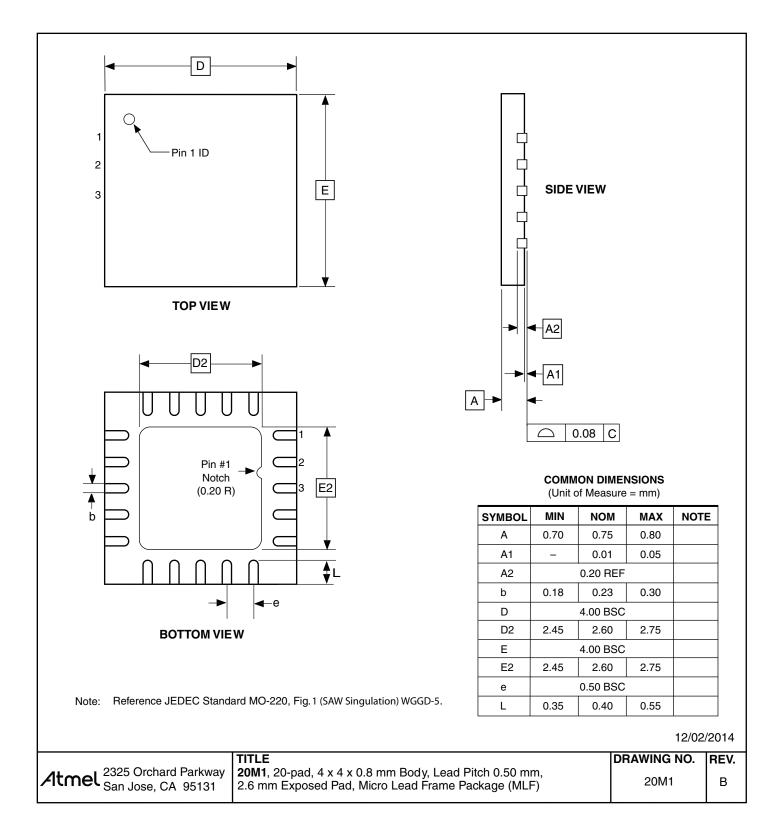
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20M1



Errata The revision in this section refers to the revision of the ATtiny2313 device.

ATtiny2313 Rev C No known errata

ATtiny2313 Rev B

- Wrong values read after Erase Only operation
- Parallel Programming does not work
- Watchdog Timer Interrupt disabled
- EEPROM can not be written below 1.9 volts

1. Wrong values read after Erase Only operation

At supply voltages below 2.7 V, an EEPROM location that is erased by the Erase Only operation may read as programmed (0x00).

Problem Fix/Workaround

If it is necessary to read an EEPROM location after Erase Only, use an Atomic Write operation with 0xFF as data in order to erase a location. In any case, the Write Only operation can be used as intended. Thus no special considerations are needed as long as the erased location is not read before it is programmed.

2. Parallel Programming does not work

Parallel Programming is not functioning correctly. Because of this, reprogramming of the device is impossible if one of the following modes are selected:

- In-System Programming disabled (SPIEN unprogrammed)
- Reset Disabled (RSTDISBL programmed)

Problem Fix/Workaround

Serial Programming is still working correctly. By avoiding the two modes above, the device can be reprogrammed serially.

3. Watchdog Timer Interrupt disabled

If the watchdog timer interrupt flag is not cleared before a new timeout occurs, the watchdog will be disabled, and the interrupt flag will automatically be cleared. This is only applicable in interrupt only mode. If the Watchdog is configured to reset the device in the watchdog timeout following an interrupt, the device works correctly.

Problem fix / Workaround

Make sure there is enough time to always service the first timeout event before a new watchdog timeout occurs. This is done by selecting a long enough time-out period.

4. EEPROM can not be written below 1.9 volts

Writing the EEPROM at V_{CC} below 1.9 volts might fail.

Problem fix / Workaround

Do not write the EEPROM when V_{CC} is below 1.9 volts.

ATtiny2313 Rev A Revision A has not been sampled.





Datasheet Revision History

Refer to the complete datasheet for revision history change log.





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2543MS-AVR-10/16





Headquarters

Atmel Corporation 2325 Orchard Parkway San Jose, CA 95131 USA Tel: 1(408) 441-0311 Fax: 1(408) 487-2600

International

Atmel Asia Unit 1-5 & 16, 19/F BEA Tower, Millennium City 5 418 Kwun Tong Road Kwun Tong, Kowloon Hong Kong Tel: (852) 2245-6100 Fax: (852) 2722-1369 Atmel Europe Le Krebs 8, Rue Jean-Pierre Timbaud BP 309 78054 Saint-Quentin-en-Yvelines Cedex France Tel: (33) 1-30-60-70-00 Fax: (33) 1-30-60-71-11

Atmel Japan

9F, Tonetsu Shinkawa Bldg. 1-24-8 Shinkawa Chuo-ku, Tokyo 104-0033 Japan Tel: (81) 3-3523-3551 Fax: (81) 3-3523-7581

Product Contact

Web Site www.atmel.com Technical Support avr@atmel.com Sales Contact www.atmel.com/contacts

Literature Requests www.atmel.com/literature

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