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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c712-04i-p

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2.2.2.6 PCON Register

The Power Control (PCON) register contains a flag bit to allow differentiation between a Power-on Reset (POR) to an external MCLR Reset or WDT Reset. These devices contain an additional bit to differentiate a Brown-out Reset condition from a Power-on Reset condition. Note: If the BODEN Configuration bit is set, BOR is '1' on Power-on Reset. If the BODEN Configuration bit is clear, BOR is unknown on Power-on Reset. The BOR Status bit is a "don't care" and is

not necessarily predictable if the brown-out circuit is disabled (the BODEN Configuration bit is clear). BOR must then be set by the user and checked on subsequent resets to see if it is clear, indicating a brown-out has occurred.

FIGURE 2-9: PCON REGISTER (ADDRESS 8Eh)



PORTB pins RB3:RB1 are multiplexed with several peripheral functions (Table 3-3). PORTB pins RB3:RB0 have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTB pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modifywrite instructions (BSF, BCF, XORWF) with TRISB as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

Four of PORTB's pins, RB7:RB4, have an interrupt-onchange feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupton-change comparison). The input pins, RB7:RB4, are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- a) Any read or write of PORTB will end the mismatch condition.
- b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.



FIGURE 3-4: BLOCK DIAGRAM OF RB1/T10S0/T1CKI PIN

6.0 TIMER2 MODULE

The Timer2 module timer has the following features:

- 8-bit timer (TMR2 register)
- 8-bit period register (PR2)
- Readable and writable (both registers)
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16)
- Interrupt on TMR2 match of PR2

Timer2 has a control register, shown in Figure 6-1. Timer2 can be shut off by clearing control bit TMR2ON (T2CON<2>) to minimize power consumption.

Figure 6-2 is a simplified block diagram of the Timer2 module.

Additional information on timer modules is available in the PIC[®] Mid-Range Reference Manual, (DS33023).

FIGURE 6-1: T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)



FIGURE 6-2: TIMER2 BLOCK DIAGRAM



7.2 Compare Mode

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the RB3/CCP1 pin is either:

- driven High
- driven Low
- remains Unchanged

The action on the pin is based on the value of control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). At the same time, interrupt flag bit CCP1IF is set.

FIGURE 7-4: COMPARE MODE OPERATION BLOCK DIAGRAM



7.2.1 CCP PIN CONFIGURATION

The user must configure the RB3/CCP1 pin as the CCP output by clearing the TRISCCP<2> bit.

Note:	Clearing the CCP1CON register will force the RB3/CCP1 compare output latch to						
	the default low level. This is neither the						
	PORTB I/O data latch nor the DATACCP						
	latch.						

7.2.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

7.2.3 SOFTWARE INTERRUPT MODE

When generate software interrupt is chosen the CCP1 pin is not affected. Only a CCP interrupt is generated (if enabled).

7.2.4 SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated which may be used to initiate an action.

The Special Event Trigger output of CCP1 resets the TMR1 register pair. This allows the CCPR1 register to effectively be a 16-bit programmable period register for Timer1.

The Special Event Trigger output of CCP1 also starts an A/D conversion (if the A/D module is enabled).

Note: The Special Event Trigger from the CCP1 module will not set interrupt flag bit TMR1IF (PIR1<0>).

TABLE 7-2: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, AND TIMER1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
07h	DATACCP			—	—	—	DCCP	_	DT1CK	XXXX XXXX	xxxx xuxu
0Bh,8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 0002	0000 000u
0Ch	PIR1		ADIF	—	—	—	CCP1IF	TMR2IF	TMR1IF	-0000	-0000
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register							ter	XXXX XXXX	uuuu uuuu
0Fh	TMR1H	Holding	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register							XXXX XXXX	uuuu uuuu
10h	T1CON			T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu
15h	CCPR1L	Capture	Capture/Compare/PWM Register 1 (LSB)							XXXX XXXX	uuuu uuuu
16h	CCPR1H	Capture	Capture/Compare/PWM Register 1 (MSB)							XXXX XXXX	uuuu uuuu
17h	CCP1CON			DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
87h	TRISCCP			—	—	—	TCCP	_	TT1CK	xxxx x1x1	xxxx x1x1
8Ch	PIE1		ADIE	—	—	—	CCP1IE	TMR2IE	TMR1IE	-0000	-0000

Legend: x = unknown, u = unchanged, — = unimplemented read as '0'. Shaded cells are not used by Capture and Timer1.

7.3 PWM Mode

In Pulse Width Modulation (PWM) mode, the CCP1 pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTB data latch, the TRISCCP<2> bit must be cleared to make the CCP1 pin an output.

Note:	Clearing the CCP1CON register will force						
	the CCP1 PWM output latch to the default						
	low level. This is neither the PORTB I/O						
	data latch nor the DATACCP latch.						

Figure 7-5 shows a simplified block diagram of the CCP module in PWM mode.

For a step by step procedure on how to set up the CCP module for PWM operation, see **Section 7.3.3** "**Set-Up for PWM Operation**".

FIGURE 7-5: SIMPLIFIED PWM BLOCK DIAGRAM



A PWM output (Figure 7-6) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/ period).

FIGURE 7-6: PWM OUTPUT



7.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

PWM period = [(PR2) + 1] • 4 • TOSC • (TMR2 prescale value)

PWM frequency is defined as 1 / [PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note:	The Timer2 postscaler (see Section 6.0							
	"Timer2 Module") is not used in the							
	determination of the PWM frequency. The							
	postscaler could be used to have a servo							
	update rate at a different frequency than							
	the PWM output.							

7.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

PWM duty cycle = (CCPR1L:CCP1CON<5:4>) • Tosc • (TMR2 prescale value)

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2 concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

Maximum PWM resolution (bits) for a given PWM frequency:

$$= \frac{\log\left(\frac{FOSC}{FPWM}\right)}{\log(2)} \quad \text{bits}$$

Note: If the PWM duty cycle value is longer than the PWM period the CCP1 pin will not be cleared.

For an example PWM period and duty cycle calculation, see the $PIC^{\textcircled{B}}$ Mid-Range Reference Manual, (DS33023).

8.4 A/D Conversions

Note:	The GO/DONE bit should NOT be set in
	the same instruction that turns on the A/D.

8.5 Use of the CCP Trigger

An A/D conversion can be started by the "Special Event Trigger" of the CCP1 module. This requires that the CCP1M3:CCP1M0 bits (CCP1CON<3:0>) be programmed as 1011 and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/DONE bit will be set, starting the A/D conversion, and the Timer1 counter will be reset to zero. Timer1 is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving the ADRES to the desired location). The appropriate analog input channel must be selected and the minimum acquisition done before the "Special Event Trigger" sets the GO/ DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), then the "Special Event Trigger" will be ignored by the A/D module, but will still reset the Timer1 counter.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
05h	PORTA		—	(1)	RA4	RA3	RA2	RA1	RA0	xx xxxx	xu uuuu
0Bh,8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	_	_	_	CCP1IF	TMR2IF	TMR1IF	-0000	-0000
1Eh	ADRES	A/D Resu	Result Register						xxxx xxxx	uuuu uuuu	
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON	0000 00-0	0000 00-0
85h	TRISA	—	—	(1)	PORTA I	Data Dire	ction Registe	r		1 1111	1 1111
8Ch	PIE1	—	ADIE	—	_	—	CCP1IE	TMR2IE	TMR1IE	-0000	-0 0000
9Fh	ADCON1		_	_	_	_	PCFG2	PCFG1	PCFG0	000	000

TABLE 8-2: SUMMARY OF A/D REGISTERS

Legend: x = unknown, u = unchanged, — = unimplemented read as '0'. Shaded cells are not used for A/D conversion. **Note 1:** Reserved bits: Do Not Use.

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9.0 SPECIAL FEATURES OF THE CPU

The PIC16C712/716 devices have a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power-saving operating modes and offer code protection. These are:

- OSC Selection
- Reset:
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
 - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Sleep
- Code protection
- ID locations
- In-Circuit Serial Programming[™] (ICSP[™])

These devices have a Watchdog Timer, which can be shut off only through Configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay on power-up only and is designed to keep the part in Reset while the power supply stabilizes. With these two timers on-chip, most applications need no external Reset circuitry. Sleep mode is designed to offer a very low-current Power-Down mode. The user can wake-up from Sleep through external Reset, Watchdog Timer Wake-up, or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost, while the LP crystal option saves power. A set of Configuration bits are used to select various options.

Additional information on special features is available in the $PIC^{\mbox{\tiny B}}$ Mid-Range Reference Manual, (DS33023).

9.1 Configuration Bits

The Configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h-3FFFh), which can be accessed only during programming.

9.2 Oscillator Configurations

9.2.1 OSCILLATOR TYPES

The PIC16CXXX can be operated in four different Oscillator modes. The user can program two Configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low-Power Crystal
- XT Crystal/Resonator
- HS High-Speed Crystal/Resonator
- RC Resistor/Capacitor

9.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 9-2). The PIC16CXXX oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1/ CLKIN pin (Figure 9-3).

FIGURE 9-2:	CRYSTAL/CERAMIC
	RESONATOR OPERATION
	(HS, XT OR LP
	OSC CONFIGURATION)



FIGURE 9-3: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC



TABLE 9-1: CERAMIC RESONATORS

Ranges Tested:

5							
Mode	Freq	OSC1	OSC2				
XT	455 kHz	68-100 pF	68-100 pF				
	2.0 MHz	15-68 pF	15-68 pF				
	4.0 MHz	15-68 pF	15-68 pF				
HS	8.0 MHz	10-68 pF	10-68 pF				
	16.0 MHz	10-22 pF	10-22 pF				
These values are for design guidance only. See							
notes at bottom of page.							

TABLE 9-2:CAPACITOR SELECTION FOR
CRYSTAL OSCILLATOR

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2		
LP	32 kHz	33 pF	33 pF		
	200 kHz	15 pF	15 pF		
XT	200 kHz	47-68 pF	47-68 pF		
	1 MHz	15 pF	15 pF		
	4 MHz	15 pF	15 pF		
HS	4 MHz	15 pF	15 pF		
	8 MHz	15-33 pF	15-33 pF		
	20 MHz	15-33 pF	15-33 pF		
These values are for design guidance only. See notes at bottom of page.					

Note 1:	Recommended values of C1 and C2 are
	identical to the ranges tested (Table 9-1).

- 2: Higher capacitance increases the stability of the oscillator, but also increases the start-up time.
- 3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
- 4: Rs may be required in HS mode, as well as XT mode to avoid overdriving crystals with low drive level specification.

PIC16C712/716







9.9 Power Control/Status Register (PCON)

The Power Control/Status Register, PCON has two bits.

Bit 0 is Brown-out Reset Status bit, $\overline{\text{BOR}}$. If the BODEN Configuration bit is set, $\overline{\text{BOR}}$ is '1' on Power-on Reset. If the BODEN Configuration bit is clear, $\overline{\text{BOR}}$ is unknown on Power-on Reset. The BOR Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (the BODEN Configuration bit is clear). BOR must then be set by the user and checked on subsequent Resets to see if it is clear, indicating a brown-out has occurred.

Bit 1 is $\overrightarrow{\text{POR}}$ (Power-on Reset Status bit). It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

TABLE 9-3:TIME-OUT IN VARIOUS SITUATIONS

Oppillator Configuration	Power	-up	Brown out	Wake-up from	
	PWRTE = 0	PWRTE = 1	Brown-out	Sleep	
XT, HS, LP	72 ms + 1024Tosc	1024Tosc	72 ms + 1024Tosc	1024Tosc	
RC	72 ms	—	72 ms	—	

TABLE 9-4: STATUS BITS AND THEIR SIGNIFICANCE

POR	BOR	ТО	PD	
0	х	1	1	Power-on Reset
0	x	0	x	Illegal, TO is set on POR
0	x	x	0	Illegal, PD is set on POR
1	0	1	1	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	MCLR Reset during normal operation
1	1	1	0	MCLR Reset during Sleep or interrupt wake-up from Sleep

TABLE 9-5: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	0x
MCLR Reset during normal operation	000h	000u uuuu	uu
MCLR Reset during Sleep	000h	0001 Ouuu	uu
WDT Reset	000h	0000 luuu	uu
WDT Wake-up	PC + 1	uuu0 Ouuu	uu
Brown-out Reset	000h	0001 luuu	u0
Interrupt wake-up from Sleep	PC + 1 ⁽¹⁾	uuul Ouuu	uu

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

Register	Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset	Wake-up via WDT or Interrupt
W	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	N/A	N/A	N/A
TMR0	XXXX XXXX	uuuu uuuu	uuuu uuuu
PCL	0000h	0000h	PC + 1 ⁽²⁾
STATUS	0001 1xxx	000q quuu (3)	uuuq quuu (3)
FSR	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA ⁽⁴⁾	0x 0000	xx xxxx	xu uuuu
PORTB ⁽⁵⁾	xxxx xxxx	uuuu uuuu	uuuu uuuu
DATACCP	x-x	u-u	u-u
PCLATH	0 0000	0 0000	u uuuu
INTCON	0000 -00x	0000 -00u	uuuu -uuu (1)
	0000	0000	uuuu (1)
PIRI	-0 0000	-0 0000	-u uuuu (1)
TMR1L	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	XXXX XXXX	uuuu uuuu	uuuu uuuu
T1CON	00 0000	uu uuuu	uu uuuu
TMR2	0000 0000	0000 0000	นนนน นนนน
T2CON	-000 0000	-000 0000	-uuu uuuu
CCPR1L	xxxx xxxx	นนนน นนนน	นนนน นนนน
CCPR1H	xxxx xxxx	นนนน นนนน	นนนน นนนน
CCP1CON	00 0000	00 0000	uu uuuu
ADRES	xxxx xxxx	uuuu uuuu	นนนน นนนน
ADCON0	0000 00-0	0000 00-0	uuuu uu-u
OPTION_REG	1111 1111	1111 1111	นนนน นนนน
TRISA	11 1111	11 1111	uu uuuu
TRISB	1111 1111	1111 1111	uuuu uuuu
TRISCCP	xxxx x1x1	xxxx x1x1	xxxx xuxu
PIF1	0000	0000	uuuu
	-0 0000	-0 0000	-u uuuu
PCON	0q	uq	uq
PR2	1111 1111	1111 1111	1111 1111
ADCON1	000	000	uuu

TABLE 9-6: INITIALIZATION CONDITIONS FOR ALL REGISTERS OF THE PIC16C712/716

Legend: u = unchanged, x = unknown, -= unimplemented bit, read as '0', q = value depends on condition

Note 1: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 9-5 for Reset value for specific condition.

4: On any device Reset, these pins are configured as inputs.

5: This is the value that will be in the port output latch.

9.10 Interrupts

The PIC16C712/716 devices have up to 7 sources of interrupt. The Interrupt Control Register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

Note:	Individual interrupt flag bits are set regard-
	less of the status of their corresponding
	mask bit or the GIE bit.

A Global Interrupt Enable bit, GIE (INTCON<7>) enables (if set) all unmasked interrupts or disables (if cleared) all interrupts. When bit GIE is enabled, and an interrupt's flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in various registers. Individual interrupt bits are set, regardless of the status of the GIE bit. The GIE bit is cleared on Reset.

The "return from interrupt" instruction, RETFIE, exits the interrupt routine, as well as sets the GIE bit, which re-enables interrupts.

The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

The peripheral interrupt flags are contained in the Special Function Registers, PIR1 and PIR2. The corresponding interrupt enable bits are contained in Special Function Registers, PIE1 and PIE2, and the peripheral interrupt enable bit is contained in Special Function Register, INTCON.

When an interrupt is responded to, the GIE bit is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends when the interrupt event occurs. The latency is the same for one or two cycle instructions. Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.



FIGURE 9-14: INTERRUPT LOGIC

9.13 Power-down Mode (Sleep)

Power-Down mode is entered by executing a $\ensuremath{\mathtt{SLEEP}}$ instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the PD bit (STATUS<3>) is cleared, the TO (STATUS<4>) bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP instruction was executed (driving high, low, or high-impedance).

For lowest current consumption in this mode, place all I/O pins at either VDD or VSS, ensure no external circuitry is drawing current from the I/O pin, powerdown the A/D and the disable external clocks. Pull all I/ O pins, that are high-impedance inputs, high or low externally to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

The $\overline{\text{MCLR}}$ pin must be at a logic high level (VIHMC).

9.13.1 WAKE-UP FROM SLEEP

The device can wake up from Sleep through one of the following events:

- 1. External Reset input on $\overline{\text{MCLR}}$ pin.
- 2. Watchdog Timer Wake-up (if WDT was enabled).
- 3. Interrupt from INT pin, RB port change, or some peripheral interrupts.

External MCLR Reset will cause a device Reset. All other events are considered a continuation of program execution and cause a "wake-up". The TO and PD bits in the STATUS register can be used to determine the cause of device Reset. The PD bit, which is set on power-up, is cleared when SLEEP is invoked. The TO bit is cleared if a WDT Time-out occurred (and caused wake-up).

The following peripheral interrupts can wake the device from Sleep:

- 1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
- 2. CCP Capture mode interrupt.
- 3. Special Event Trigger (Timer1 in Asynchronous mode using an external clock).

Other peripherals cannot generate interrupts, since during Sleep, no on-chip clocks are present.

11.7 MPLAB ICE 2000 High-Performance In-Circuit Emulator

The MPLAB ICE 2000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers. Software control of the MPLAB ICE 2000 In-Circuit Emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The architecture of the MPLAB ICE 2000 In-Circuit Emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE 2000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft[®] Windows[®] 32-bit operating system were chosen to best make these features available in a simple, unified application.

11.8 MPLAB ICE 4000 High-Performance In-Circuit Emulator

The MPLAB ICE 4000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for high-end PIC MCUs and dsPIC DSCs. Software control of the MPLAB ICE 4000 In-Circuit Emulator is provided by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 4000 is a premium emulator system, providing the features of MPLAB ICE 2000, but with increased emulation memory and high-speed performance for dsPIC30F and PIC18XXXX devices. Its advanced emulator features include complex triggering and timing, and up to 2 Mb of emulation memory.

The MPLAB ICE 4000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

11.9 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PIC MCUs and can be used to develop for these and other PIC MCUs and dsPIC DSCs. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip's In-Circuit Serial Programming[™] (ICSP[™]) protocol, offers costeffective, in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single stepping and watching variables, and CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real time. MPLAB ICD 2 also serves as a development programmer for selected PIC devices.

11.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.

12.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

Ambient temperature under bias	55°C to +125°C
Storage temperature	
Voltage on any pin with respect to Vss (except VDD, MCLR, and RA4)	0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss	0.3V to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	0V to +13.25V
Voltage on RA4 with respect to Vss	0V to +8.5V
Total power dissipation (Note 1) (PDIP and SOIC)	
Total power dissipation (Note 1) (SSOP)	0.65W
Maximum current out of Vss pin	
Maximum current into Vod pin	250 mA
Input clamp current, IiK (VI < 0 or VI > VDD)	±20 mA
Output clamp current, Iок (Vo < 0 or Vo > VDD)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA and PORTB (combined)	
Maximum current sourced by PORTA and PORTB (combined)	200 mA

- **Note 1:** Power dissipation is calculated as follows: $Pdis = VDD \times \{IDD \sum IOH\} + \sum \{(VDD-VOH) \times IOH\} + \sum (VOI \times IOL)$ **2:** Voltage spikes below Vss at the MCLR/VPP pin, inducing currents greater than 80 mA, may cause latch-up.
 - Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the MCLR/VPP pin rather than pulling this pin directly to Vss.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

12.4 AC (Timing) Characteristics

12.4.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created using one of the following formats:

1.	TppS2ppS
----	----------

2. TppS

Т			
F	Frequency	Т	Time
Lowerc	case letters (pp) and their meanings:	•	
рр			
сс	CCP1	OSC	OSC1
ck	CLKOUT	rd	RD
CS	CS	rw	RD or WR
di	SDI	sc	SCK
do	SDO	SS	SS
dt	Data in	tO	ТОСКІ
io	I/O port	t1	T1CKI
mc	MCLR	wr	WR
Upperc	case letters and their meanings:		
S			
F	Fall	Р	Period
Н	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance





TABLE 12-6: CAPTURE/COMPARE/PWM REQUIREMENTS

Param No.	Sym.	Characteristic			Min	Тур†	Max	Units	Conditions
50*	TccL	CCP1 input low time	No Prescaler		0.5Tcy + 20	_		ns	
			With Prescaler	Standard	10	_	_	ns	
				Extended (LC)	20	_	_	ns	
51*	TccH	CCP1 input high time	No Prescaler		0.5TCY + 20	—	_	ns	
			With Prescaler	Standard	10	_	_	ns	
				Extended (LC)	20	_	_	ns	
52*	TccP	CCP1 input period			<u>3Tcy + 40</u> N			ns	N = prescale value (1,4, or 16)
53*	53* TccR CCP1 output rise time		me	Standard	—	10	25	ns	
				Extended (LC)	_	25	45	ns	
54*	TccF	F CCP1 output fall time		Standard	_	10	25	ns	
				Extended (LC)	_	25	45	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 12-7:A/D CONVERTER CHARACTERISTICS:
PIC16C712/716-04 (COMMERCIAL, INDUSTRIAL, EXTENDED)
PIC16C712/716-20 (COMMERCIAL, INDUSTRIAL, EXTENDED)
PIC16LC712/716-04 (COMMERCIAL, INDUSTRIAL)

Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions	
A01	NR	Resolution	—	_	8-bits	bit	VREF = VDD = 5.12V, VSS £ VAIN £ VREF	
A02	Eabs	Total Absolute error	_	_	< ± 1	LSb	VREF = VDD = 5.12V, VSS £ VAIN £ VREF	
A03	EIL	Integral linearity error	-	_	< ± 1	LSb	VREF = VDD = 5.12V, VSS £ VAIN £ VREF	
A04	Edl	Differential linearity erro	-	_	< ± 1	LSb	VREF = VDD = 5.12V, VSS £ VAIN £ VREF	
A05	Efs	Full scale error	-	—	< ± 1	LSb	VREF = VDD = 5.12V, VSS £ VAIN £ VREF	
A06	EOFF	Offset error	-	—	< ± 1	LSb	VREF = VDD = 5.12V, VSS £ VAIN £ VREF	
A10	—	Monotonicity	_	guaranteed (Note 3)	_	—	VSS £ VAIN £ VREF	
A20	VREF	Reference voltage		2.5V	—	Vdd + 0.3	V	
A25	VAIN	Analog input voltage	Vss - 0.3	—	Vref + 0.3	V		
A30	ZAIN	Recommended impedance of analog voltage source		-	_	10.0	kΩ	
A40	IAD	A/D conversion cur-	Standard	—	180	_	μΑ	Average current consump-
		rent (VDD)	Extended (LC)	—	90	_	μA	tion when A/D is on. (Note 1)
A50	IREF	VREF input current (Note 2)		10	_	1000	μA μA	During VAIN acquisition. Based on differential of VHOLD to VAIN to charge CHOLD, see Section 9.1 "Configuration Bits". During A/D Conversion
							cycle	

2: * These parameters are characterized but not tested.

3: † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current.

The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

3: The A/D conversion result never decreases with an increase in the Input Voltage, and has no missing codes.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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