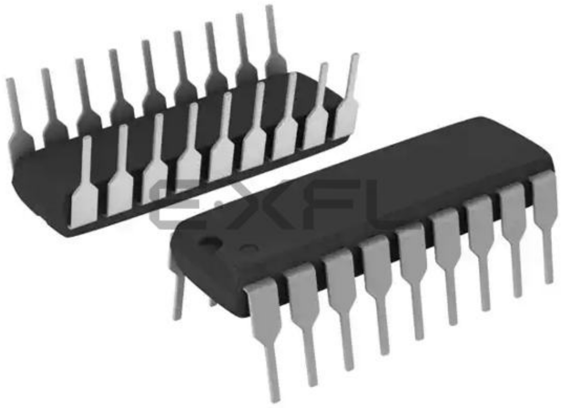

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 13 |
| Program Memory Size | 1.75KB (1K x 14) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 128 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4V ~ 5.5V |
| Data Converters | A/D 4x8b |
| Oscillator Type | External |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 18-DIP (0.300", 7.62mm) |
| Supplier Device Package | 18-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16c712-20-p |

## 2.2 Data Memory Organization

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the Special Function Registers. Bits RP1 and RP0 are the bank select bits.

| RP1(1) | RP0 |
|---|---|

(STATUS<6:5>)

= 00 → Bank 0
= 01 → Bank 1
= 10 → Bank 2 (not implemented)
= 11 → Bank 3 (not implemented)

**Note 1:** Maintain this bit clear to ensure upward compatibility with future products.

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some “high use” Special Function Registers from one bank may be mirrored in another bank for code reduction and quicker access.

### 2.2.1 GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly, or indirectly through the File Select Register FSR (see **Section 2.5 “Indirect Addressing, INDF and FSR Registers”**).

**FIGURE 2-3: REGISTER FILE MAP**

| File Address | Bank 0 | Bank 1 | File Address |
|---|---|---|---|
| 00h | INDF(1) | INDF(1) | 80h |
| 01h | TMR0 | OPTION_REG | 81h |
| 02h | PCL | PCL | 82h |
| 03h | STATUS | STATUS | 83h |
| 04h | FSR | FSR | 84h |
| 05h | PORTA | TRISA | 85h |
| 06h | PORTB | TRISB | 86h |
| 07h | DATACCP | TRISCCP | 87h |
| 08h | | | 88h |
| 09h | | | 89h |
| 0Ah | PCLATH | PCLATH | 8Ah |
| 0Bh | INTCON | INTCON | 8Bh |
| 0Ch | PIR1 | PIE1 | 8Ch |
| 0Dh | | | 8Dh |
| 0Eh | TMR1L | PCON | 8Eh |
| 0Fh | TMR1H | | 8Fh |
| 10h | T1CON | | 90h |
| 11h | TMR2 | | 91h |
| 12h | T2CON | PR2 | 92h |
| 13h | | | 93h |
| 14h | | | 94h |
| 15h | CCPR1L | | 95h |
| 16h | CCPR1H | | 96h |
| 17h | CCP1CON | | 97h |
| 18h | | | 98h |
| 19h | | | 99h |
| 1Ah | | | 9Ah |
| 1Bh | | | 9Bh |
| 1Ch | | | 9Ch |
| 1Dh | | | 9Dh |
| 1Eh | ADRES | | 9Eh |
| 1Fh | ADCON0 | ADCON1 | 9Fh |
| 20h–7Fh | General Purpose Registers 96 Bytes | General Purpose Registers 32 Bytes | A0h–BFh |
| | | | C0h–FFh |

(Blank cells:) Unimplemented data memory locations, read as ‘0’.

**Note 1:** Not a physical register.

**TABLE 3-1: PORTA FUNCTIONS**

| Name | Bit# | Buffer | Function |
|---|---|---|---|
| RA0/AN0 | bit 0 | TTL | Input/output or analog input |
| RA1/AN1 | bit 1 | TTL | Input/output or analog input |
| RA2/AN2 | bit 2 | TTL | Input/output or analog input |
| RA3/AN3/VREF | bit 3 | TTL | Input/output or analog input or VREF |
| RA4/T0CKI | bit 4 | ST | Input/output or external clock input for Timer0<br>Output is open drain type |

**Legend:** TTL = TTL input, ST = Schmitt Trigger input

**TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 05h | PORTA | — | — | —(1) | RA4 | RA3 | RA2 | RA1 | RA0 | --xx xxxx | --xu uuuu |
| 85h | TRISA | — | — | —(1) | PORTA Data Direction Register | | | | | --11 1111 | --11 1111 |
| 9Fh | ADCON1 | — | — | — | — | — | PCFG2 | PCFG1 | PCFG0 | ---- -000 | ---- -000 |

**Legend:** x = unknown, u = unchanged, — = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

**Note 1:** Reserved bits; Do Not Use.

PORTB pins RB3:RB1 are multiplexed with several peripheral functions (Table 3-3). PORTB pins RB3:RB0 have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTB pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify-write instructions (`BSF, BCF, XORWF`) with TRISB as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

Four of PORTB's pins, RB7:RB4, have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt-on-change comparison). The input pins, RB7:RB4, are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

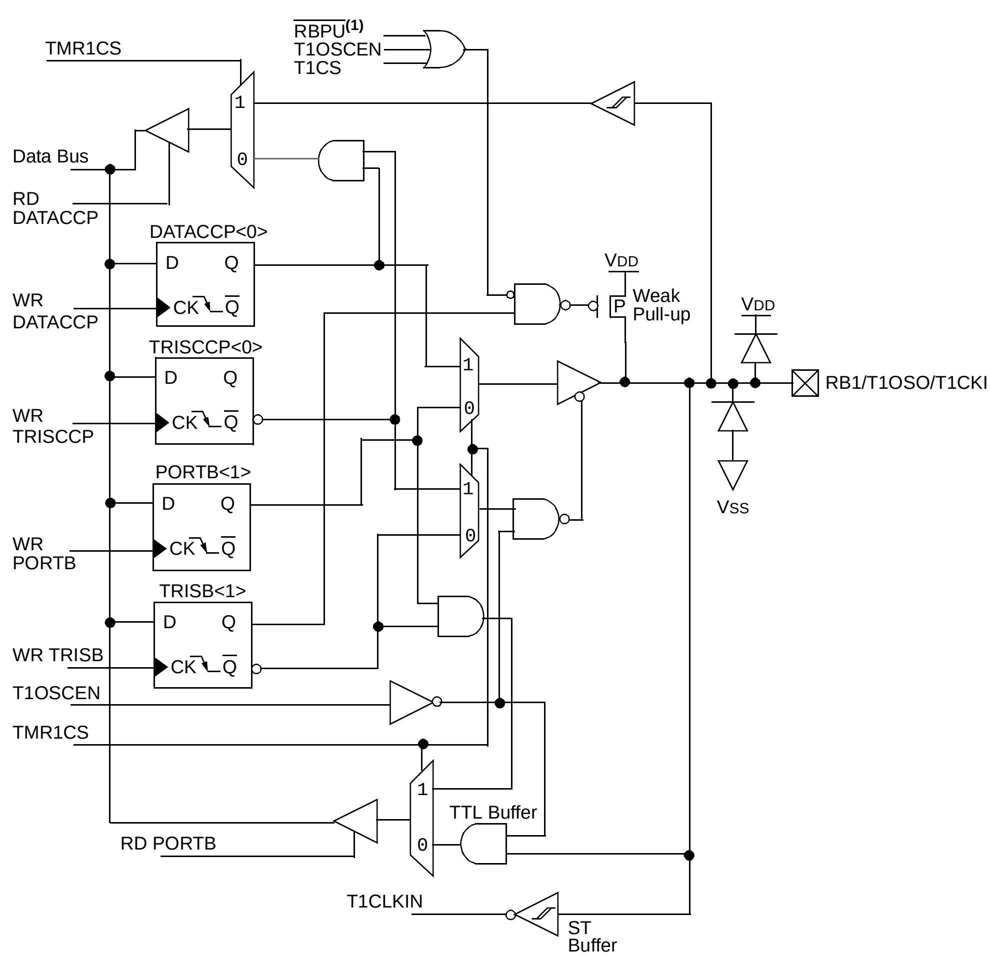
a) Any read or write of PORTB will end the mismatch condition.

b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

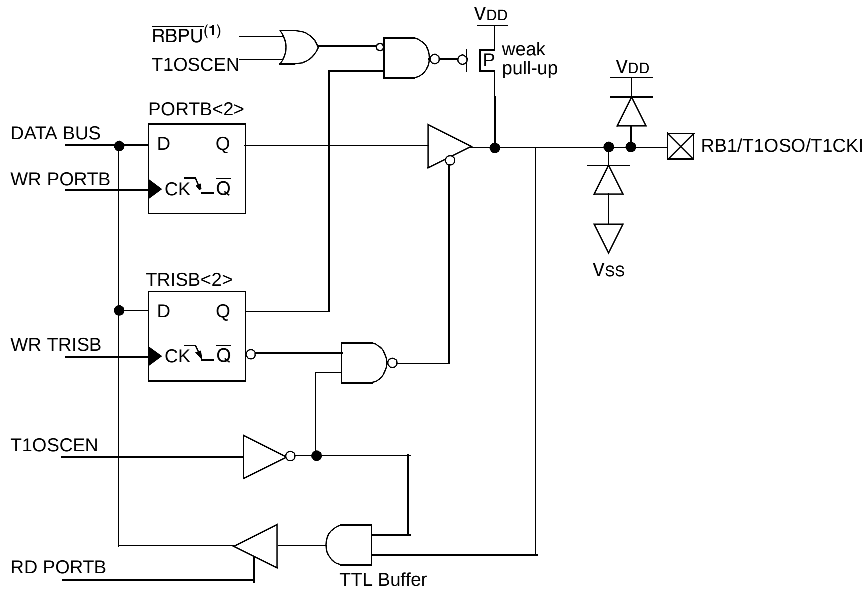
The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

**FIGURE 3-4: BLOCK DIAGRAM OF RB1/T1OSO/T1CKI PIN**



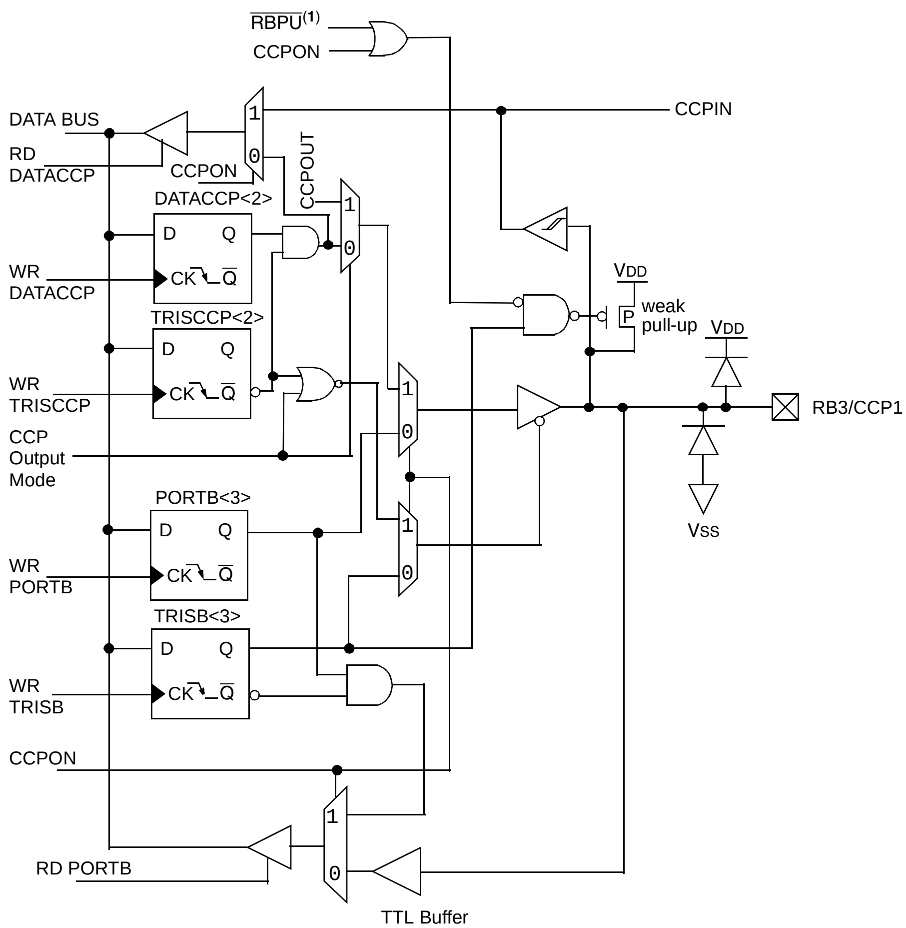

**Note 1:** To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the RBPU bit (OPTION_REG<7>).

**FIGURE 3-5: BLOCK DIAGRAM OF RB2/T1OSI PIN**




**Note 1:** To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the RBPU bit (OPTION_REG<7>).

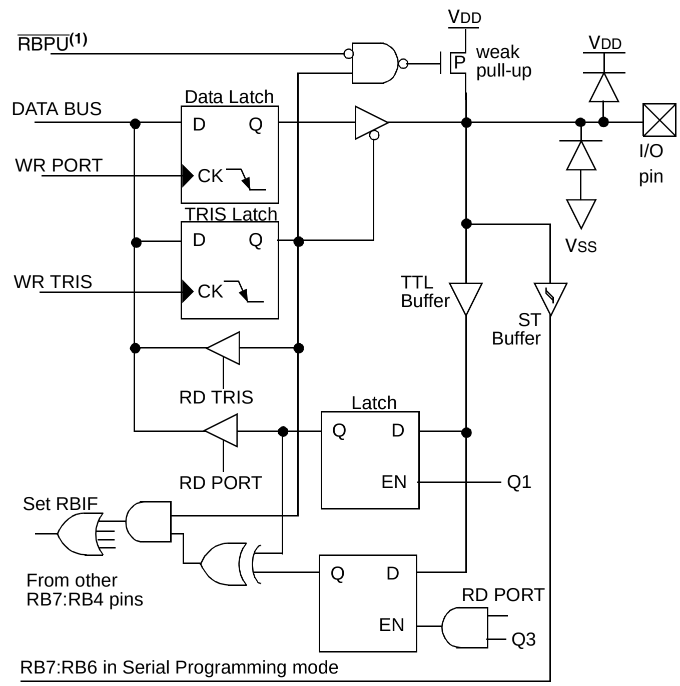
**FIGURE 3-6: BLOCK DIAGRAM OF RB3/CCP1 PIN**




**Note 1:** To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the RBPU bit (OPTION_REG<7>).

**FIGURE 3-7: BLOCK DIAGRAM OF RB7:RB4 PINS**




**Note 1:** To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the RBPU bit (OPTION_REG<7>).

**TABLE 3-3: PORTB FUNCTIONS**

| Name | Bit# | Buffer | Function |
|---|---|---|---|
| RB0/INT | bit 0 | TTL/ST(1) | Input/output pin or external interrupt input. Internal software programmable weak pull-up. |
| RB1/T1OS0/ T1CKI | bit 1 | TTL/ST(1) | Input/output pin or Timer1 oscillator output, or Timer1 clock input. Internal software programmable weak pull-up. See Timer1 section for detailed operation. |
| RB2/T1OSI | bit 2 | TTL/ST(1) | Input/output pin or Timer1 oscillator input. Internal software programmable weak pull-up. See Timer1 section for detailed operation. |
| RB3/CCP1 | bit 3 | TTL/ST(1) | Input/output pin or Capture 1 input, or Compare 1 output, or PWM1 output. Internal software programmable weak pull-up. See CCP1 section for detailed operation. |
| RB4 | bit 4 | TTL | Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. |
| RB5 | bit 5 | TTL | Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. |
| RB6 | bit 6 | TTL/ST(2) | Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming clock. |
| RB7 | bit 7 | TTL/ST(2) | Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming data. |

**Legend:** TTL = TTL input, ST = Schmitt Trigger input

**Note 1:** This buffer is a Schmitt Trigger input when configured as the external interrupt or peripheral input.

**2:** This buffer is a Schmitt Trigger input when used in Serial Programming mode.

## 7.3 PWM Mode

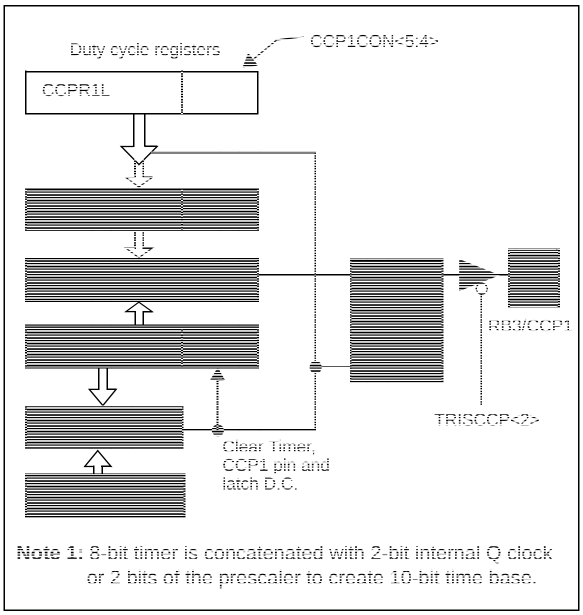
In Pulse Width Modulation (PWM) mode, the CCP1 pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTB data latch, the TRISCCP<2> bit must be cleared to make the CCP1 pin an output.

| | |
|---|---|
| **Note:** | Clearing the CCP1CON register will force the CCP1 PWM output latch to the default low level. This is neither the PORTB I/O data latch nor the DATACCP latch. |

Figure 7-5 shows a simplified block diagram of the CCP module in PWM mode.

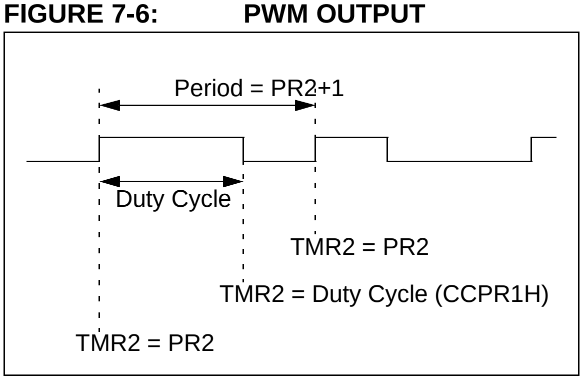
For a step by step procedure on how to set up the CCP module for PWM operation, see **Section 7.3.3 “Set-Up for PWM Operation”**.

**FIGURE 7-5: SIMPLIFIED PWM BLOCK DIAGRAM**




A PWM output (Figure 7-6) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

**FIGURE 7-6: PWM OUTPUT**




### 7.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

$$\textbf{PWM period} = [(PR2) + 1] \cdot 4 \cdot T_{OSC} \cdot (\text{TMR2 prescale value})$$

PWM frequency is defined as 1 / [PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

| | |
|---|---|
| **Note:** | The Timer2 postscaler (see **Section 6.0 “Timer2 Module”**) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output. |

### 7.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

$$\textbf{PWM duty cycle} = (CCPR1L{:}CCP1CON\langle 5{:}4\rangle) \cdot T_{osc} \cdot (\text{TMR2 prescale value})$$

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2 concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

Maximum PWM resolution (bits) for a given PWM frequency:

$$= \frac{\log\left(\frac{F_{OSC}}{F_{PWM}}\right)}{\log(2)} \text{ bits}$$

| | |
|---|---|
| **Note:** | If the PWM duty cycle value is longer than the PWM period the CCP1 pin will not be cleared. |

For an example PWM period and duty cycle calculation, see the PIC® Mid-Range Reference Manual, (DS33023).

**FIGURE 8-2: ADCON1 REGISTER (ADDRESS 9Fh)**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | PCFG2 | PCFG1 | PCFG0 |
| bit7 | | | | | | | bit0 |

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-n = Value at POR Reset

bit 7-3: **Unimplemented:** Read as ‘0’

bit 2-0: **PCFG2:PCFG0**: A/D Port Configuration Control bits

| PCFG2:PCFG0 | RA0 | RA1 | RA2 | RA3 | VREF |
|---|---|---|---|---|---|
| 0x0 | A | A | A | A | VDD |
| 0x1 | A | A | A | VREF | RA3 |
| 100 | A | A | D | A | VDD |
| 101 | A | A | D | VREF | RA3 |
| 11x | D | D | D | D | VDD |

A = Analog input

D = Digital I/O

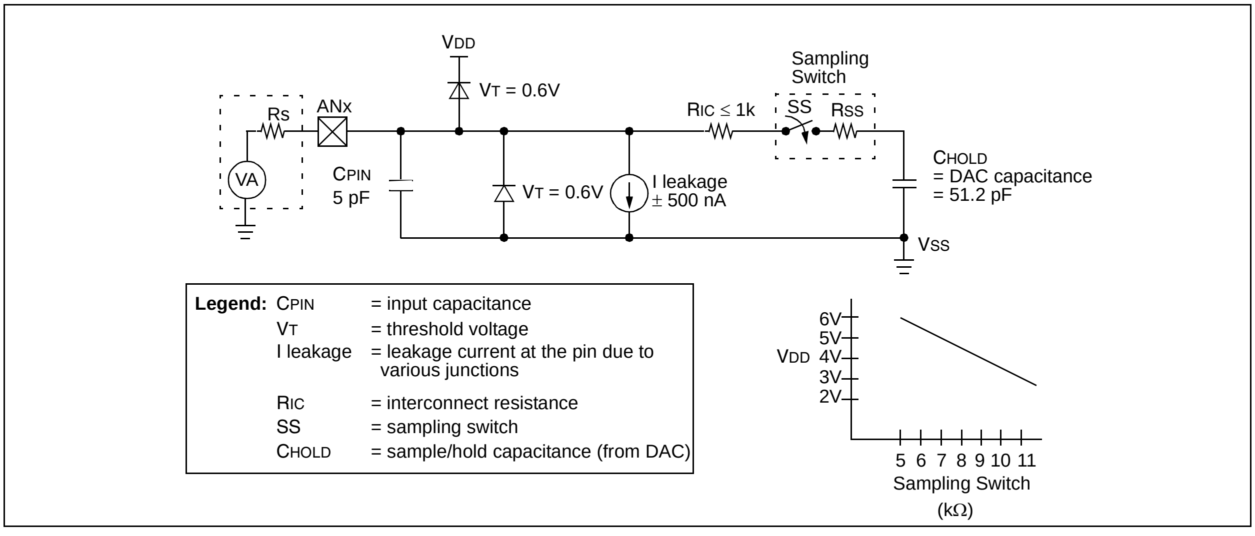
## 8.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the Charge Holding capacitor ($C_{HOLD}$) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 8-4. The source impedance ($R_S$) and the internal sampling switch ($R_{SS}$) impedance directly affect the time required to charge the capacitor $C_{HOLD}$. The sampling switch ($R_{SS}$) impedance varies over the device voltage ($V_{DD}$). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 10 kΩ**. After the analog input channel is selected (changed) this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, $T_{ACQ}$, see the PIC® Mid-Range Reference Manual, (DS33023). This equation calculates the acquisition time to within 1/2 LSb error (512 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified accuracy.

| | |
|---|---|
| **Note:** | When the conversion is started, the holding capacitor is disconnected from the input pin. |

**FIGURE 8-4: ANALOG INPUT MODEL**



## 8.2 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 9.5TAD per 8-bit conversion. The source of the A/D conversion clock is software selectable. The four possible options for TAD are:

- 2TOSC
- 8TOSC
- 32TOSC
- Internal RC oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of 1.6 μs.

Table 8-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

## 8.3 Configuring Analog Port Pins

The ADCON1 and TRISA registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS2:CHS0 bits and the TRIS bits.

**Note 1:** When reading the port register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs, will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.

**2:** Analog levels on any pin that is defined as a digital input (including the AN3:AN0 pins), may cause the input buffer to consume current that is out of the devices specification.

**TABLE 8-1: TAD vs. DEVICE OPERATING FREQUENCIES**

| AD Clock Source (TAD) | | Device Frequency | | | |
|---|---|---|---|---|---|
| **Operation** | **ADCS1:ADCS0** | **20 MHz** | **5 MHz** | **1.25 MHz** | **333.33 kHz** |
| 2TOSC | 00 | 100 ns(2) | 400 ns(2) | 1.6 μs | 6 μs |
| 8TOSC | 01 | 400 ns(2) | 1.6 μs | 6.4 μs | 24 μs(3) |
| 32TOSC | 10 | 1.6 μs | 6.4 μs | 25.6 μs(3) | 96 μs(3) |
| RC(5) | 11 | 2-6 μs(1,4) | 2-6 μs(1,4) | 2-6 μs(1,4) | 2-6 μs(1) |

**Legend:** Shaded cells are outside of recommended range.

**Note 1:** The RC source has a typical TAD time of 4 μs.

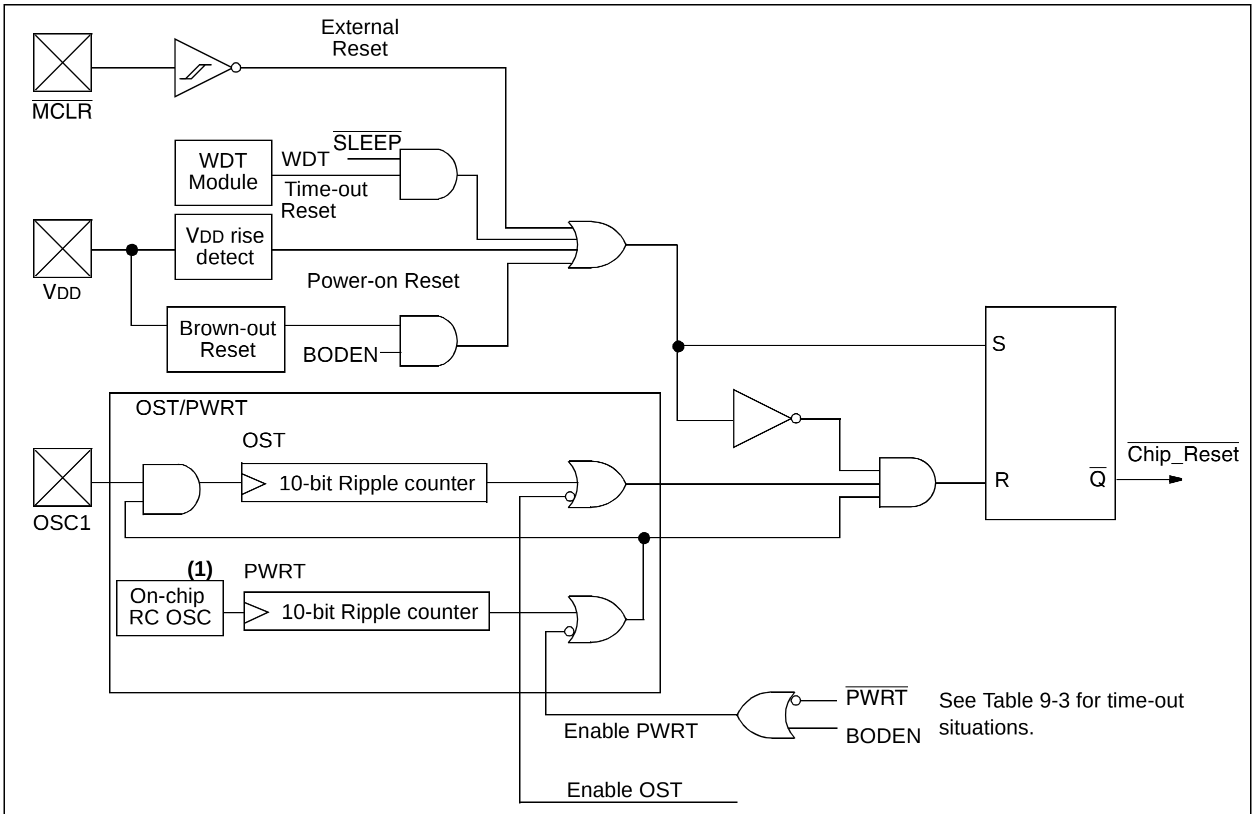
**2:** These values violate the minimum required TAD time.

**3:** For faster conversion times, the selection of another clock source is recommended.

**4:** When device frequency is greater than 1 MHz, the RC A/D conversion clock source is recommended for Sleep operation only.

**5:** For extended voltage devices (LC), please refer to Electrical Specifications section.

**FIGURE 9-6: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT**




**Note 1:** This is a separate oscillator from the RC oscillator of the CLKIN pin.

**FIGURE 9-7: BROWN-OUT SITUATIONS**

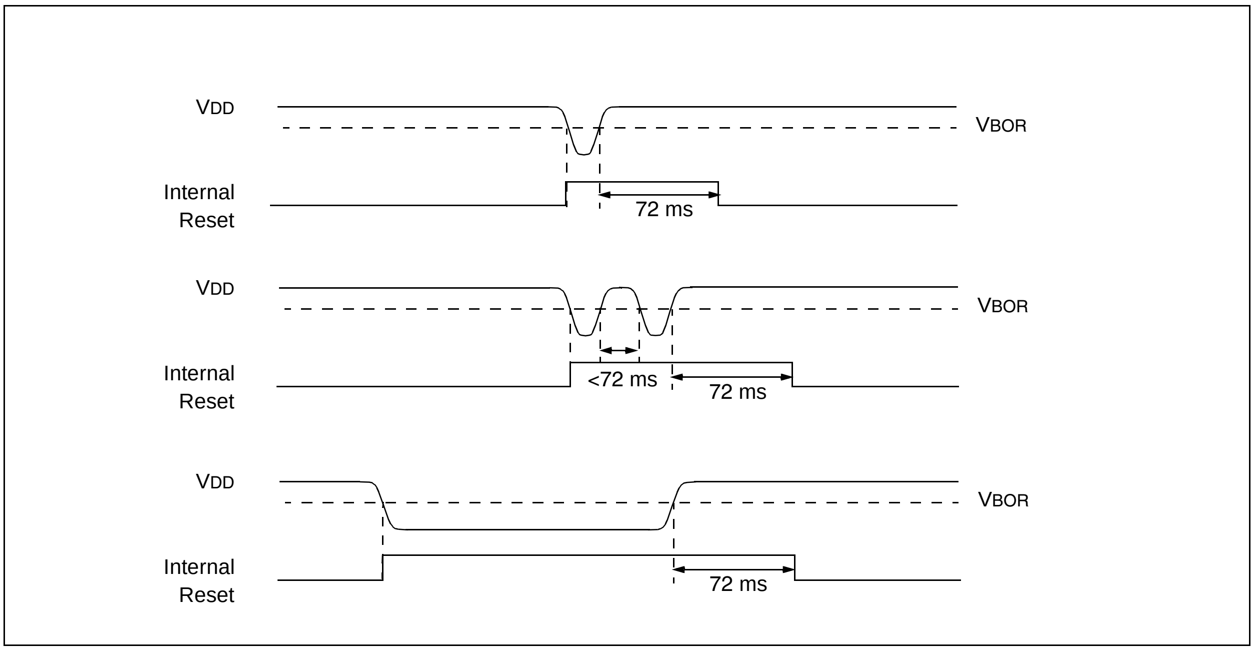


**TABLE 9-6: INITIALIZATION CONDITIONS FOR ALL REGISTERS OF THE PIC16C712/716**

| Register | Power-on Reset, Brown-out Reset | $\overline{\text{MCLR}}$ Resets WDT Reset | Wake-up via WDT or Interrupt |
|---|---|---|---|
| W | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| INDF | N/A | N/A | N/A |
| TMR0 | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PCL | 0000h | 0000h | PC + 1(2) |
| STATUS | 0001 1xxx | 000q quuu(3) | uuuq quuu(3) |
| FSR | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PORTA(4) | --0x 0000 | --xx xxxx | --xu uuuu |
| PORTB(5) | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| DATACCP | ---- -x-x | ---- -u-u | ---- -u-u |
| PCLATH | ---0 0000 | ---0 0000 | ---u uuuu |
| INTCON | 0000 -00x | 0000 -00u | uuuu -uuu(1) |
| PIR1 | ---- 0000 | ---- 0000 | ---- uuuu(1) |
| | -0-- 0000 | -0-- 0000 | -u-- uuuu(1) |
| TMR1L | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| TMR1H | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| T1CON | --00 0000 | --uu uuuu | --uu uuuu |
| TMR2 | 0000 0000 | 0000 0000 | uuuu uuuu |
| T2CON | -000 0000 | -000 0000 | -uuu uuuu |
| CCPR1L | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| CCPR1H | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| CCP1CON | --00 0000 | --00 0000 | --uu uuuu |
| ADRES | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| ADCON0 | 0000 00-0 | 0000 00-0 | uuuu uu-u |
| OPTION_REG | 1111 1111 | 1111 1111 | uuuu uuuu |
| TRISA | --11 1111 | --11 1111 | --uu uuuu |
| TRISB | 1111 1111 | 1111 1111 | uuuu uuuu |
| TRISCCP | xxxx x1x1 | xxxx x1x1 | xxxx xuxu |
| PIE1 | ---- 0000 | ---- 0000 | ---- uuuu |
| | -0-- 0000 | -0-- 0000 | -u-- uuuu |
| PCON | ---- --0q | ---- --uq | ---- --uq |
| PR2 | 1111 1111 | 1111 1111 | 1111 1111 |
| ADCON1 | ---- -000 | ---- -000 | ---- -uuu |

**Legend:** u = unchanged, x = unknown, – = unimplemented bit, read as '0', q = value depends on condition

**Note 1:** One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

**2:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

**3:** See Table 9-5 for Reset value for specific condition.

**4:** On any device Reset, these pins are configured as inputs.

**5:** This is the value that will be in the port output latch.

## 9.10 Interrupts

The PIC16C712/716 devices have up to 7 sources of interrupt. The Interrupt Control Register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

| **Note:** | Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit. |
|---|---|

A Global Interrupt Enable bit, GIE (INTCON<7>) enables (if set) all unmasked interrupts or disables (if cleared) all interrupts. When bit GIE is enabled, and an interrupt's flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in various registers. Individual interrupt bits are set, regardless of the status of the GIE bit. The GIE bit is cleared on Reset.

The "return from interrupt" instruction, `RETFIE`, exits the interrupt routine, as well as sets the GIE bit, which re-enables interrupts.

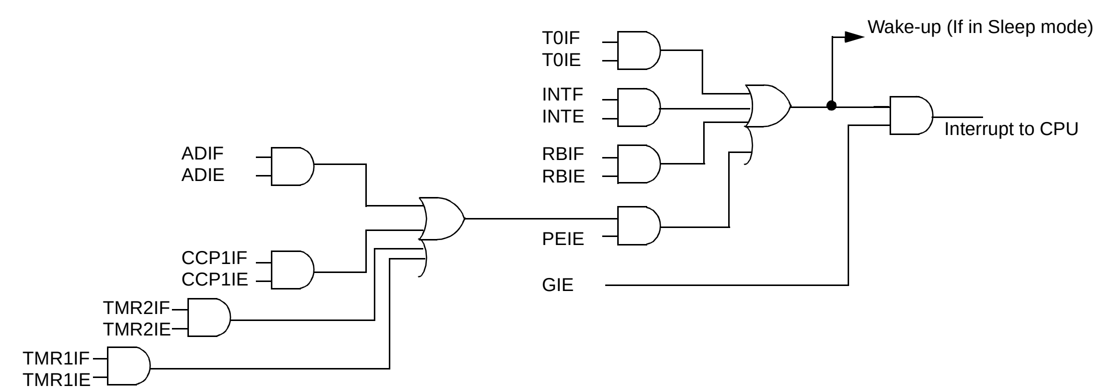
The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

The peripheral interrupt flags are contained in the Special Function Registers, PIR1 and PIR2. The corresponding interrupt enable bits are contained in Special Function Registers, PIE1 and PIE2, and the peripheral interrupt enable bit is contained in Special Function Register, INTCON.

When an interrupt is responded to, the GIE bit is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends when the interrupt event occurs. The latency is the same for one or two cycle instructions. Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

**FIGURE 9-14: INTERRUPT LOGIC**



## 9.13 Power-down Mode (Sleep)

Power-Down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{\text{PD}}$ bit (STATUS<3>) is cleared, the $\overline{\text{TO}}$ (STATUS<4>) bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP instruction was executed (driving high, low, or high-impedance).

For lowest current consumption in this mode, place all I/O pins at either $V_{DD}$ or $V_{SS}$, ensure no external circuitry is drawing current from the I/O pin, power-down the A/D and the disable external clocks. Pull all I/O pins, that are high-impedance inputs, high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at $V_{DD}$ or $V_{SS}$ for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

The $\overline{\text{MCLR}}$ pin must be at a logic high level ($V_{IHMC}$).

### 9.13.1 WAKE-UP FROM SLEEP

The device can wake up from Sleep through one of the following events:

1. External Reset input on $\overline{\text{MCLR}}$ pin.
2. Watchdog Timer Wake-up (if WDT was enabled).
3. Interrupt from INT pin, RB port change, or some peripheral interrupts.

External $\overline{\text{MCLR}}$ Reset will cause a device Reset. All other events are considered a continuation of program execution and cause a “wake-up”. The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits in the STATUS register can be used to determine the cause of device Reset. The $\overline{\text{PD}}$ bit, which is set on power-up, is cleared when SLEEP is invoked. The $\overline{\text{TO}}$ bit is cleared if a WDT Time-out occurred (and caused wake-up).

The following peripheral interrupts can wake the device from Sleep:

1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
2. CCP Capture mode interrupt.
3. Special Event Trigger (Timer1 in Asynchronous mode using an external clock).

Other peripherals cannot generate interrupts, since during Sleep, no on-chip clocks are present.

## 11.11 PICSTART Plus Development Programmer

The PICSTART Plus Development Programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus Development Programmer supports most PIC devices in DIP packages up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus Development Programmer is CE compliant.

## 11.12 Demonstration, Development and Evaluation Boards

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart® battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Check the Microchip web page (www.microchip.com) and the latest *“Product Selector Guide”* (DS00148) for the complete list of demonstration, development and evaluation kits.

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature 0°C ≤ $T_A$ ≤ +70°C for commercial<br>-40°C ≤ $T_A$ ≤ +85°C for industrial<br>-40°C ≤ $T_A$ ≤ +125°C for extended<br>Operating voltage $V_{DD}$ range as described in DC spec **Section 12.1 "DC Characteristics: PIC16C712/716-04 (Commercial, Industrial, Extended) PIC16C712/716-20 (Commercial, Industrial, Extended)"** and **Section 12.2 "DC Characteristics: PIC16LC712/716-04 (Commercial, Industrial)"** | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ†** | **Max.** | **Units** | **Conditions** |
| | | **Output Low Voltage** | | | | | |
| D080 | $V_{OL}$ | I/O ports | — | — | 0.6 | V | $I_{OL}$ = 8.5 mA, $V_{DD}$ = 4.5V, -40°C to +85°C |
| | | | — | — | 0.6 | V | $I_{OL}$ = 7.0 mA, $V_{DD}$ = 4.5V, -40°C to +125°C |
| D083 | | OSC2/CLKOUT (RC Osc mode) | — | — | 0.6 | V | $I_{OL}$ = 1.6 mA, $V_{DD}$ = 4.5V, -40°C to +85°C |
| | | | — | — | 0.6 | V | $I_{OL}$ = 1.2 mA, $V_{DD}$ = 4.5V, -40°C to +125°C |
| | | **Output High Voltage** | | | | | |
| D090 | $V_{OH}$ | I/O ports **(Note 3)** | $V_{DD}$-0.7 | — | — | V | $I_{OH}$ = -3.0 mA, $V_{DD}$ = 4.5V, -40°C to +85°C |
| | | | $V_{DD}$-0.7 | — | — | V | $I_{OH}$ = -2.5 mA, $V_{DD}$ = 4.5V, -40°C to +125°C |
| D092 | | OSC2/CLKOUT (RC Osc mode) | $V_{DD}$-0.7 | — | — | V | $I_{OH}$ = -1.3 mA, $V_{DD}$ = 4.5V, -40°C to +85°C |
| | | | $V_{DD}$-0.7 | — | — | V | $I_{OH}$ = -1.0 mA, $V_{DD}$ = 4.5V, -40°C to +125°C |
| D150* | $V_{OD}$ | **Open-Drain High Voltage** | — | — | 8.5 | V | RA4 pin |
| | | **Capacitive Loading Specs on Output Pins** | | | | | |
| D100 | $C_{OSC2}$ | OSC2 pin | — | — | 15 | pF | In XT, HS and LP modes when external clock is used to drive OSC1. |
| D101 | $C_{IO}$ | All I/O pins and OSC2 (in RC mode) | — | — | 50 | pF | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In RC Oscillator mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC MCU be driven with external clock in RC mode.

**2:** The leakage current on the $\overline{MCLR}$/$V_{PP}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as current sourced by the pin.

## 12.4 AC (Timing) Characteristics

### 12.4.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created using one of the following formats:

1. TppS2ppS
2. TppS

| **T** | | | |
|---|---|---|---|
| F | Frequency | T | Time |

Lowercase letters (pp) and their meanings:

| **pp** | | | |
|---|---|---|---|
| cc | CCP1 | osc | OSC1 |
| ck | CLKOUT | rd | $\overline{\text{RD}}$ |
| cs | $\overline{\text{CS}}$ | rw | $\overline{\text{RD}}$ or $\overline{\text{WR}}$ |
| di | SDI | sc | SCK |
| do | SDO | ss | $\overline{\text{SS}}$ |
| dt | Data in | t0 | T0CKI |
| io | I/O port | t1 | T1CKI |
| mc | $\overline{\text{MCLR}}$ | wr | $\overline{\text{WR}}$ |

Uppercase letters and their meanings:

| **S** | | | |
|---|---|---|---|
| F | Fall | P | Period |
| H | High | R | Rise |
| I | Invalid (High-impedance) | V | Valid |
| L | Low | Z | High-impedance |

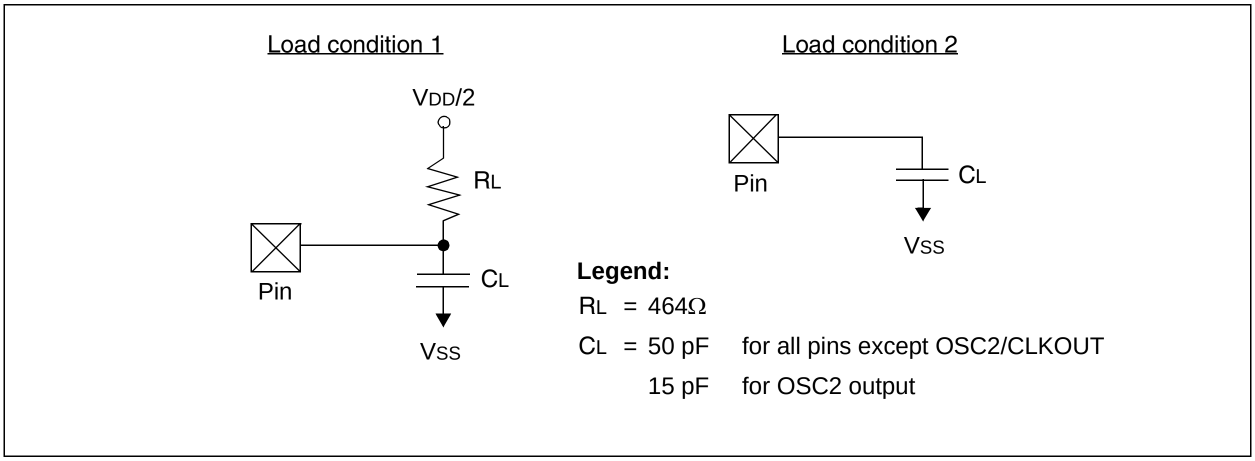
### 12.4.2 TIMING CONDITIONS

The temperature and voltages specified in Table 12-1 apply to all timing specifications, unless otherwise noted. Figure 12-3 specifies the load conditions for the timing specifications.

**TABLE 12-1: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC**

| | |
|---|---|
| **AC CHARACTERISTICS** | **Standard Operating Conditions (unless otherwise stated)**<br>Operating temperature 0°C ≤ $T_A$ ≤ +70°C for commercial<br>-40°C ≤ $T_A$ ≤ +85°C for industrial<br>-40°C ≤ $T_A$ ≤ +125°C for extended<br>Operating voltage $V_{DD}$ range as described in DC spec **Section 12.1 "DC Characteristics: PIC16C712/716-04 (Commercial, Industrial, Extended) PIC16C712/716-20 (Commercial, Industrial, Extended)"** and **Section 12.2 "DC Characteristics: PIC16LC712/716-04 (Commercial, Industrial)"**.<br>LC parts operate for commercial/industrial temp's only. |

**FIGURE 12-3: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**



### TABLE 12-7: A/D CONVERTER CHARACTERISTICS: PIC16C712/716-04 (COMMERCIAL, INDUSTRIAL, EXTENDED) PIC16C712/716-20 (COMMERCIAL, INDUSTRIAL, EXTENDED) PIC16LC712/716-04 (COMMERCIAL, INDUSTRIAL)

| Param No. | Sym. | Characteristic | | Min. | Typ† | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| A01 | NR | Resolution | | — | — | 8-bits | bit | VREF = VDD = 5.12V, VSS £ VAIN £ VREF |
| A02 | EABS | Total Absolute error | | — | — | < ± 1 | LSb | VREF = VDD = 5.12V, VSS £ VAIN £ VREF |
| A03 | EIL | Integral linearity error | | — | — | < ± 1 | LSb | VREF = VDD = 5.12V, VSS £ VAIN £ VREF |
| A04 | EDL | Differential linearity error | | — | — | < ± 1 | LSb | VREF = VDD = 5.12V, VSS £ VAIN £ VREF |
| A05 | EFS | Full scale error | | — | — | < ± 1 | LSb | VREF = VDD = 5.12V, VSS £ VAIN £ VREF |
| A06 | EOFF | Offset error | | — | — | < ± 1 | LSb | VREF = VDD = 5.12V, VSS £ VAIN £ VREF |
| A10 | — | Monotonicity | | — | guaranteed **(Note 3)** | — | — | VSS £ VAIN £ VREF |
| A20 | VREF | Reference voltage | | 2.5V | — | VDD + 0.3 | V | |
| A25 | VAIN | Analog input voltage | | VSS - 0.3 | — | VREF + 0.3 | V | |
| A30 | ZAIN | Recommended impedance of analog voltage source | | — | — | 10.0 | kΩ | |
| A40 | IAD | A/D conversion current (VDD) | Standard | — | 180 | — | μA | Average current consumption when A/D is on. **(Note 1)** |
| | | | Extended (LC) | — | 90 | — | μA | |
| A50 | IREF | VREF input current **(Note 2)** | | 10 | — | 1000 | μA | During VAIN acquisition. Based on differential of VHOLD to VAIN to charge CHOLD, see **Section 9.1 "Configuration Bits"**. |
| | | | | — | — | 10 | μA | During A/D Conversion cycle |

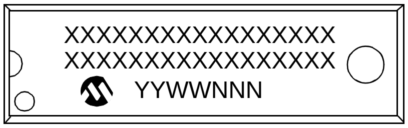
**2:** * These parameters are characterized but not tested.
**3:** † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.
**2:** VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.
**3:** The A/D conversion result never decreases with an increase in the Input Voltage, and has no missing codes.

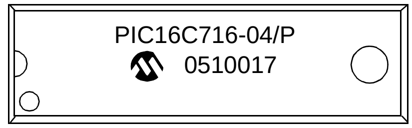
# 13.0 PACKAGING INFORMATION

## 13.1 Package Marking Information

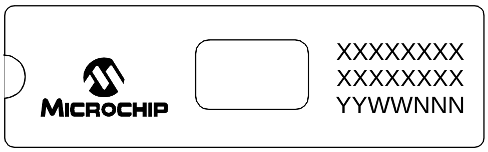
18-Lead PDIP



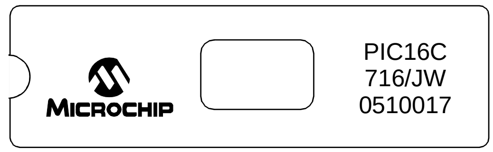

Example



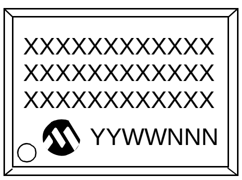

18-Lead CERDIP Windowed



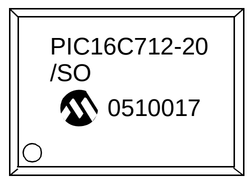

Example



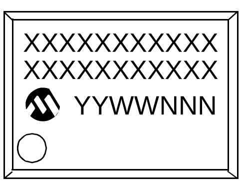

18-Lead SOIC (.300")



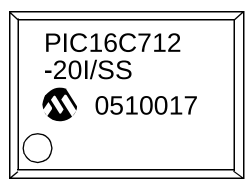

Example




20-Lead SSOP




Example




| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | e3 | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## Q



## R



## S



## T

