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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	·
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	OTP
EEPROM Size	
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c712-20e-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Key Features PIC [®] Mid-Range Reference Manual (DS33023)	PIC16C712	PIC16C716
Operating Frequency	DC – 20 MHz	DC – 20 MHz
Resets (and Delays)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)
Program Memory (14-bit words)	1K	2К
Data Memory (bytes)	128	128
Interrupts	7	7
I/O Ports	Ports A,B	Ports A,B
Timers	3	3
Capture/Compare/PWM modules	1	1
8-bit Analog-to-Digital Module	4 input channels	4 input channels

PIC16C7XX FAMILY OF DEVICES

		PIC16C710	PIC16C71	PIC16C711	PIC16C712	PIC16C715	PIC16C716	PIC16C72A	PIC16C73B
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20	20	20	20	20
Memory	EPROM Program Memory (x14 words)	512	1K	1K	1K	2K	2K	2K	4K
	Data Memory (bytes)	36	36	68	128	128	128	128	192
	Timer Module(s)	TMR0	TMR0	TMR0	TMR0 TMR1 TMR2	TMR0	TMR0 TMR1 TMR2	TMR0 TMR1 TMR2	TMR0 TMR1 TMR2
Peripherals	Capture/Compare/ PWM Module(s)	—	—	—	1	—	1	1	2
	Serial Port(s) (SPI™/I ² C™, USART)	—	—	—	—	—	—	SPI/I ² C	SPI/I ² C, USART
	A/D Converter (8-bit) Channels	4	4	4	4	4	4	5	5
	Interrupt Sources	4	4	4	7	4	7	8	11
	I/O Pins	13	13	13	13	13	13	22	22
	Voltage Range (Volts)	2.5-6.0	3.0-6.0	2.5-6.0	2.5-5.5	2.5-5.5	2.5-5.5	2.5-5.5	2.5-5.5
Features	In-Circuit Serial Programming™	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Brown-out Reset	Yes	_	Yes	Yes	Yes	Yes	Yes	Yes
	Packages	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin SDIP, SOIC, SSOP	28-pin SDIP, SOIC

1.0 **DEVICE OVERVIEW**

This document contains device-specific information. Additional information may be found in the PIC[®] Mid-Range Reference Manual, (DS33023), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip web site. The Reference Manual should be considered a complementary document to this data sheet, and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

FIGURE 1-1.
FIGURE 1-1

There are two devices (PIC16C712, PIC16C716) covered by this data sheet.

Figure 1-1 is the block diagram for both devices. The pinouts are listed in Table 1-1.



NOTES:

2.3 PCL and PCLATH

The Program Counter (PC) specifies the address of the instruction to fetch for execution. The PC is 13 bits wide. The low byte is called the PCL register. This register is readable and writable. The high byte is called the PCH register. This register contains the PC<12:8> bits and is not directly readable or writable. All updates to the PCH register go through the PCLATH register.

2.3.1 STACK

The stack allows a combination of up to 8 program calls and interrupts to occur. The stack contains the return address from this branch in program execution.

Mid-range devices have an 8-level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not modified when the stack is PUSHed or POPed.

After the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

2.4 Program Memory Paging

The CALL and GOTO instructions provide 11 bits of address to allow branching within any 2K program memory page. When doing a CALL or GOTO instruction, the upper bit of the address is provided by PCLATH<3>. When doing a CALL or GOTO instruction, the user must ensure that the page select bit is programmed so that the desired program memory page is addressed. If a return from a CALL instruction (or interrupt) is executed, the entire 13-bit PC is pushed onto the stack. Therefore, manipulation of the PCLATH<3> bit is not required for the return instructions (which POPs the address from the stack).

Name	Bit#	Buffer	Function
RA0/AN0	bit 0	TTL	Input/output or analog input
RA1/AN1	bit 1	TTL	Input/output or analog input
RA2/AN2	bit 2	TTL	Input/output or analog input
RA3/AN3/VREF	bit 3	TTL	Input/output or analog input or VREF
			Input/output or external clock input for Timer0
RA4/T0CKI	bit 4	ST	Output is open drain type

TABLE 3-1: PORTA FUNCTIONS

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
05h	PORTA	—		_(1)	RA4	RA3	RA2	RA1	RA0	xx xxxx	xu uuuu
85h	TRISA	_	_	_(1)	PORT	PORTA Data Direction Register				11 1111	11 1111
9Fh	ADCON1	—					PCFG2	PCFG1	PCFG0	000	000

Legend: x = unknown, u = unchanged, — = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

Note 1: Reserved bits; Do Not Use.

PORTB pins RB3:RB1 are multiplexed with several peripheral functions (Table 3-3). PORTB pins RB3:RB0 have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTB pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modifywrite instructions (BSF, BCF, XORWF) with TRISB as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

Four of PORTB's pins, RB7:RB4, have an interrupt-onchange feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupton-change comparison). The input pins, RB7:RB4, are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- a) Any read or write of PORTB will end the mismatch condition.
- b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.



FIGURE 3-4: BLOCK DIAGRAM OF RB1/T10S0/T1CKI PIN

4.0 **TIMER0 MODULE**

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- · Internal or external clock select
- Edge select for external clock
- 8-bit software programmable prescaler
- · Interrupt on overflow from FFh to 00h

Figure 4-1 is a simplified block diagram of the Timer0 module.

Additional information on timer modules is available in the PIC[®] Mid-Range Reference Manual, (DS33023).

4.1 **Timer0** Operation

Timer0 can operate as a timer or as a counter.

Timer mode is selected by clearing bit T0CS (OPTION_REG<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit T0CS (OPTION_REG<5>). In Counter mode, Timer0 will increment on every rising or falling edge of pin RA4/ T0CKI. The incrementing edge is determined by the Edge Select Timer0 Source bit TOSE (OPTION_REG<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed below.

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (Tosc). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

Additional information on external clock requirements is available in the PIC[®] Mid-Range Reference Manual, (DS33023).

4.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module or as a postscaler for the Watchdog Timer, respectively (Figure 4-2). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available, which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer and vice-versa.

The prescaler is not readable or writable.

The PSA and PS2:PS0 bits (OPTION_REG<3:0>) determine the prescaler assignment and prescale ratio.

Clearing bit PSA will assign the prescaler to the Timer0 module. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable.

Setting bit PSA will assign the prescaler to the Watchdog Timer (WDT). When the prescaler is assigned to the WDT, prescale values of 1:1, 1:2, ..., 1:128 are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT.

Note: Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count, but will not change the prescaler assignment.



FIGURE 4-1: TIMER0 BLOCK DIAGRAM

TMR1 Module Mode	Clock Source	Control Bits	TMR1 Module Operation	PORTB<2:1> Operation
Off	N/A	T1CON =xx 0x00	Off	PORTB<2:1> function as normal I/O
Timer	Fosc/4	T1CON =xx 0x01	TMR1 module uses the main oscillator as clock source. TMR1ON can turn on or turn off Timer1.	PORTB<2:1> function as normal I/O
Counter	External circuit	T1CON =xx 0x11 TR1SCCP =x-1	TMR1 module uses the external signal on the RB1/T1OSO/ T1CKI pin as a clock source. TMR1ON can turn on or turn off Timer1. DT1CK can read the signal on the RB1/T1OSO/ T1CKI pin.	PORTB<2> functions as normal I/O. PORTB<1> always reads '0' when configured as input. If PORTB<1> is configured as out- put, reading PORTB<1> will read the data latch. Writing to PORTB<1> will always store the
	Firmware	T1CON =xx 0x11 TR1SCCP =x-0	DATACCP<0> bit drives RB1/ T1OSO/T1CKI and produces the TMR1 clock source. TMR1ON can turn on or turn off Timer1. The DATACCP<0> bit, DT1CK, can read and write to the RB1/T1OSO/T1CKI pin.	result in the data latch, but not to the RB1/T1OSO/T1CKI pin. If the TMR1CS bit is cleared (TMR1 reverts to the timer mode), then pin PORTB<1> will be driven with the value in the data latch.
	Timer1 oscillator	T1CON =xx 1x11	RB1/T1OSO/T1CKI and RB2/ T1OSI are configured as a 2 pin crystal oscillator. RB1/T1OSI/ T1CKI is the clock input for TMR1. TMR1ON can turn on or turn off Timer1. DATACCP<1> bit, DT1CK, always reads '0' as input and can not write to the RB1/T1OSO/T1CK1 pin.	PORTB<2:1> always read '0' when configured as inputs. If PORTB<2:1> are configured as outputs, reading PORTB<2:1> will read the data latches. Writ- ing to PORTB<2:1> will always store the result in the data latches, but not to the RB2/ T1OSI and RB1/T1OSO/T1CKI pins. If the TMR1CS and T1OSCEN bits are cleared (TMR1 reverts to the timer mode and TMR1 oscillator is disabled), then pin PORTB<2:1> will be driven with the value in the data latches.

TABLE 5-1: TMR1 MODULE AND PORTB OPERATION

NOTES:

7.1 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin RB3/CCP1. An event is defined as:

- every falling edge
- every rising edge
- every 4th rising edge
- every 16th rising edge

An event is selected by control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit CCP1IF (PIR1<2>) is set. It must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value will be lost.

FIGURE 7-3:

CAPTURE MODE OPERATION BLOCK DIAGRAM



7.1.1 CCP PIN CONFIGURATION

In Capture mode, the CCP output must be disabled by setting the TRISCCP<2> bit.

Note: If the RB3/CCP1 is configured as an output by clearing the TRISCCP<2> bit, a write to the DCCP bit can cause a capture condition.

7.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

7.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep bit CCP1IE (PIE1<2>) clear to avoid false interrupts and should clear the flag bit CCP1IF following any such change in Operating mode.

7.1.4 CCP PRESCALER

There are four prescaler settings, specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. This means that any Reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore the first capture may be from a non-zero prescaler. Example 7-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

EXAMPLE 7-1: CHANGING BETWEEN CAPTURE PRESCALERS

CLRF	CCP1CON	;Turn CCP module off
MOVLW	NEW_CAPT_PS	;Load the W reg with
		; the new prescaler
		; mode value and CCP ON
MOVWF	CCP1CON	;Load CCP1CON with this
		; value

FIGURE 8-2: ADCON1 REGISTER (ADDRESS 9Fh)



9.9 Power Control/Status Register (PCON)

The Power Control/Status Register, PCON has two bits.

Bit 0 is Brown-out Reset Status bit, $\overline{\text{BOR}}$. If the BODEN Configuration bit is set, $\overline{\text{BOR}}$ is '1' on Power-on Reset. If the BODEN Configuration bit is clear, $\overline{\text{BOR}}$ is unknown on Power-on Reset. The BOR Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (the BODEN Configuration bit is clear). BOR must then be set by the user and checked on subsequent Resets to see if it is clear, indicating a brown-out has occurred.

Bit 1 is $\overrightarrow{\text{POR}}$ (Power-on Reset Status bit). It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

TABLE 9-3:TIME-OUT IN VARIOUS SITUATIONS

Occillator Configuration	Power	-up	Brown out	Wake-up from
	PWRTE = 0	PWRTE = 1	Brown-out	Sleep
XT, HS, LP	72 ms + 1024Tosc	1024Tosc	72 ms + 1024Tosc	1024Tosc
RC	72 ms	—	72 ms	—

TABLE 9-4: STATUS BITS AND THEIR SIGNIFICANCE

POR	BOR	ТО	PD	
0	x	1	1	Power-on Reset
0	x	0	x	Illegal, TO is set on POR
0	x	x	0	Illegal, PD is set on POR
1	0	1	1	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	MCLR Reset during normal operation
1	1	1	0	MCLR Reset during Sleep or interrupt wake-up from Sleep

TABLE 9-5: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	0x
MCLR Reset during normal operation	000h	000u uuuu	uu
MCLR Reset during Sleep	000h	0001 Ouuu	uu
WDT Reset	000h	0000 luuu	uu
WDT Wake-up	PC + 1	uuu0 Ouuu	uu
Brown-out Reset	000h	0001 luuu	u0
Interrupt wake-up from Sleep	PC + 1 ⁽¹⁾	uuul Ouuu	uu

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

9.10.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered, either rising if bit INTEDG (OPTION_REG<6>) is set, or falling if the INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, flag bit INTF (INTCON<1>) is set. This interrupt can be disabled by clearing enable bit INTE (INTCON<4>). Flag bit INTF must be cleared in software in the Interrupt Service Routine before re-enabling this interrupt. The INT interrupt can wake-up the processor from Sleep, if bit INTE was set prior to going into Sleep. The status of global interrupt enable bit GIE decides whether or not the processor branches to the interrupt vector following wake-up. See **Section 9.13** "**Power-down Mode** (**Sleep**)" for details on Sleep mode.

9.10.2 TMR0 INTERRUPT

An overflow (FFh \rightarrow 00h) in the TMR0 register will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>). (Section 4.0 "Timer0 Module")

9.10.3 PORTB INTCON CHANGE

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<4>). (Section 3.2 "PORTB and the TRISB Register")

9.11 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt, (i.e., W register and STATUS register). This will have to be implemented in software.

Example 9-1 stores and restores the W and STATUS registers. The register, W_TEMP, must be defined in each bank and must be defined at the same offset from the bank base address (i.e., if W_TEMP is defined at 0x20 in bank 0, it must also be defined at 0xA0 in bank 1).

The example:

- a) Stores the W register.
- b) Stores the STATUS register in bank 0.
- c) Stores the PCLATH register.
- d) Executes the Interrupt Service Routine code (User-generated).
- e) Restores the STATUS register (and bank select bit).
- f) Restores the W and PCLATH registers.

MOVWF	W TEMP	;Copy W to TEMP register, could be bank one or zero
SWAPF		;Swap status to be saved into W
CLRF	STATUS	; bank 0, regardless of current bank, Clears IRP,RP1,RP0
MOVWF	STATUS_TEMP	Save status to bank zero STATUS_TEMP register
MOVF	PCLATH, W	;Only required if using pages 1, 2 and/or 3
MOVWF	PCLATH_TEMP	;Save PCLATH into W
CLRF	PCLATH	;Page zero, regardless of current page
BCF	STATUS, IRP	Return to Bank 0
MOVF	FSR, W	;Copy FSR to W
MOVWF	FSR_TEMP	;Copy FSR from W to FSR_TEMP
:		
:(ISR)		
:		
MOVF	PCLATH_TEMP, W	;Restore PCLATH
MOVWF	PCLATH	;Move W into PCLATH
SWAPF	STATUS_TEMP,W	;Swap STATUS_TEMP register into W
		;(sets bank to original state)
MOVWF	STATUS	;Move W into STATUS register
SWAPF	W_TEMP,F	;Swap W_TEMP
SWAPF	W_TEMP,W	;Swap W_TEMP into W

EXAMPLE 9-1: SAVING STATUS, W, AND PCLATH REGISTERS IN RAM

9.12 Watchdog Timer (WDT)

The Watchdog Timer is as a free running, on-chip, RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device have been stopped, for example, by execution of a SLEEP instruction.

During normal operation, a WDT Time-out generates a device Reset (Watchdog Timer Reset). If the device is in Sleep mode, a WDT Time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The TO bit in the STATUS register will be cleared upon a Watchdog Timer Time-out.

The WDT can be permanently disabled by clearing Configuration bit WDTE (**Section 9.1 "Configuration Bits**").

WDT time-out period values may be found in the Electrical Specifications section under TwDT (parameter #31). Values for the WDT prescaler (actually a postscaler, but shared with the Timer0 prescaler) may be assigned using the OPTION_REG register.

Note: The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device Reset condition.

Note: When a CLRWDT instruction is executed and the prescaler is assigned to the WDT, the prescaler count will be cleared, but the prescaler assignment is not changed.

FIGURE 9-15: WATCHDOG TIMER BLOCK DIAGRAM



FIGURE 9-16: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bits 13:8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	(1)	_	BODEN ⁽¹⁾	CP1	CP0	PWRTE ⁽¹⁾	WDTE	FOSC1	FOSC0
81h	OPTION_REG	N/A	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer. **Note 1:** See Figure 9-1 for operation of these bits.

9.13 Power-down Mode (Sleep)

Power-Down mode is entered by executing a $\ensuremath{\mathtt{SLEEP}}$ instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the PD bit (STATUS<3>) is cleared, the TO (STATUS<4>) bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP instruction was executed (driving high, low, or high-impedance).

For lowest current consumption in this mode, place all I/O pins at either VDD or VSS, ensure no external circuitry is drawing current from the I/O pin, powerdown the A/D and the disable external clocks. Pull all I/ O pins, that are high-impedance inputs, high or low externally to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

The $\overline{\text{MCLR}}$ pin must be at a logic high level (VIHMC).

9.13.1 WAKE-UP FROM SLEEP

The device can wake up from Sleep through one of the following events:

- 1. External Reset input on $\overline{\text{MCLR}}$ pin.
- 2. Watchdog Timer Wake-up (if WDT was enabled).
- 3. Interrupt from INT pin, RB port change, or some peripheral interrupts.

External MCLR Reset will cause a device Reset. All other events are considered a continuation of program execution and cause a "wake-up". The TO and PD bits in the STATUS register can be used to determine the cause of device Reset. The PD bit, which is set on power-up, is cleared when SLEEP is invoked. The TO bit is cleared if a WDT Time-out occurred (and caused wake-up).

The following peripheral interrupts can wake the device from Sleep:

- 1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
- 2. CCP Capture mode interrupt.
- 3. Special Event Trigger (Timer1 in Asynchronous mode using an external clock).

Other peripherals cannot generate interrupts, since during Sleep, no on-chip clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

WAKE-UP USING INTERRUPTS 9.13.2

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

· If the interrupt occurs before the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the \overline{TO} bit will not be set and \overline{PD} bits will not be cleared.

• If the interrupt occurs during or after the execution of a SLEEP instruction, the device will immediately wake-up from Sleep. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the TO bit will be set and the \overline{PD} bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the PD bit. If the PD bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a **SLEEP** instruction.



4:

CLKOUT is not available in these osc modes, but shown here for timing reference.

9.14 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note:	Microchip	does	not	recommend	code	
	protecting windowed devices.					

ID Locations 9.15

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify. It is recommended that only the 4 Least Significant bits of the ID location are used.

For ROM devices, these values are submitted along with the ROM code.

9.16 In-Circuit Serial Programming™

PIC16CXXX microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

For complete details on serial programming, please refer to the In-Circuit Serial Programming[™] (ICSP[™]) Guide, (DS30277).

12.4.3 TIMING DIAGRAMS AND SPECIFICATIONS



TABLE 12-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Param	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions
No.							
1A	Fosc	External CLKIN Frequency	DC		4	MHz	RC and XT osc modes
		(Note 1)	DC	—	4	MHz	HS osc mode (-04)
			DC	—	20	MHz	HS osc mode (-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency	DC	_	4	MHz	RC osc mode
		(Note 1)	0.1	—	4	MHz	XT osc mode
			4	—	20	MHz	HS osc mode
			5	—	200	kHz	LP osc mode
1	Tosc	External CLKIN Period	250	—	—	ns	RC and XT osc modes
		(Note 1)	250	—	—	ns	HS osc mode (-04)
			50	—	—	ns	HS osc mode (-20)
			5	—	—	μs	LP osc mode
		Oscillator Period	250	_	—	ns	RC osc mode
		(Note 1)	250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (-04)
			50	—	250	ns	HS osc mode (-20)
			5	_	—	μs	LP osc mode
2	Тсү	Instruction Cycle Time (Note 1)	200		DC	ns	Tcy = 4/Fosc
3*	TosL,	External Clock in (OSC1) High or	100	_	—	ns	XT oscillator
	TosH	Low Time	2.5	—	—	μS	LP oscillator
			15		—	ns	HS oscillator
4*	TosR,	External Clock in (OSC1) Rise or	_	_	25	ns	XT oscillator
	TosF	Fall Time	—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin.

When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

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PIC16C712/716 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. Device Fi	<u>-XX X (XX XXX</u> requency Temperature Package Pattern Range Range	Examples: a) PIC16C716 – 04/P 301 = Commercial temp., PDIP package, 4 MHz, normal VDD limits, QTP pattern #301.
Device:	PIC16C712 ⁽¹⁾ , PIC16C712T ⁽²⁾ ;VDD range 4.0V to 5.5V PIC16LC712 ⁽¹⁾ , PIC16LC712T ⁽²⁾ ;VDD range 2.5V to 5.5V PIC16C716 ⁽¹⁾ , PIC16C716T ⁽²⁾ ;VDD range 4.0V to 5.5V PIC16LC716 ⁽¹⁾ , PIC16LC716T ⁽²⁾ ;VDD range 2.5V to 5.5V	 b) PIC16LC712 – 04I/SO = Industrial temp., SOIC package, 200 kHz, Extended VDD limits. c) PIC16C712 – 20I/P = Industrial temp., PDIP package, 20MHz, normal VDD limits.
Frequency Range:	04 = 4 MHz 20 = 20 MHz	Note 1: C = CMOS LC = Low Power CMOS 2: T = in tape and reel – SOIC, SSOP packages only
Temperature Range:	blank = 0°C to 70°C (Commercial) I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)	 LC extended temperature device is not offered. LC is not offered at 20 MHz
Package:	JW = Windowed CERDIP SO = SOIC P = PDIP SS = SSOP	
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	

* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type (including LC devices).

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

- 1. Your local Microchip sales office
- 2. The Microchip Worldwide Site (www.microchip.com)