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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	3.5КВ (2К х 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c716-04i-ss

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2.2.2.2 OPTION_REG Register

The OPTION_REG register is a readable and writable register, which contains various control bits to configure the TMR0 prescaler/WDT postscaler (single assignable register known also as the prescaler), the External INT Interrupt, TMR0 and the weak pull-ups on PORTB.

Note: To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer.

FIGURE 2-5: OPTION_REG REGISTER (ADDRESS 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1				
RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	R = Readable bit			
bit7							bit0	W = Writable bit			
								read as '0'			
								- n = Value at POR Reset			
bit 7:	RBPU: PORTB Pull-up Enable bit										
	1 = PORTB pull-ups are disabled										
		s puil-ups	are enac	nea by Ina	ividual port	latch valu	es				
bit 6:	INTEDG: In	nterrupt E	dge Sele		nin						
	1 = Interruption = 0 = Interruption	pt on fallin	ig edge of	f RB0/INT	pin						
bit 5:	TOCS: TM	R0 Clock \$	Source S	elect bit							
	1 = Transit	ion on RA	4/T0CKI	pin							
	0 = Interna	I instruction	on cycle o	clock (CLK	(OUT)						
bit 4:	TOSE: TMF	R0 Source	e Edge Se	elect bit							
	1 = Increm	ent on hig	h-to-low	transition	on RA4/T00	CKI pin					
h:+ 0.			v-to-nign								
DIT 3:	1 = Presca	ler is assi	aned to t	he WDT							
	0 = Presca	ler is assi	gned to t	he Timer0	module						
bit 2-0:	PS2:PS0 :	Prescaler	Rate Sel	ect bits							
	Bit Value	TMR0 Ra	ate WD1	Rate							
	000	1:2	1:	1							
	001	1:4	1:	2							
	010	1:8	1:	4 8							
	100	1:32	1:	16							
	101	1:64	1:	32							
	110 111	1:128	B 1:	64 128							
		1.200	5 1								

2.2.2.3 INTCON Register

The INTCON Register is a readable and writable register which contains various enable and flag bits for the TMR0 register overflow, RB Port change and External RB0/INT pin interrupts. **Note:** Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 2-6: INTCON REGISTER (ADDRESS 0Bh, 8Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x				
GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	R	= Readable bit		
bit7	·						bit0	W U -n	 Writable bit Unimplemented bit, read as '0' Value at POR Reset 		
bit 7:	GIE: Global Interrupt Enable bit 1 = Enables all unmasked interrupts 0 = Disables all interrupts										
bit 6:	PEIE: Per 1 = Enabl 0 = Disab	ripheral In les all unn les all per	terrupt En nasked pe ipheral int	able bit ripheral in errupts	terrupts						
bit 5:	TOIE : TMR0 Overflow Interrupt Enable bit 1 = Enables the TMR0 interrupt 0 = Disables the TMR0 interrupt										
bit 4:	IINTE: RE 1 = Enabl 0 = Disab	30/INT Ext les the RE les the RE	ternal Inte 80/INT exte 30/INT ext	rrupt Enab ernal interi ernal inter	le bit upt rupt						
bit 3:	RBIE : RB Port Change Interrupt Enable bit 1 = Enables the RB port change interrupt 0 = Disables the RB port change interrupt										
bit 2:	TOIF : TMI 1 = TMRC 0 = TMRC	R0 Overflo) register l) register o	ow Interrup has overflo did not ove	ot Flag bit owed (mus erflow	t be cleare	d in softwa	are)				
bit 1:	INTF : RB 1 = The R 0 = The R	0/INT Exte RB0/INT e RB0/INT e	ernal Inter xternal inter xternal inte	rupt Flag b errupt occu errupt did i	bit urred (must not occur	be cleare	d in softwa	re)			
bit 0:	RBIF : RB 1 = At lea 0 = None	Port Cha ist one of of the RB	nge Interr the RB7:R 7:RB4 pin	upt Flag bi B4 pins ch s have ch	t nanged stat anged state	e (must be	e cleared in	sof	tware)		

3.2 PORTB and the TRISB Register

PORTB is an 8-bit wide bidirectional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input, (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output, (i.e., put the contents of the output latch on the selected pin).

BCF	STATUS, RPO	;
CLRF	PORTB	; Initialize PORTB by
		; clearing output
		; data latches
BSF	STATUS, RPO	; Select Bank 1
MOVLW	0xCF	; Value used to
		; initialize data
		; direction
MOVWF	TRISB	; Set RB<3:0> as inputs
		; RB<5:4> as outputs
		; RB<7:6> as inputs

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTION_REG<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

FIGURE 3-3: BLOCK DIAGRAM OF RB0 PIN



NOTES:

6.0 TIMER2 MODULE

The Timer2 module timer has the following features:

- 8-bit timer (TMR2 register)
- 8-bit period register (PR2)
- Readable and writable (both registers)
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16)
- Interrupt on TMR2 match of PR2

Timer2 has a control register, shown in Figure 6-1. Timer2 can be shut off by clearing control bit TMR2ON (T2CON<2>) to minimize power consumption.

Figure 6-2 is a simplified block diagram of the Timer2 module.

Additional information on timer modules is available in the PIC[®] Mid-Range Reference Manual, (DS33023).

FIGURE 6-1: T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)



FIGURE 6-2: TIMER2 BLOCK DIAGRAM



6.1 Timer2 Operation

Timer2 can be used as the PWM time base for PWM mode of the CCP module.

The TMR2 register is readable and writable, and is cleared on any device Reset.

The input clock (Fosc/4) has a prescale option of 1:1, 1:4 or 1:16, selected by control bits T2CKPS1:T2CKPS0 (T2CON<1:0>).

The match output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling inclusive) to generate a TMR2 interrupt (latched in flag bit TMR2IF, (PIR1<1>)).

The prescaler and postscaler counters are cleared when any of the following occurs:

- a write to the TMR2 register
- a write to the T2CON register
- any device Reset (Power-on Reset, MCLR Reset, Watchdog Timer Reset, or Brown-out Reset)

TMR2 is not cleared when T2CON is written.

6.2 Timer2 Interrupt

The Timer2 module has an 8-bit period register PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon Reset.

TABLE 6-1: REGI	TERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER
-----------------	--

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Bh,8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	-	ADIF				CCP1IF	TMR2IF	TMR1IF	-00000	0000 -000
8Ch	PIE1	_	ADIE	_	_	_	CCP1IE	TMR2IE	TMR1IE	-0000	0000 -000
11h	TMR2	2 Timer2 Module's Register							0000 0000	0000 0000	
12h	T2CON	_	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
92h	PR2	R2 Timer2 Period Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, — = unimplemented read as '0'. Shaded cells are not used by the Timer2 module.

7.0 CAPTURE/COMPARE/PWM (CCP) MODULE(S)

Each CCP (Capture/Compare/PWM) module contains a 16-bit register, which can operate as a 16-bit capture register, as a 16-bit compare register or as a PWM master/slave Duty Cycle register. Table 7-1 shows the timer resources of the CCP module modes.

Capture/Compare/PWM Register 1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. All are readable and writable.

FIGURE 7-1: CCP1CON REGISTER (ADDRESS 17h)

U-0 U-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 DC1B1 DC1B0 CCP1M3 CCP1M2 CCP1M1 CCP1M0 R = Readable bit W = Writable bit bit7 bit0 U = Unimplemented bit, read as '0' -n = Value at POR Reset bit 7-6: Unimplemented: Read as '0' bit 5-4: DC1B1:DC1B0: PWM Least Significant bits Capture Mode: Unused Compare Mode: Unused PWM Mode: These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPR1L. bit 3-0: CCP1M3:CCP1M0: CCP1 Mode Select bits 0000 = Capture/Compare/PWM off (resets CCP1 module) 0100 = Capture mode, every falling edge 0101 = Capture mode, every rising edge 0110 = Capture mode, every 4th rising edge 0111 = Capture mode, every 16th rising edge 1000 = Compare mode, set output on match (CCP1IF bit is set) 1001 = Compare mode, clear output on match (CCP1IF bit is set) 1010 = Compare mode, generate software interrupt on match (CCP1IF bit is set, CCP1 pin is unaffected) 1011 = Compare mode, trigger special event (CCP1IF bit is set; CCP1 resets TMR1 and starts an A/D conversion (if A/D module is enabled)) 11xx = PWM mode

FIGURE 7-2: TRISCCP REGISTER (ADDRESS 87H)



Additional information on the CCP module is available in the PIC[®] Mid-Range Reference Manual, (DS33023).

TABLE 7-1:CCP MODE – TIMER
RESOURCE

Timer Resource						
Timer1						
Timer1						
Timer2						

7.1 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin RB3/CCP1. An event is defined as:

- every falling edge
- every rising edge
- every 4th rising edge
- every 16th rising edge

An event is selected by control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit CCP1IF (PIR1<2>) is set. It must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value will be lost.

FIGURE 7-3:

CAPTURE MODE OPERATION BLOCK DIAGRAM



7.1.1 CCP PIN CONFIGURATION

In Capture mode, the CCP output must be disabled by setting the TRISCCP<2> bit.

Note: If the RB3/CCP1 is configured as an output by clearing the TRISCCP<2> bit, a write to the DCCP bit can cause a capture condition.

7.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

7.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep bit CCP1IE (PIE1<2>) clear to avoid false interrupts and should clear the flag bit CCP1IF following any such change in Operating mode.

7.1.4 CCP PRESCALER

There are four prescaler settings, specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. This means that any Reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore the first capture may be from a non-zero prescaler. Example 7-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

EXAMPLE 7-1: CHANGING BETWEEN CAPTURE PRESCALERS

CLRF	CCP1CON	;Turn CCP module off
MOVLW	NEW_CAPT_PS	;Load the W reg with
		; the new prescaler
		; mode value and CCP ON
MOVWF	CCP1CON	;Load CCP1CON with this
		; value

9.2 Oscillator Configurations

9.2.1 OSCILLATOR TYPES

The PIC16CXXX can be operated in four different Oscillator modes. The user can program two Configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low-Power Crystal
- XT Crystal/Resonator
- HS High-Speed Crystal/Resonator
- RC Resistor/Capacitor

9.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 9-2). The PIC16CXXX oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1/ CLKIN pin (Figure 9-3).

FIGURE 9-2:	CRYSTAL/CERAMIC
	RESONATOR OPERATION
	(HS, XT OR LP
	OSC CONFIGURATION)



FIGURE 9-3: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC



TABLE 9-1: CERAMIC RESONATORS

Ranges Tested:

- J -	5							
Mode	Freq	OSC1	OSC2					
XT	455 kHz	68-100 pF	68-100 pF					
	2.0 MHz	15-68 pF	15-68 pF					
	4.0 MHz	15-68 pF	15-68 pF					
HS	8.0 MHz	10-68 pF	10-68 pF					
	16.0 MHz	10-22 pF	10-22 pF					
These values are for design guidance only. See								
notes at bottom of page.								

TABLE 9-2:CAPACITOR SELECTION FOR
CRYSTAL OSCILLATOR

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2	
LP	32 kHz	33 pF	33 pF	
	200 kHz	15 pF	15 pF	
XT	200 kHz	47-68 pF	47-68 pF	
	1 MHz	15 pF	15 pF	
	4 MHz	15 pF	15 pF	
HS	4 MHz	15 pF	15 pF	
	8 MHz	15-33 pF	15-33 pF	
	20 MHz	15-33 pF	15-33 pF	
These values are for design guidance only. See notes at bottom of page.				

Note 1:	Recommended values of C1 and C2 are
	identical to the ranges tested (Table 9-1).

- 2: Higher capacitance increases the stability of the oscillator, but also increases the start-up time.
- 3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
- 4: Rs may be required in HS mode, as well as XT mode to avoid overdriving crystals with low drive level specification.

PIC16C712/716



FIGURE 9-12: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 1



FIGURE 9-13: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2



9.10 Interrupts

The PIC16C712/716 devices have up to 7 sources of interrupt. The Interrupt Control Register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

Note:	Individual interrupt flag bits are set regard-		
	less of the status of their corresponding		
	mask bit or the GIE bit.		

A Global Interrupt Enable bit, GIE (INTCON<7>) enables (if set) all unmasked interrupts or disables (if cleared) all interrupts. When bit GIE is enabled, and an interrupt's flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in various registers. Individual interrupt bits are set, regardless of the status of the GIE bit. The GIE bit is cleared on Reset.

The "return from interrupt" instruction, RETFIE, exits the interrupt routine, as well as sets the GIE bit, which re-enables interrupts.

The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

The peripheral interrupt flags are contained in the Special Function Registers, PIR1 and PIR2. The corresponding interrupt enable bits are contained in Special Function Registers, PIE1 and PIE2, and the peripheral interrupt enable bit is contained in Special Function Register, INTCON.

When an interrupt is responded to, the GIE bit is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends when the interrupt event occurs. The latency is the same for one or two cycle instructions. Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.



FIGURE 9-14: INTERRUPT LOGIC

9.13 Power-down Mode (Sleep)

Power-Down mode is entered by executing a $\ensuremath{\mathtt{SLEEP}}$ instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the PD bit (STATUS<3>) is cleared, the TO (STATUS<4>) bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP instruction was executed (driving high, low, or high-impedance).

For lowest current consumption in this mode, place all I/O pins at either VDD or VSS, ensure no external circuitry is drawing current from the I/O pin, powerdown the A/D and the disable external clocks. Pull all I/ O pins, that are high-impedance inputs, high or low externally to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

The $\overline{\text{MCLR}}$ pin must be at a logic high level (VIHMC).

9.13.1 WAKE-UP FROM SLEEP

The device can wake up from Sleep through one of the following events:

- 1. External Reset input on $\overline{\text{MCLR}}$ pin.
- 2. Watchdog Timer Wake-up (if WDT was enabled).
- 3. Interrupt from INT pin, RB port change, or some peripheral interrupts.

External MCLR Reset will cause a device Reset. All other events are considered a continuation of program execution and cause a "wake-up". The TO and PD bits in the STATUS register can be used to determine the cause of device Reset. The PD bit, which is set on power-up, is cleared when SLEEP is invoked. The TO bit is cleared if a WDT Time-out occurred (and caused wake-up).

The following peripheral interrupts can wake the device from Sleep:

- 1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
- 2. CCP Capture mode interrupt.
- 3. Special Event Trigger (Timer1 in Asynchronous mode using an external clock).

Other peripherals cannot generate interrupts, since during Sleep, no on-chip clocks are present.

9.16 In-Circuit Serial Programming™

PIC16CXXX microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

For complete details on serial programming, please refer to the In-Circuit Serial Programming[™] (ICSP[™]) Guide, (DS30277).

11.11 PICSTART Plus Development Programmer

The PICSTART Plus Development Programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus Development Programmer supports most PIC devices in DIP packages up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus Development Programmer is CE compliant.

11.12 Demonstration, Development and Evaluation Boards

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM[™] and dsPICDEM[™] demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ[®] security ICs, CAN, IrDA[®], PowerSmart[®] battery management, SEEVAL[®] evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Check the Microchip web page (www.microchip.com) and the latest *"Product Selector Guide"* (DS00148) for the complete list of demonstration, development and evaluation kits.

13.2 Package Details

The following sections give the technical details of the packages.

18-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Notes: Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

.008

.045

.014

.310

5

5

.012

.058

.018

.370

10

10

.015

.070

.022

.430

15

15

0.20

1.14

0.36

7.87

5

5

0.29

1.46

0.46

9.40

10

10

0.38

1.78

0.56

10.92

15

15

С

B1

В

eВ

α

β

δ

JEDEC Equivalent: MS-001

Drawing No. C04-007

Lead Thickness

Upper Lead Width

Lower Lead Width

Overall Row Spacing

Mold Draft Angle Top

Mold Draft Angle Bottom

* Controlling Parameter § Significant Characteristic

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PIC16C712/716 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. Device Fi	<u>-XX X (XX XXX</u> requency Temperature Package Pattern Range Range	Examples: a) PIC16C716 – 04/P 301 = Commercial temp., PDIP package, 4 MHz, normal VDD limits, QTP pattern #301.	
Device:	PIC16C712 ⁽¹⁾ , PIC16C712T ⁽²⁾ ;VDD range 4.0V to 5.5V PIC16LC712 ⁽¹⁾ , PIC16LC712T ⁽²⁾ ;VDD range 2.5V to 5.5V PIC16C716 ⁽¹⁾ , PIC16C716T ⁽²⁾ ;VDD range 4.0V to 5.5V PIC16LC716 ⁽¹⁾ , PIC16LC716T ⁽²⁾ ;VDD range 2.5V to 5.5V	 b) PIC16LC712 – 04I/SO = Industrial temp., SOIC package, 200 kHz, Extended VDD limits. c) PIC16C712 – 20I/P = Industrial temp., PDIP package, 20MHz, normal VDD limits. 	
Frequency Range:	04 = 4 MHz 20 = 20 MHz	Note 1: C = CMOS LC = Low Power CMOS 2: T = in tape and reel – SOIC, SSOP packages only	
Temperature Range:	blank = 0°C to 70°C (Commercial) I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)	 LC extended temperature device is not offered. LC is not offered at 20 MHz 	
Package:	JW = Windowed CERDIP SO = SOIC P = PDIP SS = SSOP		
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)		

* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type (including LC devices).

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

- 1. Your local Microchip sales office
- 2. The Microchip Worldwide Site (www.microchip.com)

NOTES:

Worldwide Sales and Service

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