



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c716-20-ss

Table of Contents

1.0	Device Overview	5
2.0	Memory Organization	9
3.0	I/O Ports	21
4.0	Timer0 Module	29
5.0	Timer1 Module	31
6.0	Timer2 Module	36
7.0	Capture/Compare/PWM (CCP) Module(s)	39
8.0	Analog-to-Digital Converter (A/D) Module	45
9.0	Special Features of the CPU	51
10.0	Instruction Set Summary	67
11.0	Development Support	69
12.0	Electrical Characteristics	73
13.0	Packaging Information	89
	Revision History	95
	Conversion Considerations	95
	Migration from Base-line to Mid-Range Devices	95
	Index	97
	On-Line Support	101
	Reader Response	102
	PIC16C712/716 Product Identification System	103

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at docerrors@microchip.com or fax the **Reader Response Form** in the back of this data sheet to (480) 792-4150. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

<http://www.microchip.com>

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000A is version A of document DS30000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; <http://www.microchip.com>
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our web site at www.microchip.com to receive the most current information on all of our products.

PIC16C712/716

TABLE 1-1: PIC16C712/716 PINOUT DESCRIPTION

Pin Name	PIC16C712/716		Pin Type	Buffer Type	Description
	DIP, SOIC	SSOP			
MCLR/VPP MCLR VPP	4	4	I P	ST	Master clear (Reset) input. This pin is an active low Reset to the device. Programming voltage input
OSC1/CLKIN OSC1 CLKIN	16	18	I I	ST CMOS	Oscillator crystal input or external clock source input. ST buffer when configured in RC mode. CMOS otherwise. External clock source input.
OSC2/CLKOUT OSC2 CLKOUT	15	17	O O	— —	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
RA0/AN0 RA0 AN0	17	19	I/O I	TTL Analog	PORTA is a bidirectional I/O port. Digital I/O Analog input 0
RA1/AN1 RA1 AN1	18	20	I/O I	TTL Analog	Digital I/O Analog input 1
RA2/AN2 RA2 AN2	1	1	I/O I	TTL Analog	Digital I/O Analog input 2
RA3/AN3/VREF RA3 AN3 VREF	2	2	I/O I I	TTL Analog Analog	Digital I/O Analog input 3 A/D Reference Voltage input.
RA4/T0CKI RA4 T0CKI	3	3	I/O I	ST/OD ST	Digital I/O. Open drain when configured as output. Timer0 external clock input

Legend: TTL = TTL-compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
OD = Open drain output
SM = SMBus compatible input. An external resistor is required if this pin is used as an output
NPU = N-channel pull-up PU = Weak internal pull-up
No-P diode = No P-diode to VDD AN = Analog input or output
I = input O = output
P = Power L = LCD Driver

2.0 MEMORY ORGANIZATION

There are two memory blocks in each of these PIC[®] microcontroller devices. Each block (Program Memory and Data Memory) has its own bus so that concurrent access can occur.

Additional information on device memory may be found in the PIC[®] Mid-Range Reference Manual, (DS33023).

2.1 Program Memory Organization

The PIC16C712/716 has a 13-bit Program Counter (PC) capable of addressing an 8K x 14 program memory space. PIC16C712 has 1K x 14 words of program memory and PIC16C716 has 2K x 14 words of program memory. Accessing a location above the physically implemented address will cause a wraparound.

The Reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK OF THE PIC16C712

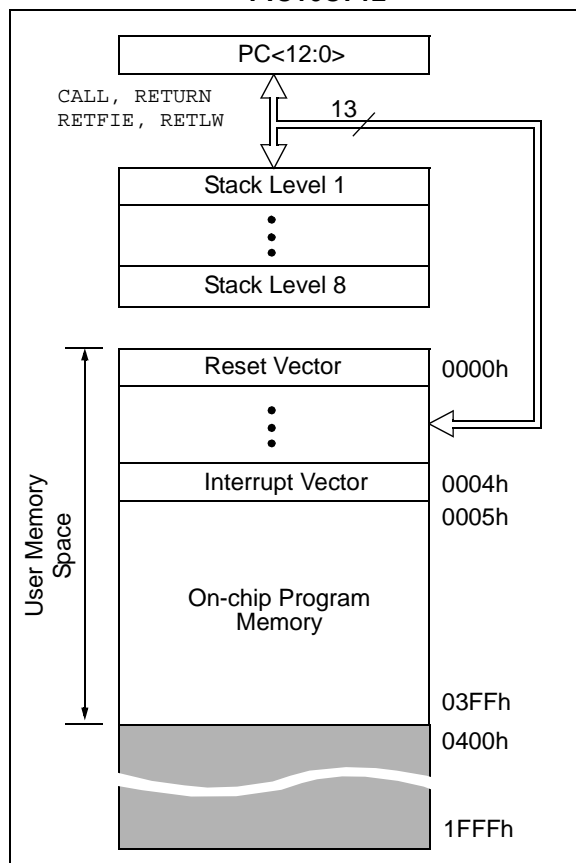
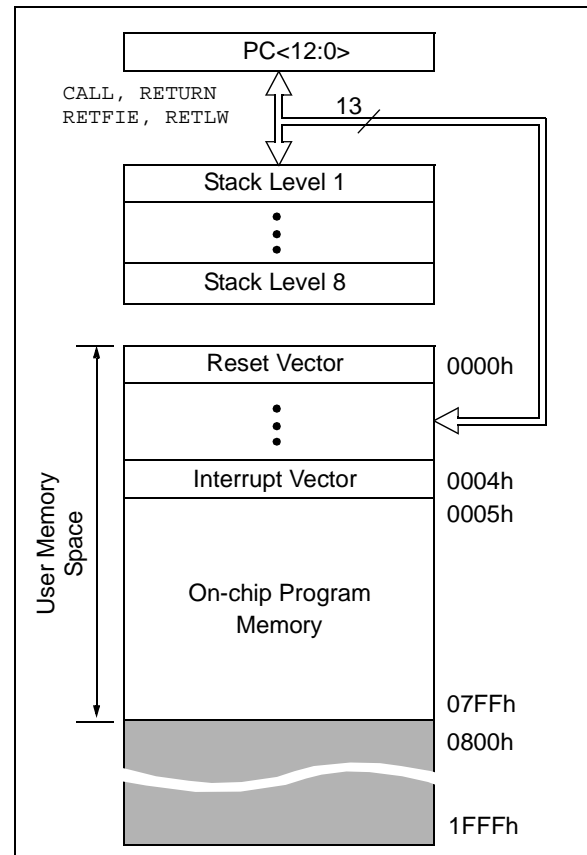


FIGURE 2-2: PROGRAM MEMORY MAP AND STACK OF PIC16C716



2.2.2.5 PIR1 Register

This register contains the individual flag bits for the peripheral interrupts.

Note: Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 2-8: PIR1 REGISTER (ADDRESS 0Ch)

U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	ADIF	—	—	—	CCP1IF	TMR2IF	TMR1IF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
-n = Value at POR Reset

bit 7: **Unimplemented:** Read as '0'

bit 6: **ADIF:** A/D Converter Interrupt Flag bit
1 = An A/D conversion completed (must be cleared in software)
0 = The A/D conversion is not complete

bit 5-3: **Unimplemented:** Read as '0'

bit 2: **CCP1IF:** CCP1 Interrupt Flag bit
Capture Mode:
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare Mode:
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM Mode:
Unused in this mode

bit 1: **TMR2IF:** TMR2 to PR2 Match Interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 to PR2 match occurred

bit 0: **TMR1IF:** TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflowed (must be cleared in software)
0 = TMR1 register did not overflow

PIC16C712/716

2.2.2.6 PCON Register

The Power Control (PCON) register contains a flag bit to allow differentiation between a Power-on Reset (POR) to an external $\overline{\text{MCLR}}$ Reset or WDT Reset. These devices contain an additional bit to differentiate a Brown-out Reset condition from a Power-on Reset condition.

Note: If the BODEN Configuration bit is set, $\overline{\text{BOR}}$ is '1' on Power-on Reset. If the BODEN Configuration bit is clear, $\overline{\text{BOR}}$ is unknown on Power-on Reset.

The $\overline{\text{BOR}}$ Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (the BODEN Configuration bit is clear). $\overline{\text{BOR}}$ must then be set by the user and checked on subsequent resets to see if it is clear, indicating a brown-out has occurred.

FIGURE 2-9: PCON REGISTER (ADDRESS 8Eh)

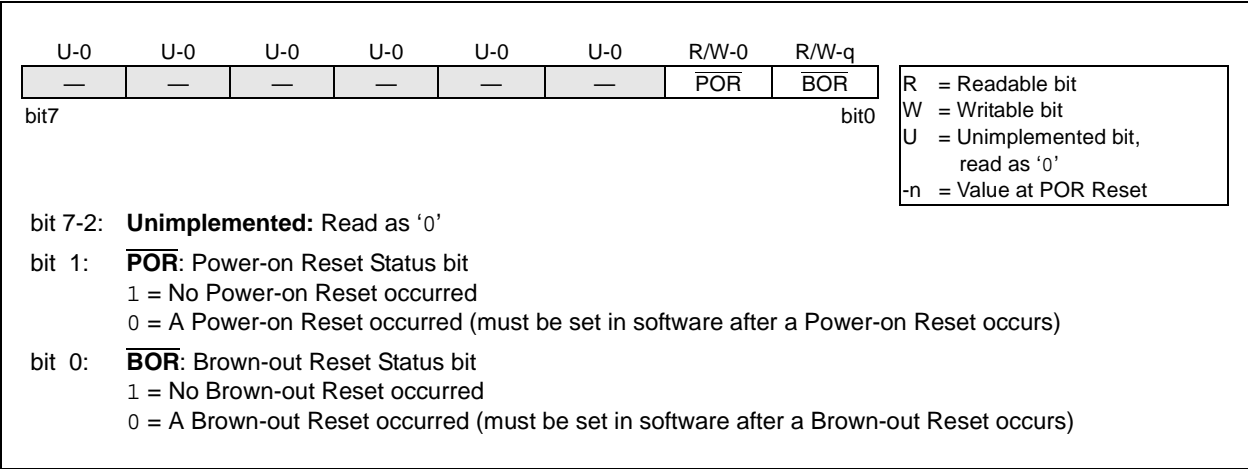


TABLE 3-1: PORTA FUNCTIONS

Name	Bit#	Buffer	Function
RA0/AN0	bit 0	TTL	Input/output or analog input
RA1/AN1	bit 1	TTL	Input/output or analog input
RA2/AN2	bit 2	TTL	Input/output or analog input
RA3/AN3/VREF	bit 3	TTL	Input/output or analog input or VREF
RA4/T0CKI	bit 4	ST	Input/output or external clock input for Timer0 Output is open drain type

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
05h	PORTA	—	—	— ⁽¹⁾	RA4	RA3	RA2	RA1	RA0	--xx xxxx	--xu uuuu
85h	TRISA	—	—	— ⁽¹⁾	PORTA Data Direction Register					--11 1111	--11 1111
9Fh	ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0	---- -000	---- -000

Legend: x = unknown, u = unchanged, — = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

Note 1: Reserved bits; Do Not Use.

PORTB pins RB3:RB1 are multiplexed with several peripheral functions (Table 3-3). PORTB pins RB3:RB0 have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTB pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify-write instructions (BSF, BCF, XORWF) with TRISB as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

Four of PORTB's pins, RB7:RB4, have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt-on-change comparison). The input pins, RB7:RB4, are compared with the old value latched on the last read of

PORTB. The “mismatch” outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

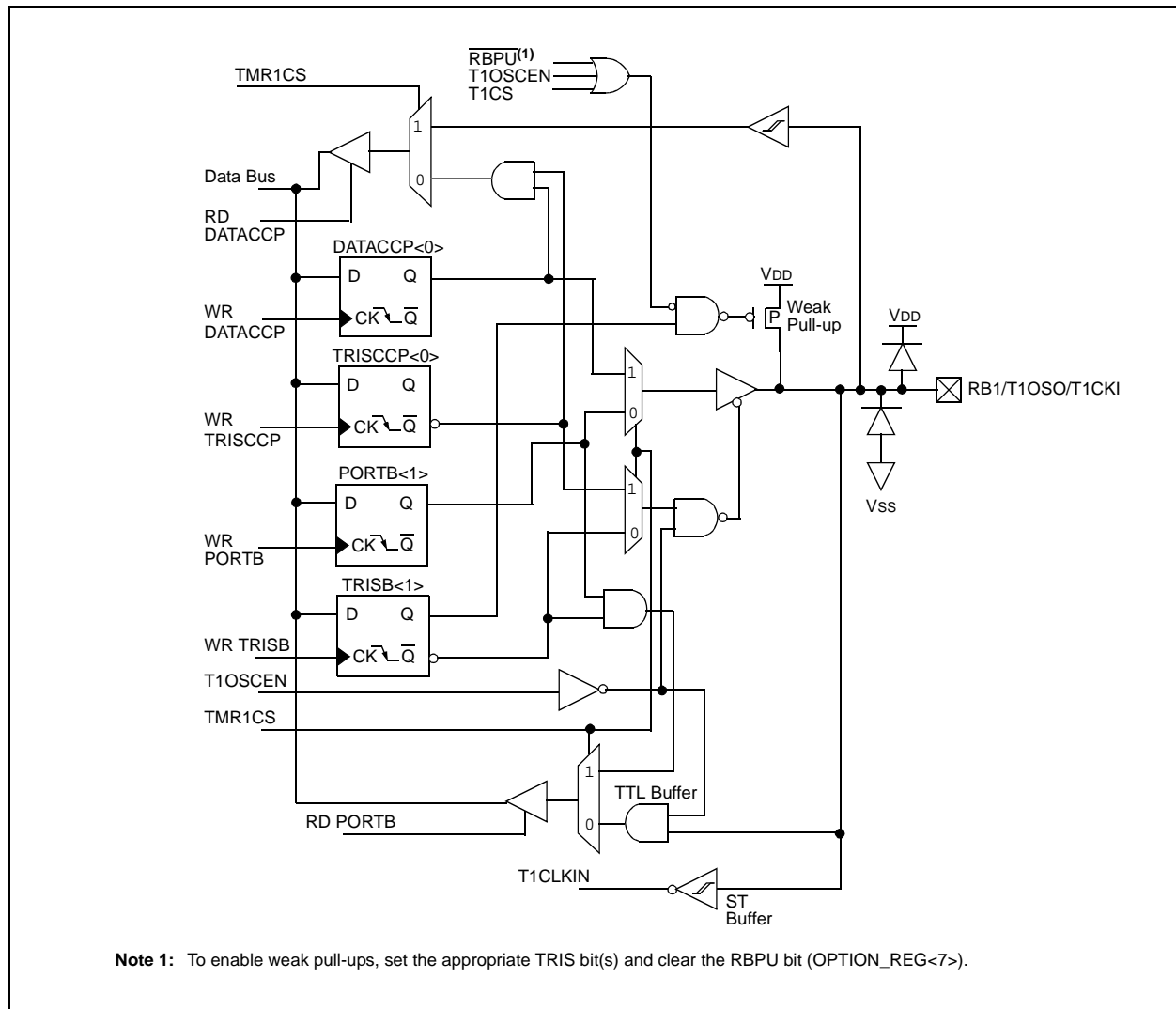
This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- Any read or write of PORTB will end the mismatch condition.
- Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

FIGURE 3-4: BLOCK DIAGRAM OF RB1/T1OSO/T1CKI PIN



PIC16C712/716

FIGURE 3-5: BLOCK DIAGRAM OF RB2/T1OSI PIN

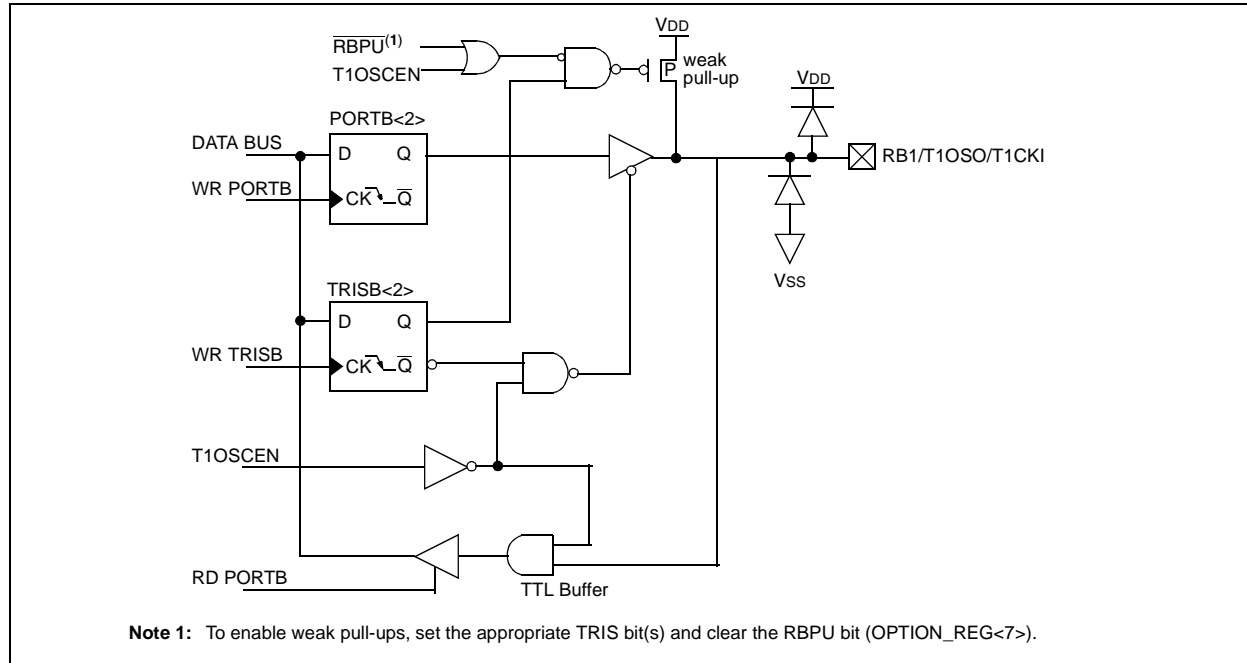


FIGURE 3-6: BLOCK DIAGRAM OF RB3/CCP1 PIN

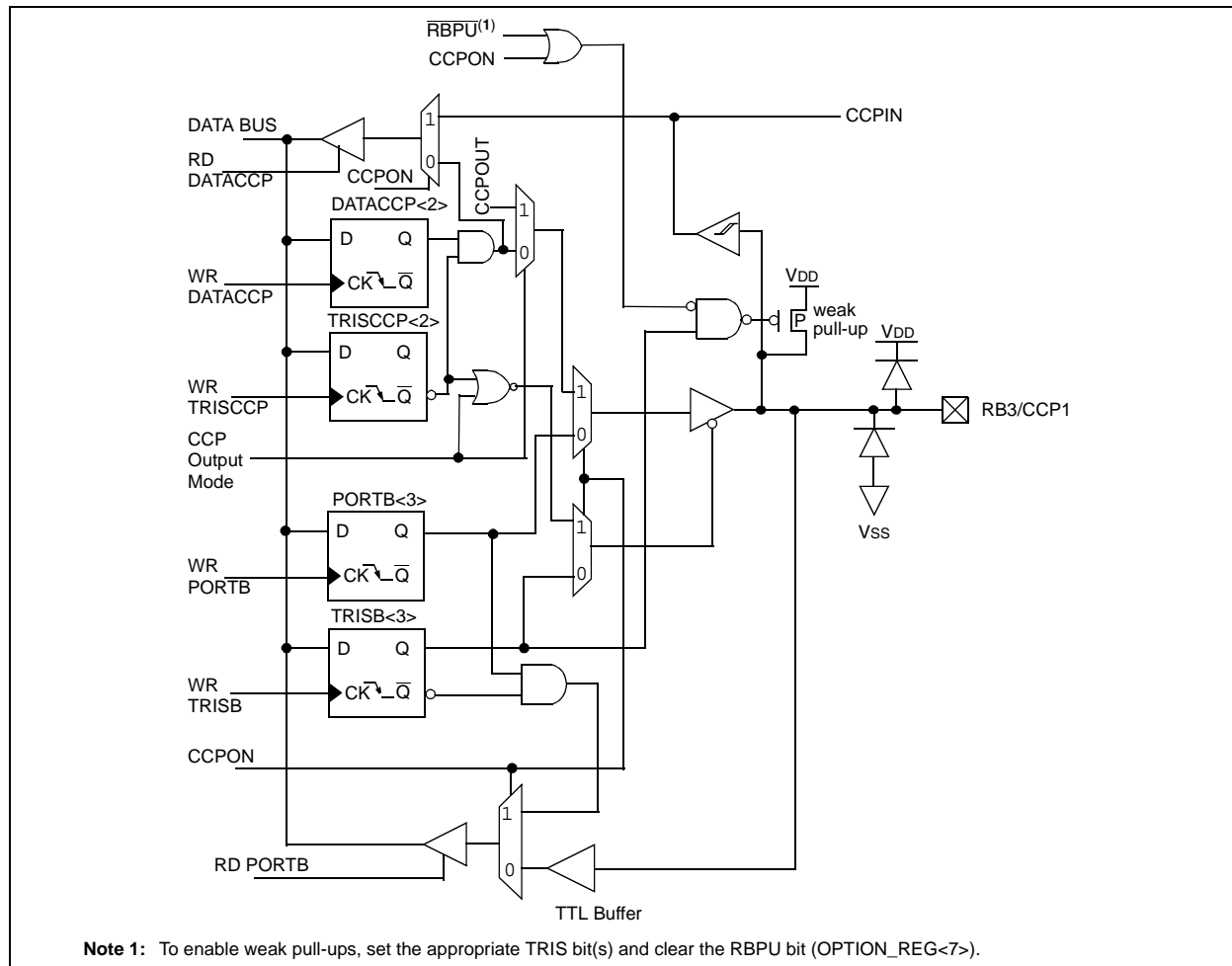


TABLE 5-1: TMR1 MODULE AND PORTB OPERATION

TMR1 Module Mode	Clock Source	Control Bits	TMR1 Module Operation	PORTB<2:1> Operation
Off	N/A	T1CON = --xx 0x00	Off	PORTB<2:1> function as normal I/O
Timer	Fosc/4	T1CON = --xx 0x01	TMR1 module uses the main oscillator as clock source. TMR1ON can turn on or turn off Timer1.	PORTB<2:1> function as normal I/O
Counter	External circuit	T1CON = --xx 0x11 TR1SCCP = ---- -x-1	TMR1 module uses the external signal on the RB1/T1OSO/T1CKI pin as a clock source. TMR1ON can turn on or turn off Timer1. DT1CK can read the signal on the RB1/T1OSO/T1CKI pin.	PORTB<2> functions as normal I/O. PORTB<1> always reads '0' when configured as input. If PORTB<1> is configured as output, reading PORTB<1> will read the data latch. Writing to PORTB<1> will always store the result in the data latch, but not to the RB1/T1OSO/T1CKI pin. If the TMR1CS bit is cleared (TMR1 reverts to the timer mode), then pin PORTB<1> will be driven with the value in the data latch.
	Firmware	T1CON = --xx 0x11 TR1SCCP = ---- -x-0	DATAACP<0> bit drives RB1/T1OSO/T1CKI and produces the TMR1 clock source. TMR1ON can turn on or turn off Timer1. The DATAACP<0> bit, DT1CK, can read and write to the RB1/T1OSO/T1CKI pin.	
	Timer1 oscillator	T1CON = --xx 1x11	RB1/T1OSO/T1CKI and RB2/T1OSI are configured as a 2 pin crystal oscillator. RB1/T1OSI/T1CKI is the clock input for TMR1. TMR1ON can turn on or turn off Timer1. DATAACP<1> bit, DT1CK, always reads '0' as input and can not write to the RB1/T1OSO/T1CKI pin.	PORTB<2:1> always read '0' when configured as inputs. If PORTB<2:1> are configured as outputs, reading PORTB<2:1> will read the data latches. Writing to PORTB<2:1> will always store the result in the data latches, but not to the RB2/T1OSI and RB1/T1OSO/T1CKI pins. If the TMR1CS and T1OSCEN bits are cleared (TMR1 reverts to the timer mode and TMR1 oscillator is disabled), then pin PORTB<2:1> will be driven with the value in the data latches.

7.0 CAPTURE/COMPARE/PWM (CCP) MODULE(S)

Each CCP (Capture/Compare/PWM) module contains a 16-bit register, which can operate as a 16-bit capture register, as a 16-bit compare register or as a PWM master/slave Duty Cycle register. Table 7-1 shows the timer resources of the CCP module modes.

Capture/Compare/PWM Register 1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. All are readable and writable.

Additional information on the CCP module is available in the PIC® Mid-Range Reference Manual, (DS33023).

TABLE 7-1: CCP MODE – TIMER RESOURCE

CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

FIGURE 7-1: CCP1CON REGISTER (ADDRESS 17h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
-n = Value at POR Reset

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **DC1B1:DC1B0:** PWM Least Significant bits
Capture Mode: Unused
Compare Mode: Unused
PWM Mode: These bits are the two LSBs of the PWM duty cycle. The eight MSBs are found in CCPR1L.

bit 3-0: **CCP1M3:CCP1M0:** CCP1 Mode Select bits
0000 = Capture/Compare/PWM off (resets CCP1 module)
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode, set output on match (CCP1IF bit is set)
1001 = Compare mode, clear output on match (CCP1IF bit is set)
1010 = Compare mode, generate software interrupt on match (CCP1IF bit is set, CCP1 pin is unaffected)
1011 = Compare mode, trigger special event (CCP1IF bit is set; CCP1 resets TMR1 and starts an A/D conversion (if A/D module is enabled))
11xx = PWM mode

FIGURE 7-2: TRISCCP REGISTER (ADDRESS 87H)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	—	—	TCCP	—	TT1CK
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
-n = Value at POR Reset

bit 7-3: **Reserved bits; Do Not Use**

bit 2: **TCCP – Tri-state control bit for CCP**
0 = Output pin driven
1 = Output pin tristated

bit 1: **Reserved bit; Do Not Use**

bit 0: **TT1CK – Tri-state control bit for T1CKI pin**
0 = T1CKI pin is an output
1 = T1CKI pin is an input

PIC16C712/716

7.3 PWM Mode

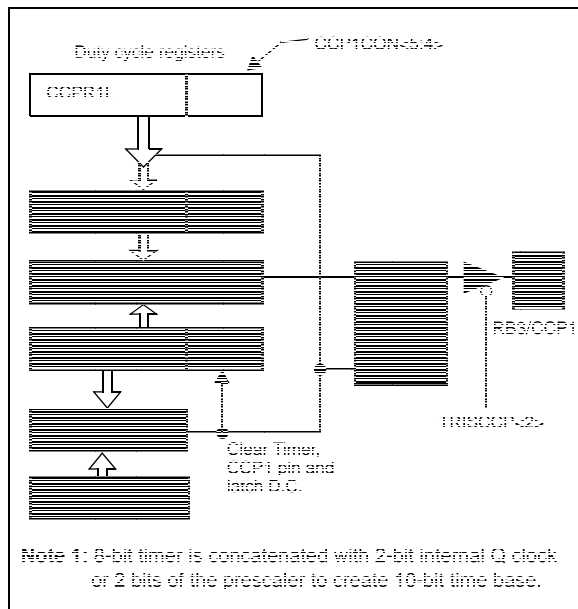
In Pulse Width Modulation (PWM) mode, the CCP1 pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTB data latch, the TRISCCP<2> bit must be cleared to make the CCP1 pin an output.

Note: Clearing the CCP1CON register will force the CCP1 PWM output latch to the default low level. This is neither the PORTB I/O data latch nor the DATAACP latch.

Figure 7-5 shows a simplified block diagram of the CCP module in PWM mode.

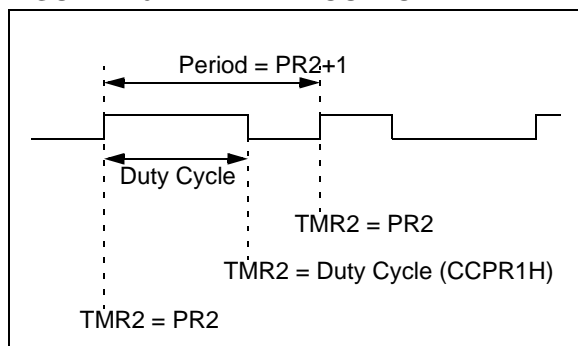
For a step by step procedure on how to set up the CCP module for PWM operation, see **Section 7.3.3 “Set-Up for PWM Operation”**.

FIGURE 7-5: SIMPLIFIED PWM BLOCK DIAGRAM



A PWM output (Figure 7-6) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 7-6: PWM OUTPUT



7.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

$$\text{PWM period} = [(PR2) + 1] \cdot 4 \cdot T_{osc} \cdot (\text{TMR2 prescale value})$$

PWM frequency is defined as $1 / [\text{PWM period}]$.

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note: The Timer2 postscaler (see **Section 6.0 “Timer2 Module”**) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

7.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSBs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

$$\text{PWM duty cycle} = (\text{CCPR1L:CCP1CON<5:4>}) \cdot T_{osc} \cdot (\text{TMR2 prescale value})$$

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2 concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

Maximum PWM resolution (bits) for a given PWM frequency:

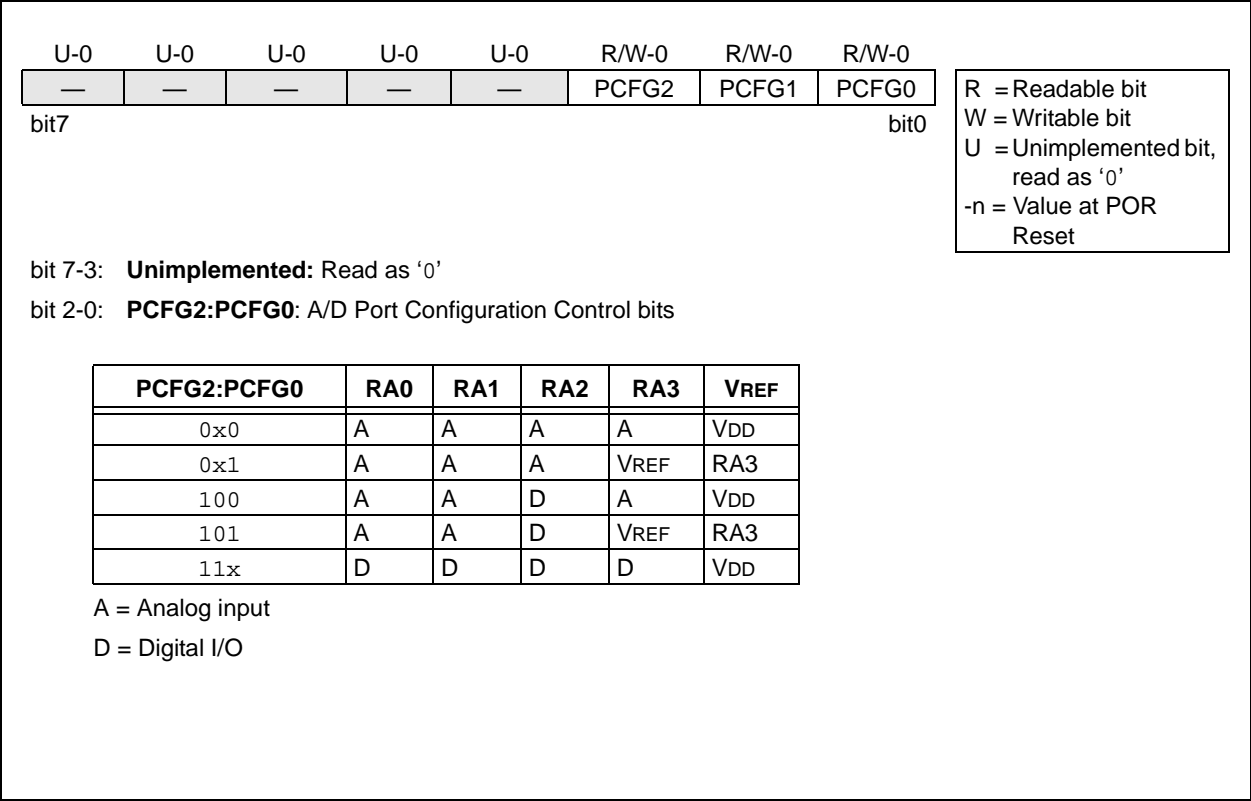
$$= \frac{\log\left(\frac{F_{osc}}{F_{PWM}}\right)}{\log(2)} \text{ bits}$$

Note: If the PWM duty cycle value is longer than the PWM period the CCP1 pin will not be cleared.

For an example PWM period and duty cycle calculation, see the PIC® Mid-Range Reference Manual, (DS33023).

PIC16C712/716

FIGURE 8-2: ADCON1 REGISTER (ADDRESS 9Fh)



PIC16C712/716

9.9 Power Control/Status Register (PCON)

The Power Control/Status Register, PCON has two bits.

Bit 0 is Brown-out Reset Status bit, $\overline{\text{BOR}}$. If the BODEN Configuration bit is set, $\overline{\text{BOR}}$ is '1' on Power-on Reset. If the BODEN Configuration bit is clear, $\overline{\text{BOR}}$ is unknown on Power-on Reset.

The $\overline{\text{BOR}}$ Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (the BODEN Configuration bit is clear). $\overline{\text{BOR}}$ must then be set by the user and checked on subsequent Resets to see if it is clear, indicating a brown-out has occurred.

Bit 1 is $\overline{\text{POR}}$ (Power-on Reset Status bit). It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

TABLE 9-3: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out	Wake-up from Sleep
	$\overline{\text{PWRTE}} = 0$	$\overline{\text{PWRTE}} = 1$		
XT, HS, LP	72 ms + 1024Tosc	1024Tosc	72 ms + 1024Tosc	1024Tosc
RC	72 ms	—	72 ms	—

TABLE 9-4: STATUS BITS AND THEIR SIGNIFICANCE

$\overline{\text{POR}}$	$\overline{\text{BOR}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	
0	x	1	1	Power-on Reset
0	x	0	x	Illegal, $\overline{\text{TO}}$ is set on $\overline{\text{POR}}$
0	x	x	0	Illegal, $\overline{\text{PD}}$ is set on $\overline{\text{POR}}$
1	0	1	1	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	$\overline{\text{MCLR}}$ Reset during normal operation
1	1	1	0	$\overline{\text{MCLR}}$ Reset during Sleep or interrupt wake-up from Sleep

TABLE 9-5: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---- --0x
$\overline{\text{MCLR}}$ Reset during normal operation	000h	000u uuuu	---- --uu
$\overline{\text{MCLR}}$ Reset during Sleep	000h	0001 0uuu	---- --uu
WDT Reset	000h	0000 1uuu	---- --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu
Brown-out Reset	000h	0001 1uuu	---- --u0
Interrupt wake-up from Sleep	PC + 1 ⁽¹⁾	uuu1 0uuu	---- --uu

Legend: u = unchanged, x = unknown, — = unimplemented bit read as '0'.

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

9.10 Interrupts

The PIC16C712/716 devices have up to 7 sources of interrupt. The Interrupt Control Register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

Note: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

A Global Interrupt Enable bit, GIE (INTCON<7>) enables (if set) all unmasked interrupts or disables (if cleared) all interrupts. When bit GIE is enabled, and an interrupt's flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in various registers. Individual interrupt bits are set, regardless of the status of the GIE bit. The GIE bit is cleared on Reset.

The "return from interrupt" instruction, `RETFIE`, exits the interrupt routine, as well as sets the GIE bit, which re-enables interrupts.

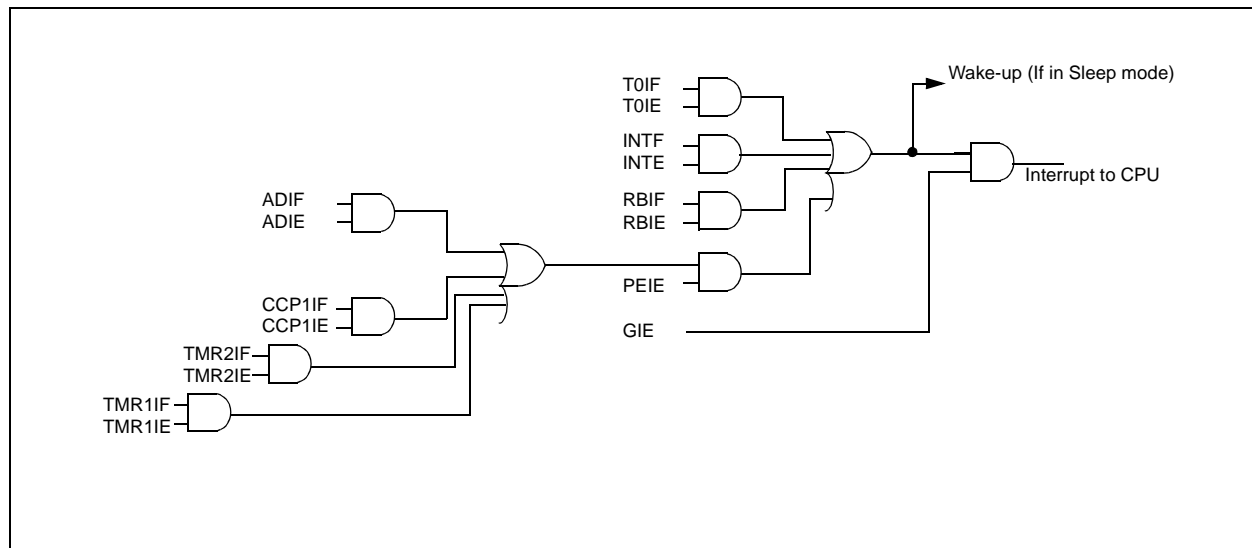
The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

The peripheral interrupt flags are contained in the Special Function Registers, PIR1 and PIR2. The corresponding interrupt enable bits are contained in Special Function Registers, PIE1 and PIE2, and the peripheral interrupt enable bit is contained in Special Function Register, INTCON.

When an interrupt is responded to, the GIE bit is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends when the interrupt event occurs. The latency is the same for one or two cycle instructions. Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

FIGURE 9-14: INTERRUPT LOGIC



12.1 DC Characteristics: PIC16C712/716-04 (Commercial, Industrial, Extended) PIC16C712/716-20 (Commercial, Industrial, Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature		0°C ≤ TA ≤ +70°C	for commercial	
					-40°C ≤ TA ≤ +85°C	for industrial	
					-40°C ≤ TA ≤ +125°C	for extended	
Param No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
D001 D001A	VDD	Supply Voltage	4.0 4.5 VBOR*	— — —	5.5 5.5 5.5	V V V	XT, RC and LP osc mode HS osc mode BOR enabled ⁽⁷⁾
D002*	VDR	RAM Data Retention Voltage ⁽¹⁾	—	1.5	—	V	
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004* D004A*	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05 TBD	— —	— —	V/ms	PWRT enabled (PWRT $\overline{\text{E}}$ bit clear) PWRT disabled (PWRT $\overline{\text{E}}$ bit set) See section on Power-on Reset for details
D005	VBOR	Brown-out Reset voltage trip point	3.65	—	4.35	V	BODEN bit set
D010 D013	IDD	Supply Current ^(2,5)	— —	0.8 4.0	2.5 8.0	mA mA	FOSC = 4 MHz, VDD = 4.0V FOSC = 20 MHz, VDD = 4.0V
D020 D021 D021B	IPD	Power-down Current ^(3,5)	— — — —	10.5 1.5 1.5 2.5	42 16 19 19	μA μA μA μA	VDD = 4.0V, WDT enabled, -40°C to +85°C VDD = 4.0V, WDT disabled, 0°C to +70°C VDD = 4.0V, WDT disabled, -40°C to +85°C VDD = 4.0V, WDT disabled, -40°C to +125°C
D022* D022A*	ΔIWD ΔIBOR	Module Differential Current ⁽⁶⁾ Watchdog Timer Brown-out Reset	— —	6.0 TBD	20 200	μA μA	WDTE bit set, VDD = 4.0V BODEN bit set, VDD = 5.0V
1A	FOSC	LP Oscillator Operating Frequency RC Oscillator Operating Frequency XT Oscillator Operating Frequency HS Oscillator Operating Frequency	0 0 0 0	— — — —	200 4 4 20	KHz MHz MHz MHz	All temperatures All temperatures All temperatures All temperatures

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD and VSS.

4: For RC Osc mode, current through REXT is not included. The current through the resistor can be estimated by the formula $I_r = VDD/2R_{EXT}$ (mA) with REXT in kOhm.

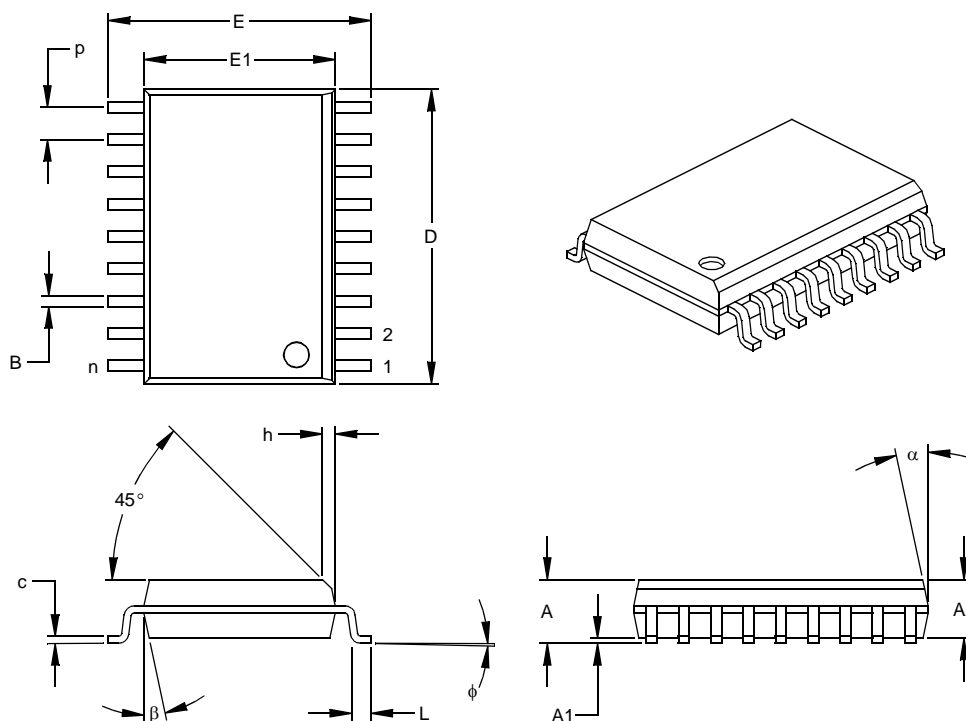
5: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

7: This is the voltage where the device enters the Brown-out Reset. When BOR is enabled, the device will operate correctly to this trip point.

18-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	P		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.012	0.23	0.27	0.30
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

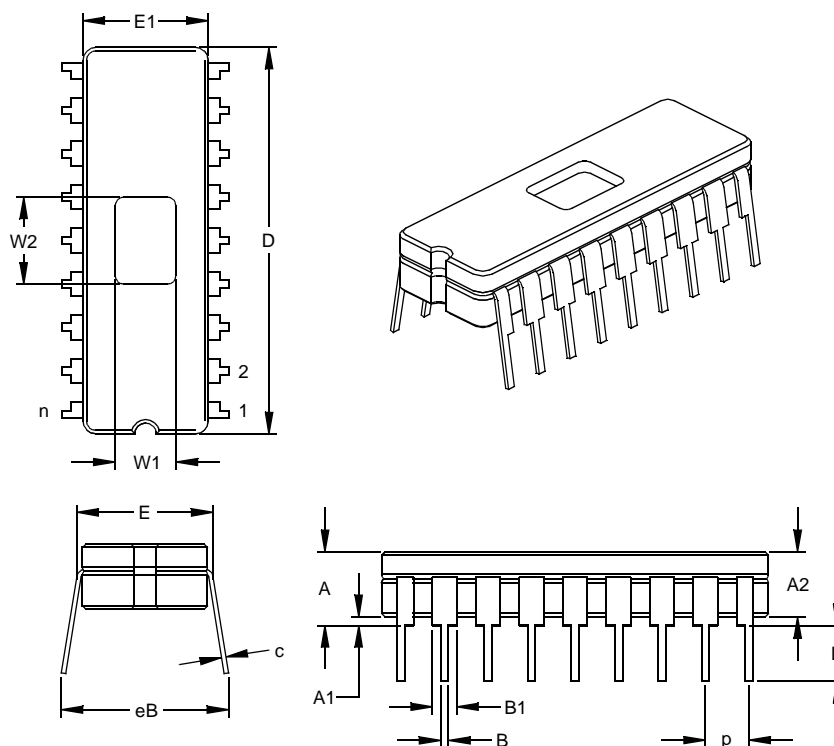
JEDEC Equivalent: MS-013

Drawing No. C04-051

PIC16C712/716

18-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.170	.183	.195	4.32	4.64	4.95
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.023	.030	0.38	0.57	0.76
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Ceramic Pkg. Width	E1	.285	.290	.295	7.24	7.37	7.49
Overall Length	D	.880	.900	.920	22.35	22.86	23.37
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81
Lead Thickness	c	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.055	.060	1.27	1.40	1.52
Lower Lead Width	B	.016	.019	.021	0.41	0.47	0.53
Overall Row Spacing	§ eB	.345	.385	.425	8.76	9.78	10.80
Window Width	W1	.130	.140	.150	3.30	3.56	3.81
Window Length	W2	.190	.200	.210	4.83	5.08	5.33

* Controlling Parameter
 § Significant Characteristic
 JEDEC Equivalent: MO-036
 Drawing No. C04-010

INDEX

A

A/D	45
A/D Converter Enable (ADIE Bit)	16
A/D Converter Flag (ADIF Bit)	17, 47
A/D Converter Interrupt, Configuring	47
ADCON0 Register	11, 45
ADCON1 Register	12, 45, 46
ADRES Register	11, 45, 47
Analog Port Pins, Configuring	49
Block Diagram	47
Block Diagram, Analog Input Model	48
Channel Select (CHS2:CHS0 Bits)	45
Clock Select (ADCS1:ADCS0 Bits)	45
Configuring the Module	47
Conversion Clock (Tad)	49
Conversion Status (GO/DONE Bit)	45, 47
Conversions	50
Converter Characteristics	86
Module On/Off (ADON Bit)	45
Port Configuration Control (PCFG2:PCFG0 Bits)	46
Sampling Requirements	48
Special Event Trigger (CCP)	41, 50
Timing Diagram	87
Absolute Maximum Ratings	73
ADCON0 Register	11, 45
ADCS1:ADCS0 Bits	45
ADON Bit	45
CHS2:CHS0 Bits	45
GO/DONE Bit	45, 47
ADCON1 Register	12, 45, 46
PCFG2:PCFG0 Bits	46
ADRES Register	11, 45, 47
Analog-to-Digital Converter. <i>See</i> A/D Architecture	
PIC16C712/716 Block Diagram	5
Assembler	
MPASM Assembler	70

B

Banking, Data Memory	10, 13
BOR. <i>See</i> Brown-out Reset	
Brown-Out Reset (BOR)	55
Brown-out Reset (BOR)	51, 54, 58, 59
BOR Enable (BODEN Bit)	52
BOR Status (BOR Bit)	18
Timing Diagram	83

C

C Compilers	
MPLAB C18	70
MPLAB C30	70
Capture (CCP Module)	40
Block Diagram	40
CCP Pin Configuration	40
CCPR1H:CCPR1L Registers	40
Changing Between Capture Prescalers	40
Software Interrupt	40
Timer1 Mode Selection	40
Capture/Compare/PWM (CCP)	39
Capture Mode. <i>See</i> Capture	
CCP1CON Register	11, 39
CCPR1H Register	11, 39
CCPR1L Register	11, 39
Compare Mode. <i>See</i> Compare	

Enable (CCP1IE Bit)	16
Flag (CCP1IF Bit)	17
PWM Mode. <i>See</i> PWM	
Timer Resources	39
Timing Diagram	85
CCP1CON Register	39
CCP1M3:CCP1M0 Bits	39
CCP1X:CCP1Y Bits	39
Code Protection	51, 65
CP1:CP0 Bits	52
Compare (CCP Module)	41
Block Diagram	41
CCP Pin Configuration	41
CCPR1H:CCPR1L Registers	41
Software Interrupt	41
Special Event Trigger	34, 41, 50
Timer1 Mode Selection	41
Configuration Bits	51
Conversion Considerations	95
Customer Change Notification Service	101
Customer Notification Service	101
Customer Support	101

D

Data Memory	10
Bank Select (RP1:RP0 Bits)	10, 13
General Purpose Registers	10
Register File Map	10
Special Function Registers	11
DC Characteristics	75, 77
Development Support	69
Direct Addressing	20

E

Electrical Characteristics	73
Errata	3
External Power-on Reset Circuit	55

F

Family of Devices	
PIC16C7XX	2
Firmware Instructions	67

I

I/O Ports	21
ID Locations	51, 65
In-Circuit Serial Programming™ (ICSP™)	51, 65
Indirect Addressing	20
FSR Register	10, 11, 20
INDF Register	11
Instruction Format	67
Instruction Set	67
Summary Table	68
INT Interrupt (RB0/INT). <i>See</i> Interrupt Sources	
INTCON Register	11, 15
GIE Bit	15
INTE Bit	15
INTF Bit	15
PEIE Bit	15
RBIE Bit	15
RBIF Bit	15, 24
TOIE Bit	15
TOIF Bit	15
Internet Address	101

PORTC	
TRISC Register	12
Postscaler, Timer2	
Select (TOUTPS3:TOUTPS0 Bits)	36
Postscaler, WDT	29
Assignment (PSA Bit)	14, 29
Block Diagram	30
Rate Select (PS2:PS0 Bits)	14, 29
Switching Between Timer0 and WDT	30
Power-down Mode. <i>See</i> Sleep	
Power-on Reset (POR)	51, 54, 55, 58, 59
Oscillator Start-up Timer (OST)	51, 55
POR Status ($\overline{\text{POR}}$ Bit)	18
Power Control (PCON) Register	58
Power-down (PD Bit)	13, 54
Power-on Reset Circuit, External	55
Power-up Timer (PWRT)	51, 55
PWRT Enable (PWRTE Bit)	52
Time-out ($\overline{\text{TO}}$ Bit)	13, 54
Time-out Sequence	57
Time-out Sequence on Power-up	60
Timing Diagram	83
Prescaler, Capture	40
Prescaler, Timer0	29
Assignment (PSA Bit)	14, 29
Block Diagram	30
Rate Select (PS2:PS0 Bits)	14, 29
Switching Between Timer0 and WDT	30
Prescaler, Timer1	32
Select (T1CKPS1:T1CKPS0 Bits)	31
Prescaler, Timer2	42
Select (T2CKPS1:T2CKPS0 Bits)	36
Product Identification System	103
Program Counter	
PCL Register	11, 19
PCLATH Register	11, 19, 62
Reset Conditions	58
Program Memory	9
Interrupt Vector	9
Paging	9, 19
Program Memory Map	9
Reset Vector	9
Program Verification	65
Programming, Device Instructions	67
PWM (CCP Module)	42
Block Diagram	42
CCPR1H:CCPR1L Registers	42
Duty Cycle	42
Example Frequencies/Resolutions	43
Output Diagram	42
Period	42
Set-Up for PWM Operation	43
TMR2 to PR2 Match	36, 42
TMR2 to PR2 Match Enable (TMR2IE Bit)	16
TMR2 to PR2 Match Flag (TMR2IF Bit)	17
Q	
Q-Clock	42
R	
RAM. <i>See</i> Data Memory	
Reader Response	104
Register File	10
Register File Map	10
Reset	51, 54
Block Diagram	56

Brown-out Reset (BOR). <i>See</i> Brown-out Reset (BOR)	
MCLR Reset. <i>See</i> MCLR	
Power-on Reset (POR). <i>See</i> Power-on Reset (POR)	
Reset Conditions for All Registers	59
Reset Conditions for PCON Register	58
Reset Conditions for Program Counter	58
Reset Conditions for STATUS Register	58
Timing Diagram	83
WDT Reset. <i>See</i> Watchdog Timer (WDT)	
Revision History	95

S

Sleep	64
Sleep	51, 54
Software Simulator (MPLAB SIM)	70
Special Event Trigger. <i>See</i> Compare	
Special Features of the CPU	51
Special Function Registers	11
Speed, Operating	1
Stack	19
STATUS Register	11, 13, 62
C Bit	13
DC Bit	13
IRP Bit	13
$\overline{\text{PD}}$ Bit	13, 54
RP1:RP0 Bits	13
TO Bit	13, 54
Z Bit	13

T

T1CON Register	11, 31
T1CKPS1:T1CKPS0 Bits	31
T1OSCEN Bit	31
T1SYNC Bit	31
TMR1CS Bit	31
TMR1ON Bit	31
T2CON Register	11, 36
T2CKPS1:T2CKPS0 Bits	36
TMR2ON Bit	36
TOUTPS3:TOUTPS0 Bits	36
Timer0	29
Block Diagram	29
Clock Source Edge Select (T0SE Bit)	14, 29
Clock Source Select (T0CS Bit)	14, 29
Overflow Enable (T0IE Bit)	15
Overflow Flag (T0IF Bit)	15, 62
Overflow Interrupt	30, 62
Prescaler. <i>See</i> Prescaler, Timer0	
Timing Diagram	84
TMR0 Register	11
Timer1	31
Block Diagram	32
Capacitor Selection	34
Clock Source Select (TMR1CS Bit)	31
External Clock Input Sync (T1SYNC Bit)	31
Module On/Off (TMR1ON Bit)	31
Oscillator	31, 34
Oscillator Enable (T1OSCEN Bit)	31
Overflow Enable (TMR1IE Bit)	16
Overflow Flag (TMR1IF Bit)	17
Overflow Interrupt	31, 34
Prescaler. <i>See</i> Prescaler, Timer1	
Special Event Trigger (CCP)	34, 41
T1CON Register	11, 31
Timing Diagram	84
TMR1H Register	11, 31

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rPIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MTP, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

Analog-for-the-Digital Age, Application Maestro, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscent Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICtail, REAL ICE, rLAB, Select Mode, SQL, Serial Quad I/O, Total Endurance, TSHARC, UniWinDriver, WiperLock, ZENA and Z-Scale are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

GestIC and ULPP are registered trademarks of Microchip Technology Germany II GmbH & Co. & KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 1999-2013, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

ISBN: 9781620769751

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
= ISO/TS 16949 =

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.