What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc716t-04i-so

TABLE 1-1:   PIC16C712/716 PINOUT DESCRIPTION (CONTINUED)

Pin Name	PIC16C712/716 DIP, SOIC	SSOP	Pin Type	Buffer Type	Description
					PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/INT	6	7			
RB0			I/O	TTL	Digital I/O
INT			I	ST	External Interrupt
RB1/T1OSO/T1CKI	7	8			
RB1			I/O	TTL	Digital I/O
T1OSO			O	—	Timer1 oscillator output. Connects to crystal in oscillator mode.
T1CKI			I	ST	Timer1 external clock input.
RB2/T1OSI	8	9			
RB2			I/O	TTL	Digital I/O
T1OSI			I	—	Timer1 oscillator input. Connects to crystal in oscillator mode.
RB3/CCP1	9	10			
RB3			I/O	TTL	Digital I/O
CCP1			I/O	ST	Capture1 input, Compare1 output, PWM1 output.
RB4	10	12	I/O	TTL	Digital I/O Interrupt on change pin.
RB5	11	12	I/O	TTL	Digital I/O Interrupt on change pin.
RB6	12	13	I/O	TTL	Digital I/O Interrupt on change pin.
			I	ST	ICSP programming clock.
RB7	13	14	I/O	TTL	Digital I/O Interrupt on change pin.
			I/O	ST	ICSP programming data.
V$_{SS}$	5	5, 6	P	—	Ground reference for logic and I/O pins.
V$_{DD}$	14	15, 16	P	—	Positive supply for logic and I/O pins.

Legend: TTL = TTL-compatible input   CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
OD = Open drain output
SM = SMBus compatible input. An external resistor is required if this pin is used as an output
NPU = N-channel pull-up   PU = Weak internal pull-up
No-P diode = No P-diode to V$_{DD}$ AN = Analog input or output
I = input   O = output
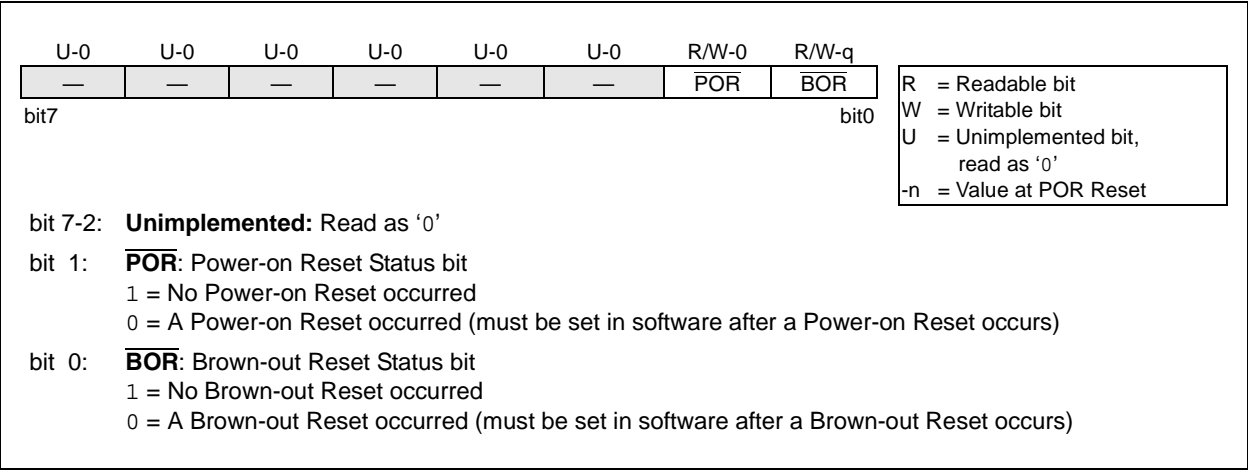P = Power   L = LCD Driver

2.2.2.6 PCON Register

The Power Control (PCON) register contains a flag bit to allow differentiation between a Power-on Reset (POR) to an external MCLR Reset or WDT Reset. These devices contain an additional bit to differentiate a Brown-out Reset condition from a Power-on Reset condition.

> **Note:** If the BODEN Configuration bit is set, BOR is '1' on Power-on Reset. If the BODEN Configuration bit is clear, BOR is unknown on Power-on Reset.
>
> The BOR Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (the BODEN Configuration bit is clear). BOR must then be set by the user and checked on subsequent resets to see if it is clear, indicating a brown-out has occurred.

FIGURE 2-9: PCON REGISTER (ADDRESS 8Eh)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-q
—	—	—	—	—	—	POR	BOR

bit7   bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
-n = Value at POR Reset

bit 7-2: **Unimplemented:** Read as '0'

bit 1: **POR**: Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0: **BOR**: Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

PORTB pins RB3:RB1 are multiplexed with several peripheral functions (Table 3-3). PORTB pins RB3:RB0 have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTB pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify-write instructions (BSF, BCF, XORWF) with TRISB as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

Four of PORTB's pins, RB7:RB4, have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt-on-change comparison). The input pins, RB7:RB4, are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).
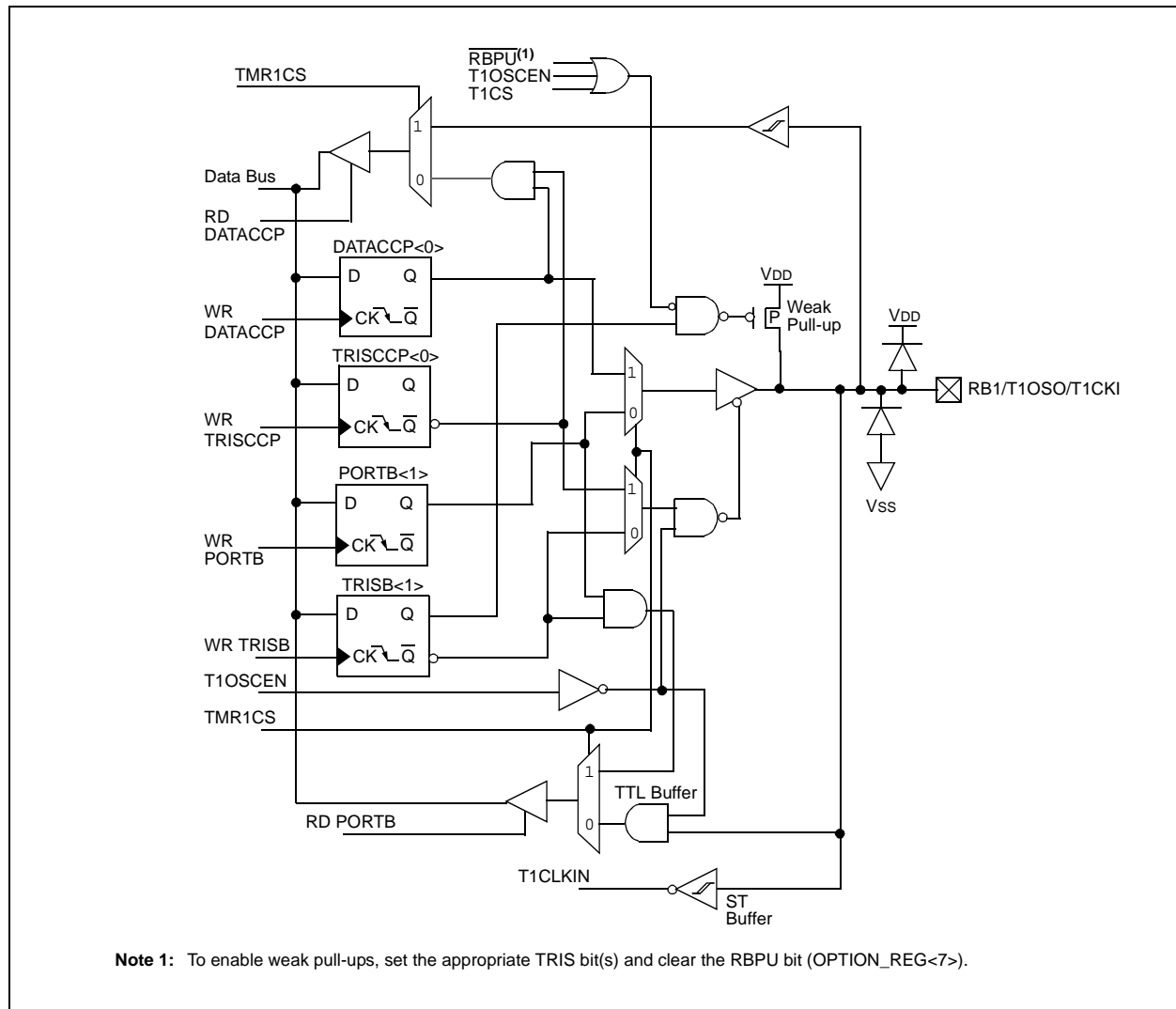
This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB will end the mismatch condition.

b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

FIGURE 3-4:   **BLOCK DIAGRAM OF RB1/T1OSO/T1CKI PIN**

Note 1: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the RBPU bit (OPTION_REG<7>).

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TABLE 3-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
81h	OPTION_REG	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

FIGURE 5-2: **TIMER1 BLOCK DIAGRAM**

Note 1: When the T1OSCEN bit is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.

5.2 Timer1 Module and PORTB Operation

When Timer1 is configured as timer running from the main oscillator, PORTB<2:1> operate as normal I/O lines. When Timer1 is configured to function as a counter however, the clock source selection may affect the operation of PORTB<2:1>. Multiplexing details of the Timer1 clock selection on PORTB are shown in Figure 3-4 and Figure 3-5.

The clock source for Timer1 in the Counter mode can be from one of the following:

1. External circuit connected to the RB1/T1OSO/T1CKI pin
2. Firmware controlled DATACCP<0> bit, DT1CKI
3. Timer1 oscillator

Table 5-1 shows the details of Timer1 mode selections, control bit settings, TMR1 and PORTB operations.

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7.1 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin RB3/CCP1. An event is defined as:

- every falling edge
- every rising edge
- every 4th rising edge
- every 16th rising edge

An event is selected by control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit CCP1IF (PIR1<2>) is set. It must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value will be lost.

FIGURE 7-3: CAPTURE MODE OPERATION BLOCK DIAGRAM
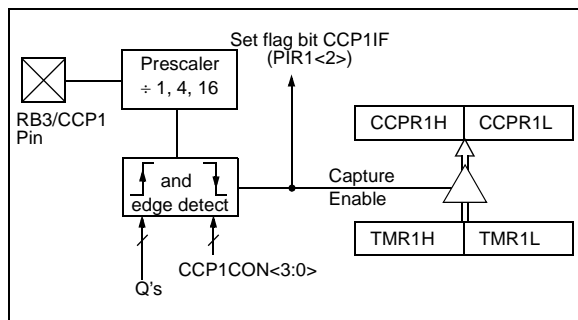
7.1.1 CCP PIN CONFIGURATION

In Capture mode, the CCP output must be disabled by setting the TRISCCP<2> bit.

> **Note:** If the RB3/CCP1 is configured as an output by clearing the TRISCCP<2> bit, a write to the DCCP bit can cause a capture condition.

7.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

7.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep bit CCP1IE (PIE1<2>) clear to avoid false interrupts and should clear the flag bit CCP1IF following any such change in Operating mode.

7.1.4 CCP PRESCALER

There are four prescaler settings, specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. This means that any Reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore the first capture may be from a non-zero prescaler. Example 7-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

EXAMPLE 7-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
CLRF    CCP1CON      ;Turn CCP module off
MOVLW   NEW_CAPT_PS  ;Load the W reg with
                     ; the new prescaler
                     ; mode value and CCP ON
MOVWF   CCP1CON      ;Load CCP1CON with this
                     ; value
```

7.2 Compare Mode

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the RB3/CCP1 pin is either:

• driven High
• driven Low
• remains Unchanged

The action on the pin is based on the value of control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). At the same time, interrupt flag bit CCP1IF is set.

FIGURE 7-4: **COMPARE MODE OPERATION BLOCK DIAGRAM**
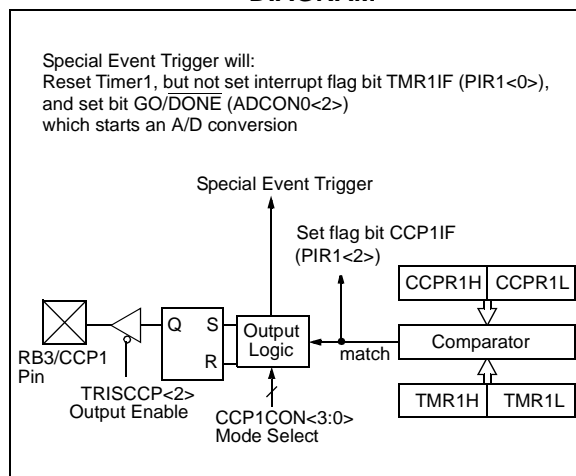
7.2.1 CCP PIN CONFIGURATION

The user must configure the RB3/CCP1 pin as the CCP output by clearing the TRISCCP<2> bit.

> **Note:** Clearing the CCP1CON register will force the RB3/CCP1 compare output latch to the default low level. This is neither the PORTB I/O data latch nor the DATACCP latch.

7.2.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

7.2.3 SOFTWARE INTERRUPT MODE

When generate software interrupt is chosen the CCP1 pin is not affected. Only a CCP interrupt is generated (if enabled).

7.2.4 SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated which may be used to initiate an action.

The Special Event Trigger output of CCP1 resets the TMR1 register pair. This allows the CCPR1 register to effectively be a 16-bit programmable period register for Timer1.

The Special Event Trigger output of CCP1 also starts an A/D conversion (if the A/D module is enabled).

> **Note:** The Special Event Trigger from the CCP1 module will not set interrupt flag bit TMR1IF (PIR1<0>).

TABLE 7-2: **REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, AND TIMER1**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
07h	DATACCP	—	—	—	—	—	DCCP	—	DT1CK	xxxx xxxx	xxxx xuxu
0Bh,8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	—	CCP1IF	TMR2IF	TMR1IF	-0-- -000	-0-- -000
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu
15h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
87h	TRISCCP	—	—	—	—	—	TCCP	—	TT1CK	xxxx x1x1	xxxx x1x1
8Ch	PIE1	—	ADIE	—	—	—	CCP1IE	TMR2IE	TMR1IE	-0-- -000	-0-- -000

Legend: x = unknown, u = unchanged, — = unimplemented read as '0'. Shaded cells are not used by Capture and Timer1.

7.3.3   SET-UP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
3. Make the CCP1 pin an output by clearing the TRISCCP<2> bit.
4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
5. Configure the CCP1 module for PWM operation.

TABLE 7-3:   EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 20 MHz

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	5.5

TABLE 7-4:   REGISTERS ASSOCIATED WITH PWM AND TIMER2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
07h	DATACCP	—	—	—	—	—	DCCP	—	DT1CK	xxxx xxxx	xxxx xuxu
0Bh,8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	—	CCP1IF	TMR2IF	TMR1IF	-0-- -000	-0-- -000
11h	TMR2	Timer2 Module's Register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
87h	TRISCCP	—	—	—	—	—	TCCP	—	TT1CK	xxxx x1x1	xxxx x1x1
8Ch	PIE1	—	ADIE	—	—	—	CCP1IE	TMR2IE	TMR1IE	-0-- -000	-0-- -000
92h	PR2	Timer2 Module's Period Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, — = unimplemented read as '0'. Shaded cells are not used by PWM and Timer2.

FIGURE 8-2: ADCON1 REGISTER (ADDRESS 9Fh)

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCFG2	PCFG1	PCFG0

bit7   bit0

```
R  = Readable bit
W  = Writable bit
U  = Unimplemented bit,
     read as '0'
-n = Value at POR
     Reset
```

bit 7-3: **Unimplemented:** Read as '0'

bit 2-0: **PCFG2:PCFG0**: A/D Port Configuration Control bits

PCFG2:PCFG0	RA0	RA1	RA2	RA3	V$_{REF}$
0x0	A	A	A	A	V$_{DD}$
0x1	A	A	A	V$_{REF}$	RA3
100	A	A	D	A	V$_{DD}$
101	A	A	D	V$_{REF}$	RA3
11x	D	D	D	D	V$_{DD}$

A = Analog input

D = Digital I/O
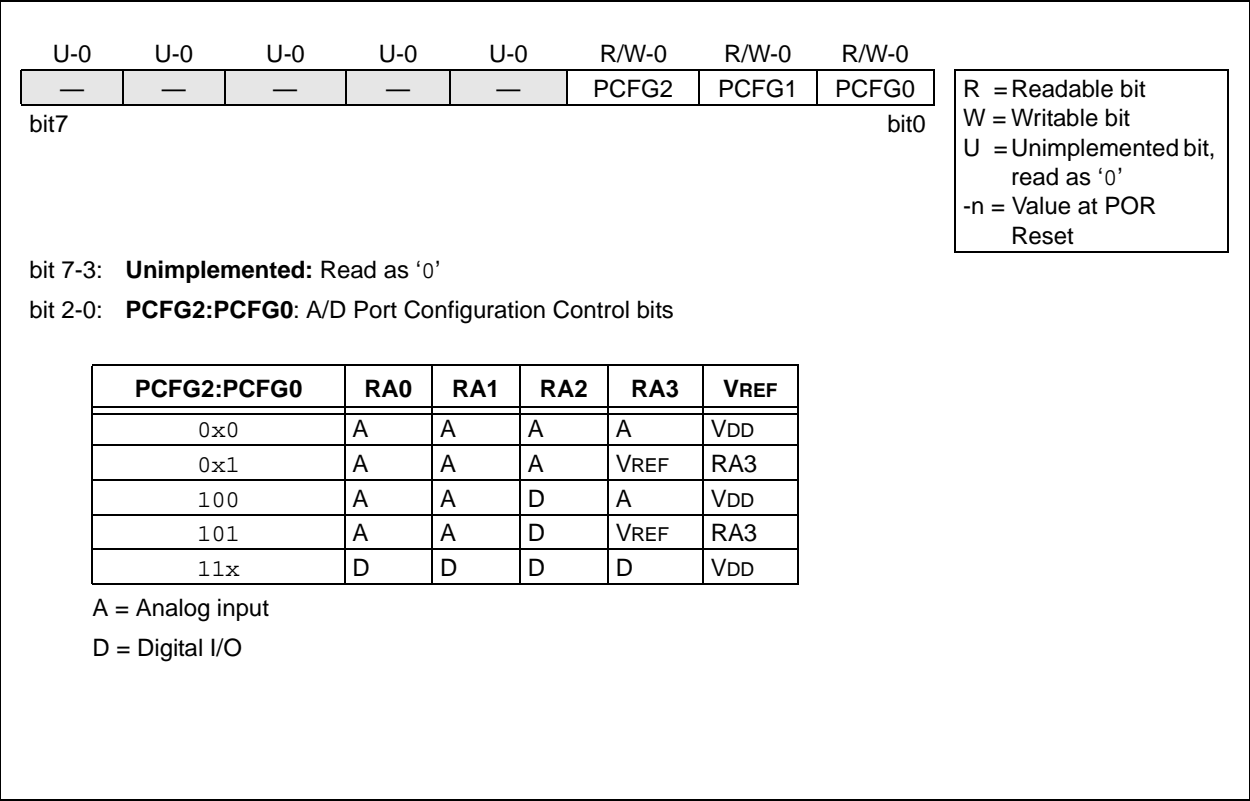
FIGURE 9-1: **CONFIGURATION WORD**

CP1	CP0	CP1	CP0	CP1	CP0	—	BODEN	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0

bit13   bit0

Register:CONFIG
Address2007h

bit 13-8, 5-4: **$\overline{CP1:CP0}$**: Code Protection bits **(2)**
Code Protection for 2K Program memory (PIC16C716)
11 = Programming code protection off
10 = 0400h-07FFh code protected
01 = 0200h-07FFh code protected
00 = 0000h-07FFh code protected

bit 13-8, 5-4:
Code Protection for 1K Program memory bits (PIC16C712)
11 = Programming code protection off
10 = Programming code protection off
01 = 0200h-03FFh code-protected
00 = 0000h-03FFh code-protected

bit 7:   **Unimplemented**: Read as '1'
bit 6:   **BODEN**: Brown-out Reset Enable bit **(1)**
1 = BOR enabled
0 = BOR disabled
bit 3:   **$\overline{PWRTE}$**: Power-up Timer Enable bit **(1)**
1 = PWRT disabled
0 = PWRT enabled
bit 2:   **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled
bit 1-0:   **FOSC1:FOSC0**: Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: Enabling Brown-out Reset automatically enables Power-up Timer (PWRT) regardless of the value of bit $\overline{PWRTE}$.
Ensure the Power-up Timer is enabled anytime Brown-out Reset is enabled.

2: All of the $\overline{CP1:CP0}$ pairs have to be given the same value to enable the code protection scheme listed.

9.12   Watchdog Timer (WDT)

The Watchdog Timer is as a free running, on-chip, RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device have been stopped, for example, by execution of a SLEEP instruction.

During normal operation, a WDT Time-out generates a device Reset (Watchdog Timer Reset). If the device is in Sleep mode, a WDT Time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The $\overline{TO}$ bit in the STATUS register will be cleared upon a Watchdog Timer Time-out.

The WDT can be permanently disabled by clearing Configuration bit WDTE (**Section 9.1 "Configuration Bits"**).

WDT time-out period values may be found in the Electrical Specifications section under T_{WDT} (parameter #31). Values for the WDT prescaler (actually a postscaler, but shared with the Timer0 prescaler) may be assigned using the OPTION_REG register.

> **Note:**   The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device Reset condition.

.

> **Note:**   When a CLRWDT instruction is executed and the prescaler is assigned to the WDT, the prescaler count will be cleared, but the prescaler assignment is not changed.

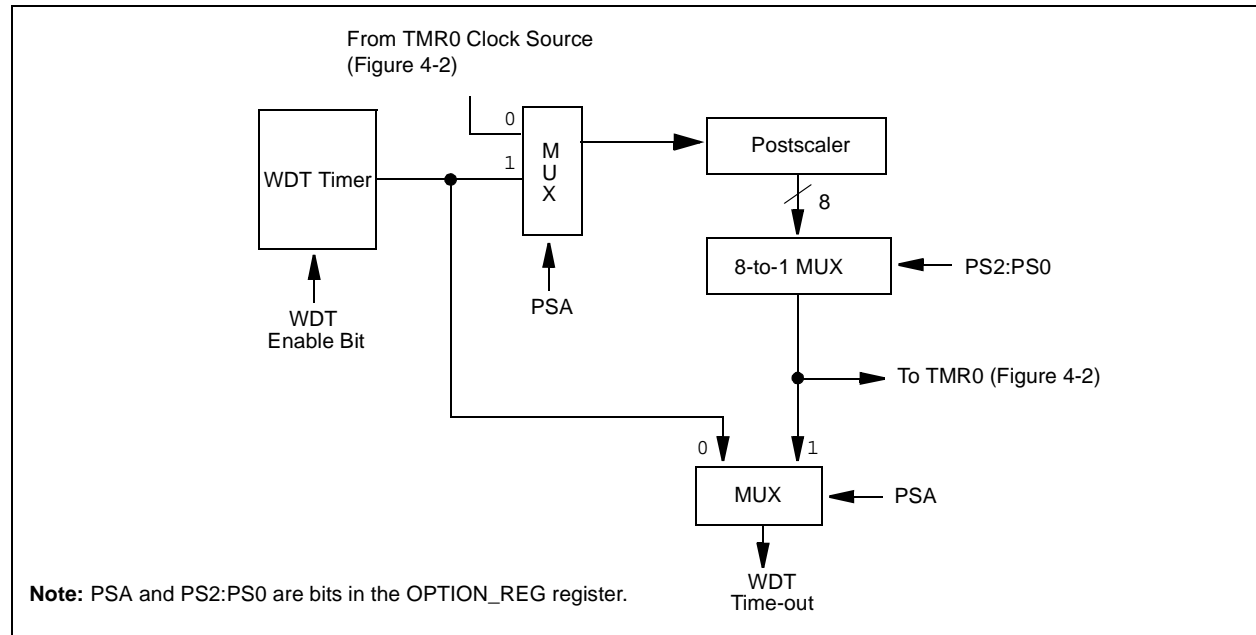**FIGURE 9-15:   WATCHDOG TIMER BLOCK DIAGRAM**

FIGURE 9-16:   SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bits 13:8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	**(1)**	—	BODEN[1]	$\overline{CP1}$	$\overline{CP0}$	PWRTE[1]	WDTE	FOSC1	FOSC0
81h	OPTION_REG	N/A	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.
Note 1:   See Figure 9-1 for operation of these bits.

9.16   In-Circuit Serial Programming™

PIC16CXXX microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

For complete details on serial programming, please refer to the In-Circuit Serial Programming™ (ICSP™) Guide, (DS30277).

10.0   INSTRUCTION SET SUMMARY

Each PIC16CXXX instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CXXX instruction set summary in Table 10-2 lists **byte-oriented**, **bit-oriented**, and **literal and control** operations. Table 10-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

TABLE 10-1:   OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
PC	Program Counter
$\overline{TO}$	Time-out bit
$\overline{PD}$	Power-down bit
Z	Zero bit
DC	Digit Carry bit
C	Carry bit

The instruction set is highly orthogonal and is grouped into three basic categories:

• **Byte-oriented** operations
• **Bit-oriented** operations
• **Literal and control** operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs.

Table 10-2 lists the instructions recognized by the MPASM assembler.

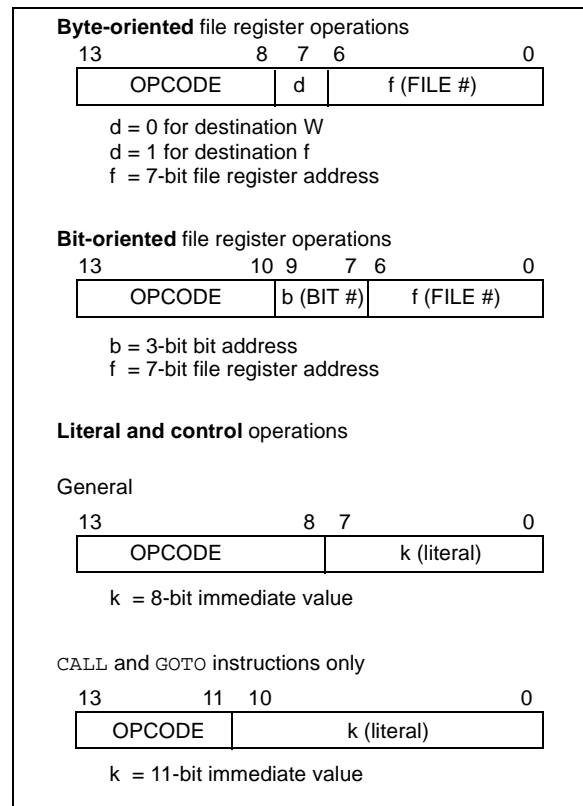Figure 10-1 shows the general formats that the instructions can have.

> **Note:** To maintain upward compatibility with future PIC16CXXX products, do not use the OPTION and TRIS instructions.

All examples use the following format to represent a hexadecimal number:

    0xhh

where h signifies a hexadecimal digit.

FIGURE 10-1:   GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations
```
13            8  7  6            0
| OPCODE     | d | f (FILE #)     |
```
d = 0 for destination W
d = 1 for destination f
f = 7-bit file register address

Bit-oriented file register operations
```
13          10 9   7 6            0
| OPCODE    | b (BIT #) | f (FILE #) |
```
b = 3-bit bit address
f = 7-bit file register address

Literal and control operations

General
```
13              8  7            0
| OPCODE       | k (literal)     |
```
k = 8-bit immediate value

CALL and GOTO instructions only
```
13        11 10               0
| OPCODE  | k (literal)        |
```
k = 11-bit immediate value

A description of each instruction is available in the PIC® Mid-Range Reference Manual, (DS33023).

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TABLE 10-2: **PIC16CXXX INSTRUCTION SET**

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb	LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS							
ADDWF	**f, d**	Add W and f	1	00	0111 dfff ffff	C,DC,Z	**1,2**
ANDWF	**f, d**	AND W with f	1	00	0101 dfff ffff	Z	**1,2**
CLRF	**f**	Clear f	1	00	0001 1fff ffff	Z	**2**
CLRW	**-**	Clear W	1	00	0001 0000 0011	Z	
COMF	**f, d**	Complement f	1	00	1001 dfff ffff	Z	**1,2**
DECF	**f, d**	Decrement f	1	00	0011 dfff ffff	Z	**1,2**
DECFSZ	**f, d**	Decrement f, Skip if 0	1(2)	00	1011 dfff ffff		**1,2,3**
INCF	**f, d**	Increment f	1	00	1010 dfff ffff	Z	**1,2**
INCFSZ	**f, d**	Increment f, Skip if 0	1(2)	00	1111 dfff ffff		**1,2,3**
IORWF	**f, d**	Inclusive OR W with f	1	00	0100 dfff ffff	Z	**1,2**
MOVF	**f, d**	Move f	1	00	1000 dfff ffff	Z	**1,2**
MOVWF	**f**	Move W to f	1	00	0000 1fff ffff		
NOP	**-**	No Operation	1	00	0000 0xx0 0000		
RLF	**f, d**	Rotate Left f through Carry	1	00	1101 dfff ffff	C	**1,2**
RRF	**f, d**	Rotate Right f through Carry	1	00	1100 dfff ffff	C	**1,2**
SUBWF	**f, d**	Subtract W from f	1	00	0010 dfff ffff	C,DC,Z	**1,2**
SWAPF	**f, d**	Swap nibbles in f	1	00	1110 dfff ffff		**1,2**
XORWF	**f, d**	Exclusive OR W with f	1	00	0110 dfff ffff	Z	**1,2**
BIT-ORIENTED FILE REGISTER OPERATIONS							
BCF	**f, b**	Bit Clear f	1	01	00bb bfff ffff		**1,2**
BSF	**f, b**	Bit Set f	1	01	01bb bfff ffff		**1,2**
BTFSC	**f, b**	Bit Test f, Skip if Clear	1 (2)	01	10bb bfff ffff		**3**
BTFSS	**f, b**	Bit Test f, Skip if Set	1 (2)	01	11bb bfff ffff		**3**
LITERAL AND CONTROL OPERATIONS							
ADDLW	**k**	Add literal and W	1	11	111x kkkk kkkk	C,DC,Z	
ANDLW	**k**	AND literal with W	1	11	1001 kkkk kkkk	Z	
CALL	**k**	Call subroutine	2	10	0kkk kkkk kkkk		
CLRWDT	**-**	Clear Watchdog Timer	1	00	0000 0110 0100	$\overline{TO},\overline{PD}$	
GOTO	**k**	Go to address	2	10	1kkk kkkk kkkk		
IORLW	**k**	Inclusive OR literal with W	1	11	1000 kkkk kkkk	Z	
MOVLW	**k**	Move literal to W	1	11	00xx kkkk kkkk		
RETFIE	**-**	Return from interrupt	2	00	0000 0000 1001		
RETLW	**k**	Return with literal in W	2	11	01xx kkkk kkkk		
RETURN	**-**	Return from Subroutine	2	00	0000 0000 1000		
SLEEP	**-**	Go into standby mode	1	00	0000 0110 0011	$\overline{TO},\overline{PD}$	
SUBLW	**k**	Subtract W from literal	1	11	110x kkkk kkkk	C,DC,Z	
XORLW	**k**	Exclusive OR literal with W	1	11	1010 kkkk kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

PIC16C712/716

	Standard Operating Conditions (unless otherwise stated)
DC CHARACTERISTICS	Operating temperature 0°C $\leq T_A \leq$ +70°C for commercial -40°C $\leq T_A \leq$ +85°C for industrial -40°C $\leq T_A \leq$ +125°C for extended Operating voltage V_{DD} range as described in DC spec **Section 12.1 "DC Characteristics: PIC16C712/716-04 (Commercial, Industrial, Extended) PIC16C712/716-20 (Commercial, Industrial, Extended)"** and **Section 12.2 "DC Characteristics: PIC16LC712/716-04 (Commercial, Industrial)"**

Param No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
D080	V_{OL}	**Output Low Voltage** I/O ports	—	—	0.6	V	I_{OL} = 8.5 mA, V_{DD} = 4.5V, -40°C to +85°C
			—	—	0.6	V	I_{OL} = 7.0 mA, V_{DD} = 4.5V, -40°C to +125°C
D083		OSC2/CLKOUT (RC Osc mode)	—	—	0.6	V	I_{OL} = 1.6 mA, V_{DD} = 4.5V, -40°C to +85°C
			—	—	0.6	V	I_{OL} = 1.2 mA, V_{DD} = 4.5V, -40°C to +125°C
D090	V_{OH}	**Output High Voltage** I/O ports **(Note 3)**	V_{DD}-0.7	—	—	V	I_{OH} = -3.0 mA, V_{DD} = 4.5V, -40°C to +85°C
			V_{DD}-0.7	—	—	V	I_{OH} = -2.5 mA, V_{DD} = 4.5V, -40°C to +125°C
D092		OSC2/CLKOUT (RC Osc mode)	V_{DD}-0.7	—	—	V	I_{OH} = -1.3 mA, V_{DD} = 4.5V, -40°C to +85°C
			V_{DD}-0.7	—	—	V	I_{OH} = -1.0 mA, V_{DD} = 4.5V, -40°C to +125°C
D150*	V_{OD}	**Open-Drain High Voltage**	—	—	8.5	V	RA4 pin
D100	C_{OSC2}	**Capacitive Loading Specs on Output Pins** OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	C_{IO}	All I/O pins and OSC2 (in RC mode)	—	—	50	pF	

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC Oscillator mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC MCU be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$/V$_{PP}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

TABLE 12-7: A/D CONVERTER CHARACTERISTICS:
PIC16C712/716-04 (COMMERCIAL, INDUSTRIAL, EXTENDED)
PIC16C712/716-20 (COMMERCIAL, INDUSTRIAL, EXTENDED)
PIC16LC712/716-04 (COMMERCIAL, INDUSTRIAL)

Param No.	Sym.	Characteristic		Min.	Typ†	Max.	Units	Conditions
A01	N_R	Resolution		—	—	8-bits	bit	$V_{REF} = V_{DD} = 5.12V$, $V_{SS} \pounds V_{AIN} \pounds V_{REF}$
A02	E_{ABS}	Total Absolute error		—	—	< ± 1	LSb	$V_{REF} = V_{DD} = 5.12V$, $V_{SS} \pounds V_{AIN} \pounds V_{REF}$
A03	E_{IL}	Integral linearity error		—	—	< ± 1	LSb	$V_{REF} = V_{DD} = 5.12V$, $V_{SS} \pounds V_{AIN} \pounds V_{REF}$
A04	E_{DL}	Differential linearity error		—	—	< ± 1	LSb	$V_{REF} = V_{DD} = 5.12V$, $V_{SS} \pounds V_{AIN} \pounds V_{REF}$
A05	E_{FS}	Full scale error		—	—	< ± 1	LSb	$V_{REF} = V_{DD} = 5.12V$, $V_{SS} \pounds V_{AIN} \pounds V_{REF}$
A06	E_{OFF}	Offset error		—	—	< ± 1	LSb	$V_{REF} = V_{DD} = 5.12V$, $V_{SS} \pounds V_{AIN} \pounds V_{REF}$
A10	—	Monotonicity		—	guaranteed **(Note 3)**	—	—	$V_{SS} \pounds V_{AIN} \pounds V_{REF}$
A20	V_{REF}	Reference voltage		2.5V	—	$V_{DD} + 0.3$	V	
A25	V_{AIN}	Analog input voltage		$V_{SS} - 0.3$	—	$V_{REF} + 0.3$	V	
A30	Z_{AIN}	Recommended impedance of analog voltage source		—	—	10.0	kΩ	
A40	I_{AD}	A/D conversion current (V_{DD})	Standard	—	180	—	μA	Average current consumption when A/D is on. **(Note 1)**
			Extended (LC)	—	90	—	μA	
A50	I_{REF}	V_{REF} input current **(Note 2)**		10	—	1000	μA	During V_{AIN} acquisition. Based on differential of V_{HOLD} to V_{AIN} to charge C_{HOLD}, see **Section 9.1 "Configuration Bits"**.
				—	—	10	μA	During A/D Conversion cycle

2: * These parameters are characterized but not tested.

3: † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current.
The power-down current spec includes any such leakage from the A/D module.

2: V_{REF} current is from RA3 pin or V_{DD} pin, whichever is selected as reference input.

3: The A/D conversion result never decreases with an increase in the Input Voltage, and has no missing codes.
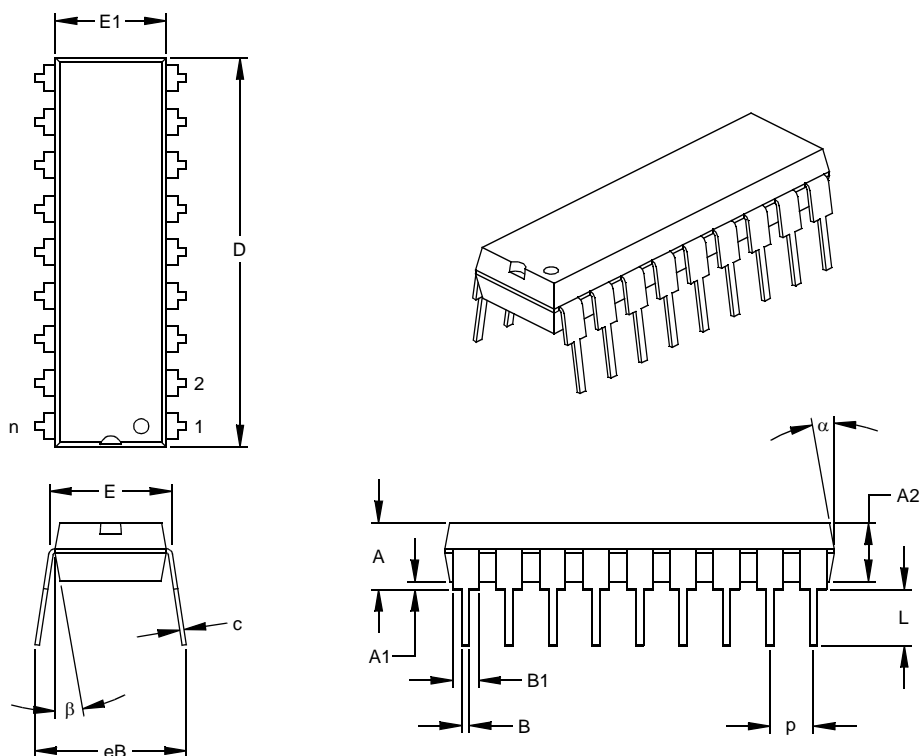
13.2   Package Details

The following sections give the technical details of the packages.

18-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

	Units	INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.890	.898	.905	22.61	22.80	22.99
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-007

NOTES:

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