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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	72MHz
Connectivity	CANbus, Ethernet, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	70
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	98K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2387fbd100-551

- On-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the RTC oscillator.
- Versatile pin function selections allow more possibilities for using on-chip peripheral functions.

3. Applications

- Industrial control
- Medical systems
- Protocol converter
- Communications

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2387FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash (kB)	SRAM (kB)					Ethernet	USB device + 4 kB FIFO	SD/MMC	GP DMA	Channels			Temp range
		Local bus	Ethernet buffers	GP/USB	RTC	Total					CAN	ADC	DAC	
LPC2387FBD100	512	64	16	16	2	98	RMII	yes	yes	yes	2	6	1	−40 °C to +85 °C

5. Block diagram

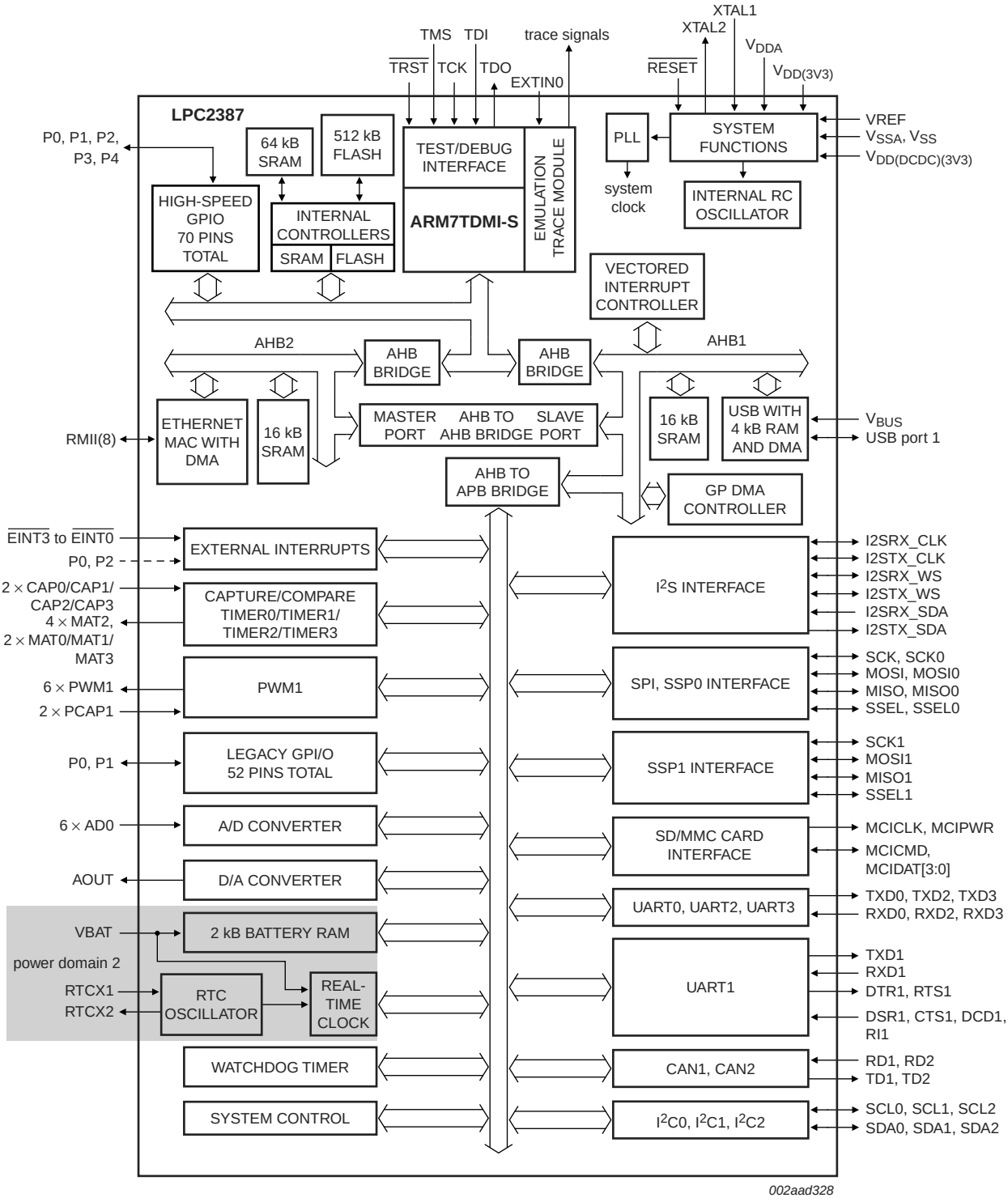


Fig 1. LPC2387 block diagram

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P1[18]/ USB_UP_LED/ PWM1[1]/ CAP1[0]	32[1]	I/O	**P1[18] —** General purpose digital input/output pin.
		O	**USB_UP_LED —** USB GoodLink LED indicator. It is LOW when device is configured (non-control endpoints enabled), or when host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when host is enabled and detects activity on the bus.
		O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
		I	**CAP1[0] —** Capture input for Timer 1, channel 0.
P1[19]/ USB_TX_E1/ USB_PPWR1/ CAP1[1]	33[1]	I/O	**P1[19] —** General purpose digital input/output pin.
		O	**USB_TX_E1 —** Transmit Enable signal for USB port 1 (OTG transceiver).
		O	**USB_PPWR1 —** Port Power enable signal for USB port 1.
		I	**CAP1[1] —** Capture input for Timer 1, channel 1.
P1[20]/ USB_TX_DP1/ PWM1[2]/SCK0	34[1]	I/O	**P1[20] —** General purpose digital input/output pin.
		O	**USB_TX_DP1 —** D+ transmit data for USB port 1 (OTG transceiver).
		O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
		I/O	**SCK0 —** Serial clock for SSP0.
P1[21]/ USB_TX_DM1/ PWM1[3]/SSEL0	35[1]	I/O	**P1[21] —** General purpose digital input/output pin.
		O	**USB_TX_DM1 —** D− transmit data for USB port 1 (OTG transceiver).
		O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
		I/O	**SSEL0 —** Slave Select for SSP0.
P1[22]/ USB_RCV1/ USB_PWRD1/ MAT1[0]	36[1]	I/O	**P1[22] —** General purpose digital input/output pin.
		I	**USB_RCV1 —** Differential receive data for USB port 1 (OTG transceiver).
		I	**USB_PWRD1 —** Power Status for USB port 1 (host power switch).
		O	**MAT1[0] —** Match output for Timer 1, channel 0.
P1[23]/ USB_RX_DP1/ PWM1[4]/MISO0	37[1]	I/O	**P1[23] —** General purpose digital input/output pin.
		I	**USB_RX_DP1 —** D+ receive data for USB port 1 (OTG transceiver).
		O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
		I/O	**MISO0 —** Master In Slave Out for SSP0.
P1[24]/ USB_RX_DM1/ PWM1[5]/MOSI0	38[1]	I/O	**P1[24] —** General purpose digital input/output pin.
		I	**USB_RX_DM1 —** D− receive data for USB port 1 (OTG transceiver).
		O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
		I/O	**MOSI0 —** Master Out Slave in for SSP0.
P1[25]/ USB_LS1/ USB_HSTEN1/ MAT1[1]	39[1]	I/O	**P1[25] —** General purpose digital input/output pin.
		O	**USB_LS1 —** Low-speed status for USB port 1 (OTG transceiver).
		O	**USB_HSTEN1 —** Host Enabled status for USB port 1.
		O	**MAT1[1] —** Match output for Timer 1, channel 1.
P1[26]/ USB_SSPND1/ PWM1[6]/ CAP0[0]	40[1]	I/O	**P1[26] —** General purpose digital input/output pin.
		O	**USB_SSPND1 —** USB port 1 bus suspend status (OTG transceiver).
		O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
		I	**CAP0[0] —** Capture input for Timer 0, channel 0.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P2[4]/PWM1[5]/ DSR1/TRACESYNC	69[1]	I/O	**P2[4] —** General purpose digital input/output pin.
		O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
		I	**DSR1 —** Data Set Ready input for UART1.
		O	**TRACESYNC —** Trace Synchronization.
P2[5]/PWM1[6]/ DTR1/TRACEPKT0	68[1]	I/O	**P2[5] —** General purpose digital input/output pin.
		O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
		O	**DTR1 —** Data Terminal Ready output for UART1.
		O	**TRACEPKT0 —** Trace Packet, bit 0.
P2[6]/PCAP1[0]/RI1/ TRACEPKT1	67[1]	I/O	**P2[6] —** General purpose digital input/output pin.
		I	**PCAP1[0] —** Capture input for PWM1, channel 0.
		I	**RI1 —** Ring Indicator input for UART1.
		O	**TRACEPKT1 —** Trace Packet, bit 1.
P2[7]/RD2/ RTS1/TRACEPKT2	66[1]	I/O	**P2[7] —** General purpose digital input/output pin.
		I	**RD2 —** CAN2 receiver input.
		O	**RTS1 —** Request to Send output for UART1.
		O	**TRACEPKT2 —** Trace Packet, bit 2.
P2[8]/TD2/ TXD2/TRACEPKT3	65[1]	I/O	**P2[8] —** General purpose digital input/output pin.
		O	**TD2 —** CAN2 transmitter output.
		O	**TXD2 —** Transmitter output for UART2.
		O	**TRACEPKT3 —** Trace Packet, bit 3.
P2[9]/ USB_CONNECT/ RXD2/EXTIN0	64[1]	I/O	**P2[9] —** General purpose digital input/output pin.
		O	**USB_CONNECT —** Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
		I	**RXD2 —** Receiver input for UART2.
		I	**EXTIN0 —** External Trigger Input.
P2[10]/$\overline{\text{EINT0}}$	53[6]	I/O	**P2[10] —** General purpose digital input/output pin. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip bootloader to take over control of the part after a reset.
		I	**$\overline{\text{EINT0}}$ —** External interrupt 0 input.
P2[11]/$\overline{\text{EINT1}}$/ MCIDAT1/ I2STX_CLK	52[6]	I/O	**P2[11] —** General purpose digital input/output pin.
		I	**$\overline{\text{EINT1}}$ —** External interrupt 1 input.
		O	**MCIDAT1 —** Data line for SD/MMC interface.
		I/O	**I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
P2[12]/$\overline{\text{EINT2}}$/ MCIDAT2/ I2STX_WS	51[6]	I/O	**P2[12] —** General purpose digital input/output pin.
		I	**$\overline{\text{EINT2}}$ —** External interrupt 2 input.
		O	**MCIDAT2 —** Data line for SD/MMC interface.
		I/O	**I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.

FIQs have the highest priority. If more than one request is assigned to FIQ, the VIC ORs the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs, which include all interrupt requests that are not classified as FIQs, have a programmable interrupt priority. When more than one interrupt is assigned the same priority and occur simultaneously, the one connected to the lowest numbered VIC channel will be serviced first.

The VIC ORs the requests from all of the vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping to the address supplied by that register.

7.5.1 Interrupt sources

Each peripheral device has one interrupt line connected to the VIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any pin on port 0 and port 2 (total of 42 pins) regardless of the selected function, can be programmed to generate an interrupt on a rising edge, a falling edge, or both. Such interrupt request coming from port 0 and/or port 2 will be combined with the $\overline{\text{EINT3}}$ interrupt requests.

7.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.7 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected LPC2387 peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receive. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the AHB master.

7.7.1 Features

- Two DMA channels. Each channel can support a unidirectional transfer.
- The GPDMA can transfer data between the 16 kB SRAM and peripherals such as the SD/MMC, two SSP, and I^2S interfaces.

Additionally, any pin on port 0 and port 2 (total of 42 pins) providing a digital function can be programmed to generate an interrupt on a rising edge, a falling edge, or both. The edge detection is asynchronous, so it may operate when clocks are not present such as during Power-down mode. Each enabled interrupt can be used to wake up the chip from Power-down mode.

7.8.1 Features

- Bit level set and clear registers allow a single instruction to set or clear any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- Backward compatibility with other earlier devices is maintained with legacy port 0 and port 1 registers appearing at the original addresses on the APB.

7.9 Ethernet

The Ethernet block contains a full featured 10 Mbit/s or 100 Mbit/s Ethernet MAC designed to provide optimized performance through the use of DMA hardware acceleration. Features include a generous suite of control registers, half or full duplex operation, flow control, control frames, hardware acceleration for transmit retry, receive packet filtering and wake-up on LAN activity. Automatic frame transmission and reception with scatter-gather DMA off-loads many operations from the CPU.

The Ethernet block and the CPU share a dedicated AHB subsystem that is used to access the Ethernet SRAM for Ethernet data, control, and status information. All other AHB traffic in the LPC2387 takes place on a different AHB subsystem, effectively separating Ethernet activity from the rest of the system. The Ethernet DMA can also access the USB SRAM if it is not being used by the USB block.

The Ethernet block interfaces between an off-chip Ethernet PHY using the Reduced MII (RMII) protocol and the on-chip Media Independent Interface Management (MIIM) serial bus.

7.9.1 Features

- Ethernet standards support:
  - Supports 10 Mbit/s or 100 Mbit/s PHY devices including 10 Base-T, 100 Base-TX, 100 Base-FX, and 100 Base-T4.
  - Fully compliant with IEEE standard 802.3.
  - Fully compliant with 802.3x full duplex flow control and half duplex back pressure.
  - Flexible transmit and receive frame options.
  - Virtual Local Area Network (VLAN) frame support.
- Memory management:
  - Independent transmit and receive buffers memory mapped to shared SRAM.
  - DMA managers with scatter/gather DMA and arrays of frame descriptors.
  - Memory traffic optimized by buffering and pre-fetching.
- Enhanced Ethernet features:

7.17 SD/MMC card interface

The Secure Digital and Multimedia Card Interface (MCI) allows access to external SD memory cards. The SD card interface conforms to the *SD Multimedia Card Specification Version 2.11*.

7.17.1 Features

- The MCI provides all functions specific to the SD/MMC memory card. These include the clock generation unit, power management control, and command and data transfer.
- Conforms to *Multimedia Card Specification v2.11*.
- Conforms to *Secure Digital Memory Card Physical Layer Specification, v0.96.*
- Can be used as a multimedia card bus or a secure digital memory card bus host. The SD/MMC can be connected to several multimedia cards or a single secure digital memory card.
- DMA supported through the GPDMA controller.

7.18 I^2C-bus serial I/O controllers

The LPC2387 contains three I^2C-bus controllers.

The I^2C-bus is bidirectional, for inter-IC control using only two wires: a Serial CLock line (SCL), and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I^2C-bus implemented in LPC2387 supports bit rates up to 400 kbit/s (Fast I^2C-bus).

7.18.1 Features

- I^2C0 is a standard I^2C compliant bus interface with open-drain pins.
- I^2C1 and I^2C2 use standard I/O pins and do not support powering off of individual devices connected to the same bus lines.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.

The LPC2387 also implements a separate power domain in order to allow turning off power to the bulk of the device while maintaining operation of the RTC and a small SRAM, referred to as the battery RAM.

7.24.4.1 Idle mode

In Idle mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.24.4.2 Sleep mode

In Sleep mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Sleep mode and the logic levels of chip pins remain static. The output of the IRC is disabled but the IRC is not powered down for a fast wake-up later. The 32 kHz RTC oscillator is not stopped because the RTC interrupts may be used as the wake-up source. The PLL is automatically turned off and disconnected. The CCLK and USB clock dividers automatically get reset to zero.

The Sleep mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Sleep mode reduces chip power consumption to a very low value. The flash memory is left on in Sleep mode, allowing a very quick wake-up.

On the wake-up of Sleep mode, if the IRC was used before entering Sleep mode, the code execution and peripherals activities will resume after 4 cycles expire. If the main external oscillator was used, the code execution will resume when 4096 cycles expire.

The customers need to reconfigure the PLL and clock dividers accordingly.

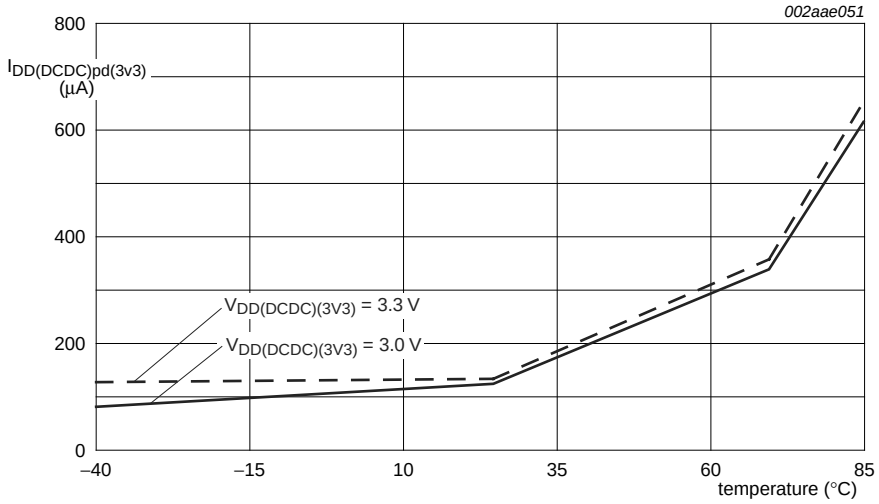
7.24.4.3 Power-down mode

Power-down mode does everything that Sleep mode does, but also turns off the IRC oscillator and the flash memory. This saves more power, but requires waiting for resumption of flash operation before execution of code or data access in the flash memory can be accomplished.

On the wake-up of Power-down mode, if the IRC was used before entering Power-down mode, it will take IRC 60 μs to start-up. After this 4 IRC cycles will expire before the code execution can then be resumed if the code was running from SRAM. In the meantime, the flash wake-up timer then counts 4 MHz IRC clock cycles to make the 100 μs flash start-up time. When it times out, access to the flash will be allowed. The customers need to reconfigure the PLL and clock dividers accordingly.

7.24.4.4 Deep power-down mode

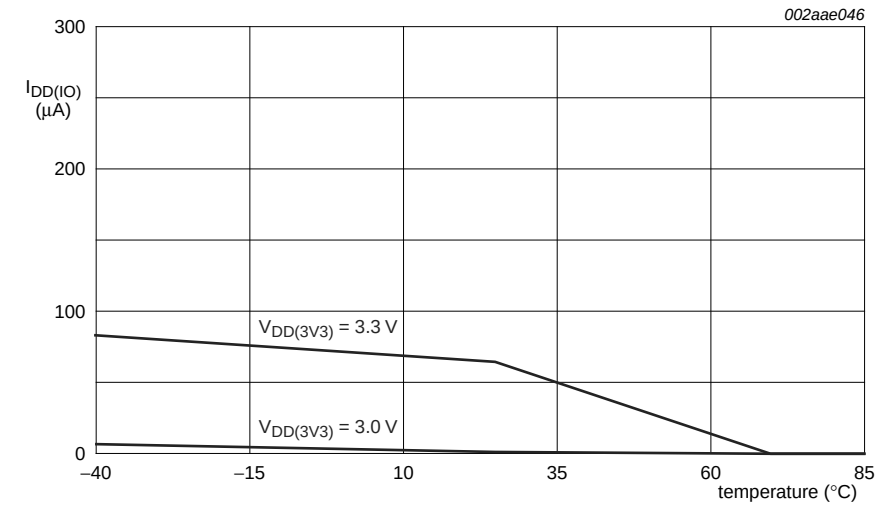
Deep power-down mode is similar to the Power-down mode, but now the on-chip regulator that supplies power to the internal logic is also shut off. This produces the lowest possible power consumption without removing power from the entire chip. Since the Deep power-down mode shuts down the on-chip logic power supply, there is no register or memory retention, and resumption of operation involves the same activities as a full chip reset.



$V_{DD(3V3)} = V_{i(VBAT)} = 3.3$ V; $T_{amb} = 25$ °C.

Fig 6. Total DC-to-DC converter supply current $I_{DD(DCDC)pd(3V3)}$ at different temperatures in Power-down mode

10.2 Deep power-down mode



$V_{DD(3V3)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C.

Fig 7. I/O maximum supply current $I_{DD(IO)}$ versus temperature in Deep power-down mode

12. ADC electrical characteristics

Table 13. ADC electrical characteristics

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error		[1][2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		[1][4]	-	-	±2	LSB
E_O	offset error		[1][5]	-	-	±3	LSB
E_G	gain error		[1][6]	-	-	±0.5	%
E_T	absolute error		[1][7]	-	-	±4	LSB
R_{vsi}	voltage source interface resistance		[8]	-	-	40	kΩ

[1] Conditions: V_{SSA} = 0 V, V_{DDA} = 3.3 V.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 15.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 15.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 15.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 15.

[7] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 15.

[8] See Figure 16.

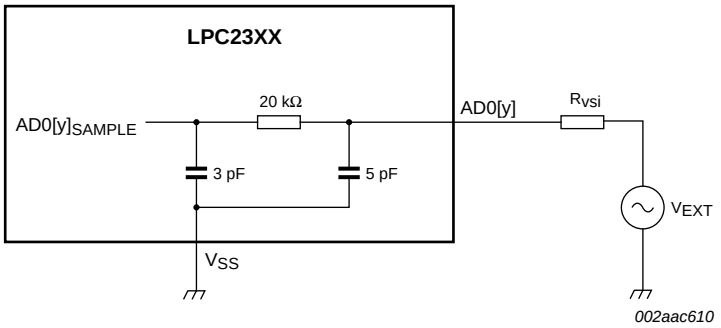


Fig 16. Suggested ADC interface - LPC2387 AD0[y] pin

13. DAC electrical characteristics

Table 14. DAC electrical characteristics

V_{DDA} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
E_D	differential linearity error		-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity		-	±1.5	-	LSB
E_O	offset error		-	0.6	-	%
E_G	gain error		-	0.6	-	%
C_L	load capacitance		-	200	-	pF
R_L	load resistance		1	-	-	kΩ

14. Application information

14.1 Suggested USB interface solutions

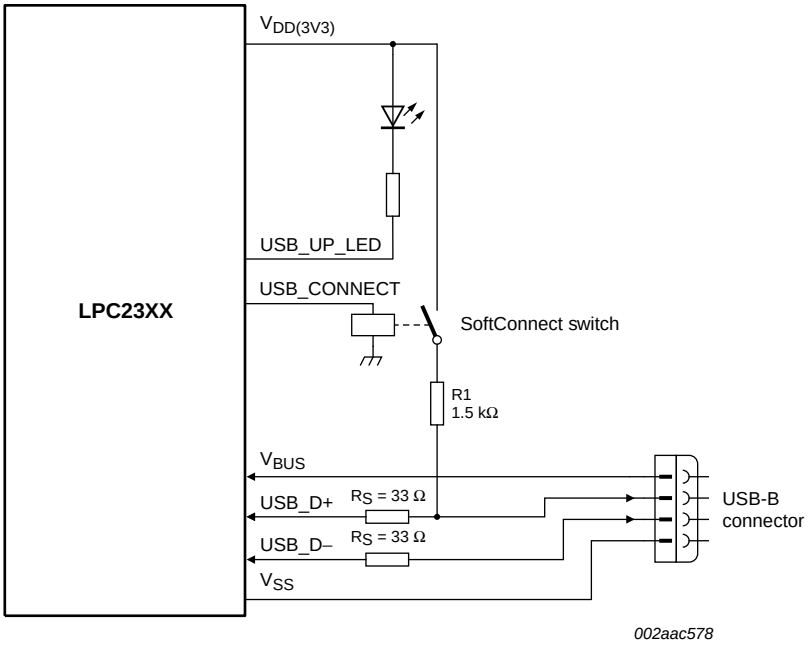


Fig 17. LPC2387 USB interface on a self-powered device

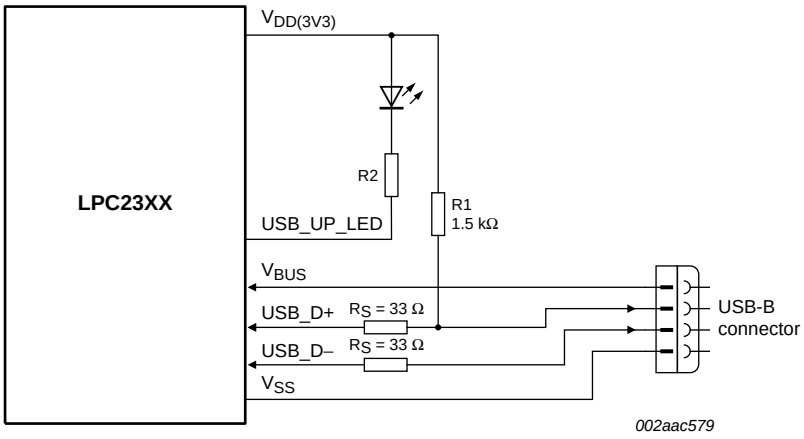


Fig 18. LPC2387 USB interface on a bus-powered device

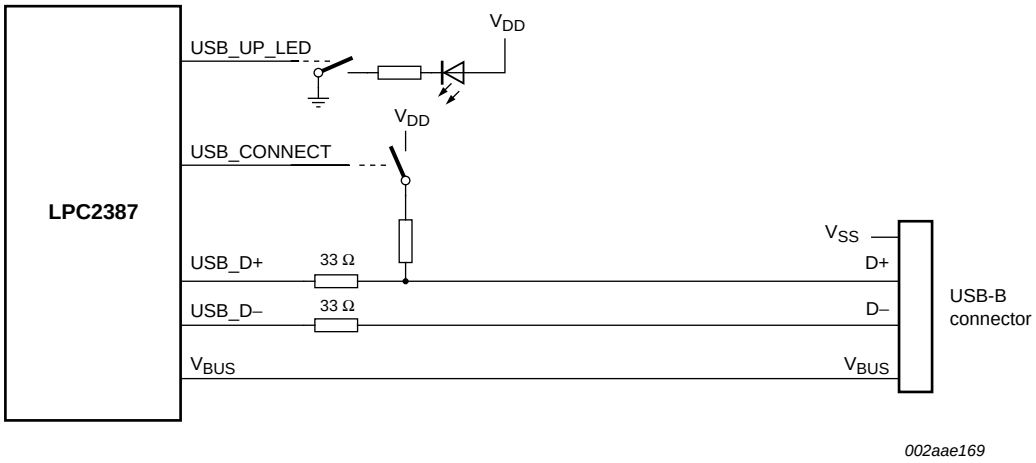


Fig 21. LPC2387 USB device port configuration

14.2 Crystal oscillator XTAL input and component selection

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i / (C_i + C_g)$. In slave mode, a minimum of 200 mV (RMS) is needed.

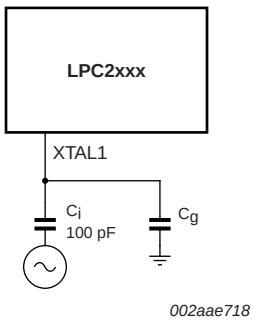


Fig 22. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 22), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTAL2 pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 23 and in Table 15 and Table 16. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 23 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer.

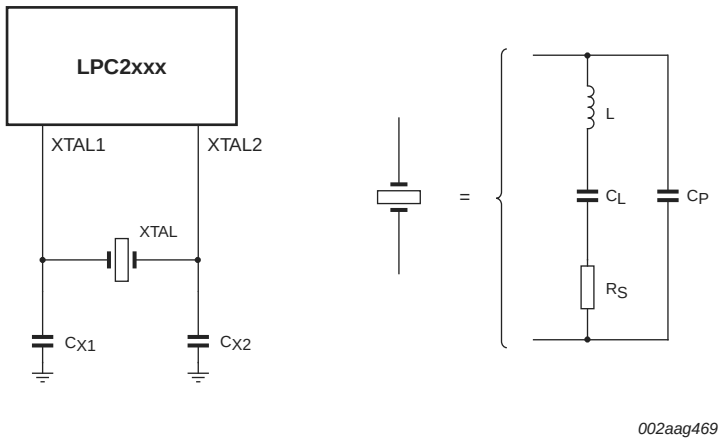


Fig 23. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 15. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 16. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

14.5 Standard I/O pin configuration

Figure 25 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Analog input (for ADC input channels)

The default configuration for standard I/O pins is input with pull-up enabled. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.

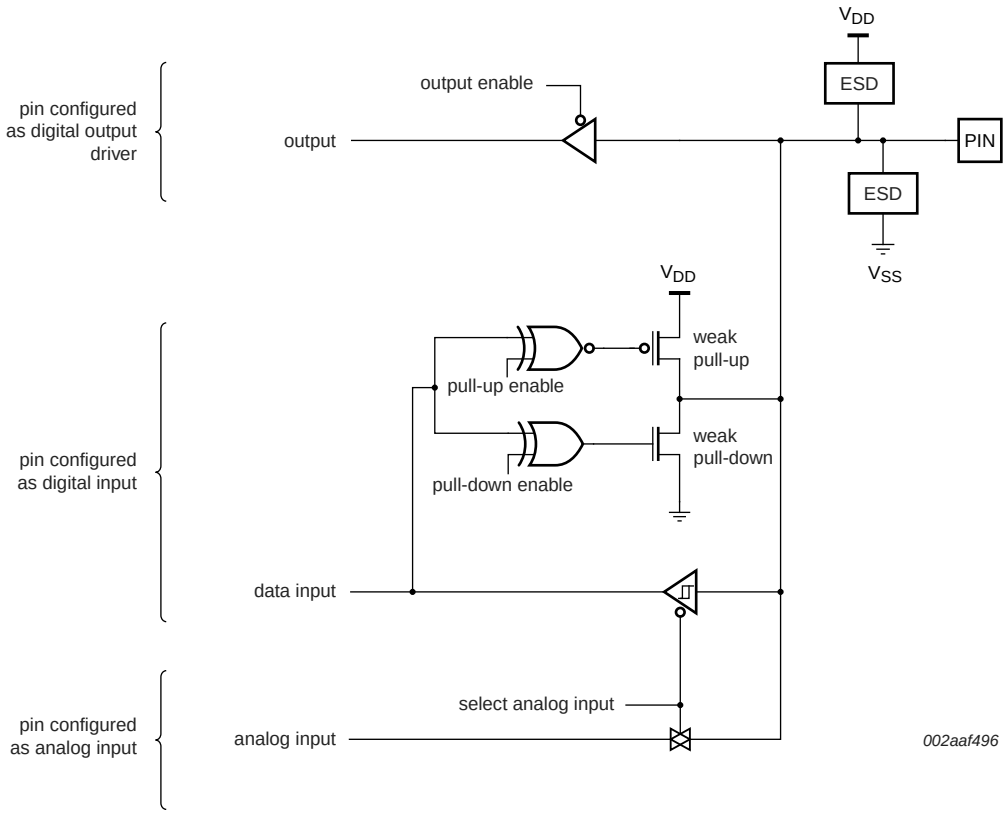
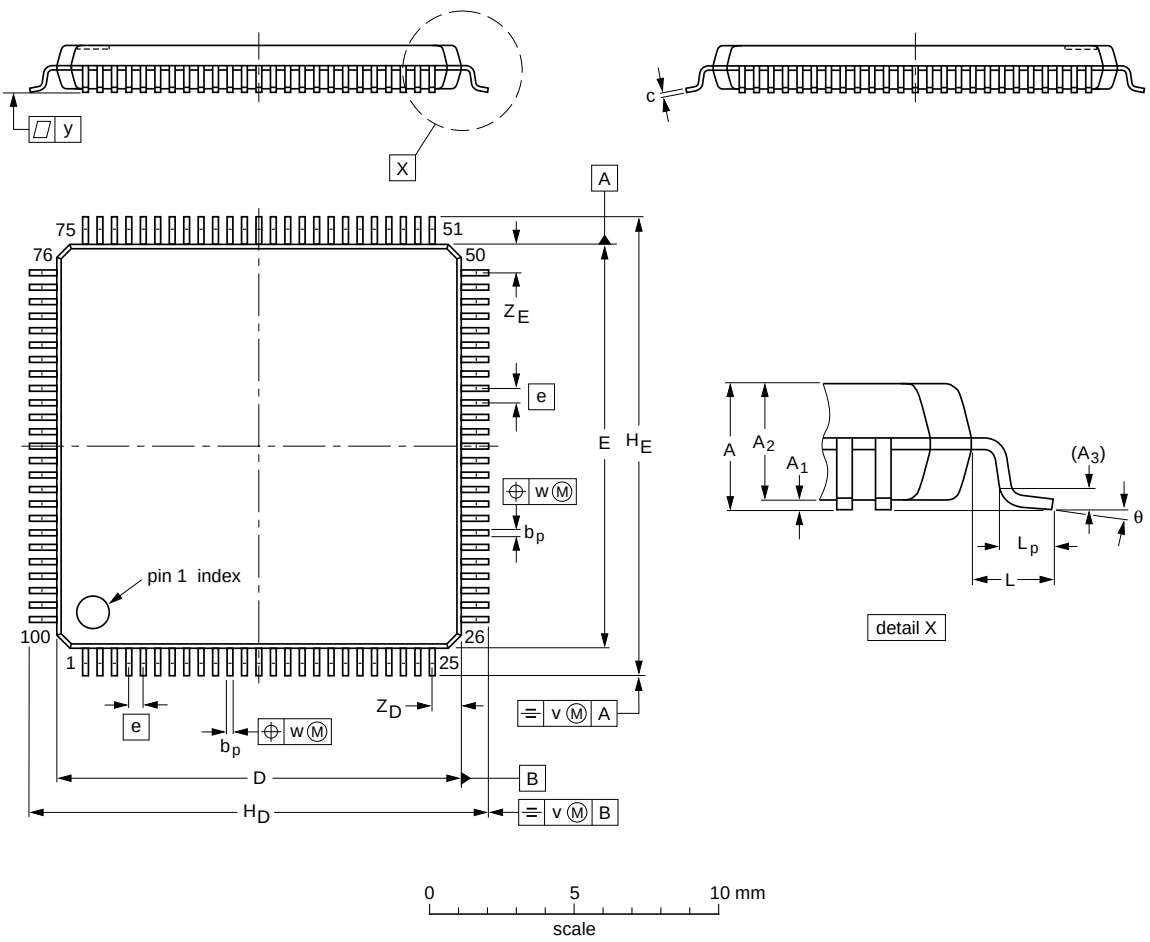


Fig 25. Standard I/O pin configuration with analog input

15. Package outline

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 27. Package outline SOT407-1 (LQFP100)

16. Abbreviations

Table 18. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DCC	Debug Communication Channel
DMA	Direct Memory Access
DSP	Digital Signal Processing
EOP	End Of Packet
ETM	Embedded Trace Macrocell
GP	General Purpose
GPIO	General Purpose Input/Output
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
MII	Media Independent Interface
MIIM	Media Independent Interface Management
PHY	Physical Layer
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RMII	Reduced Media Independent Interface
SE0	Single Ended Zero
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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