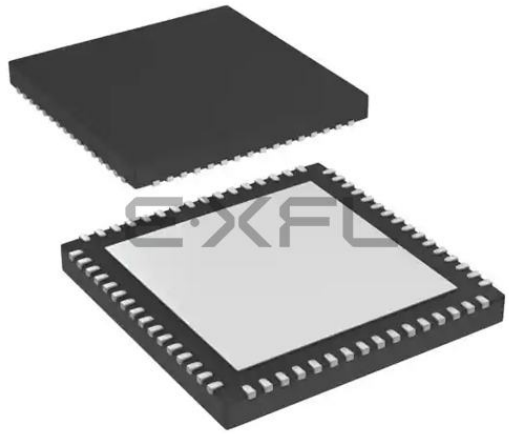

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Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	30
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-HVQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f36b3ednp-u0

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

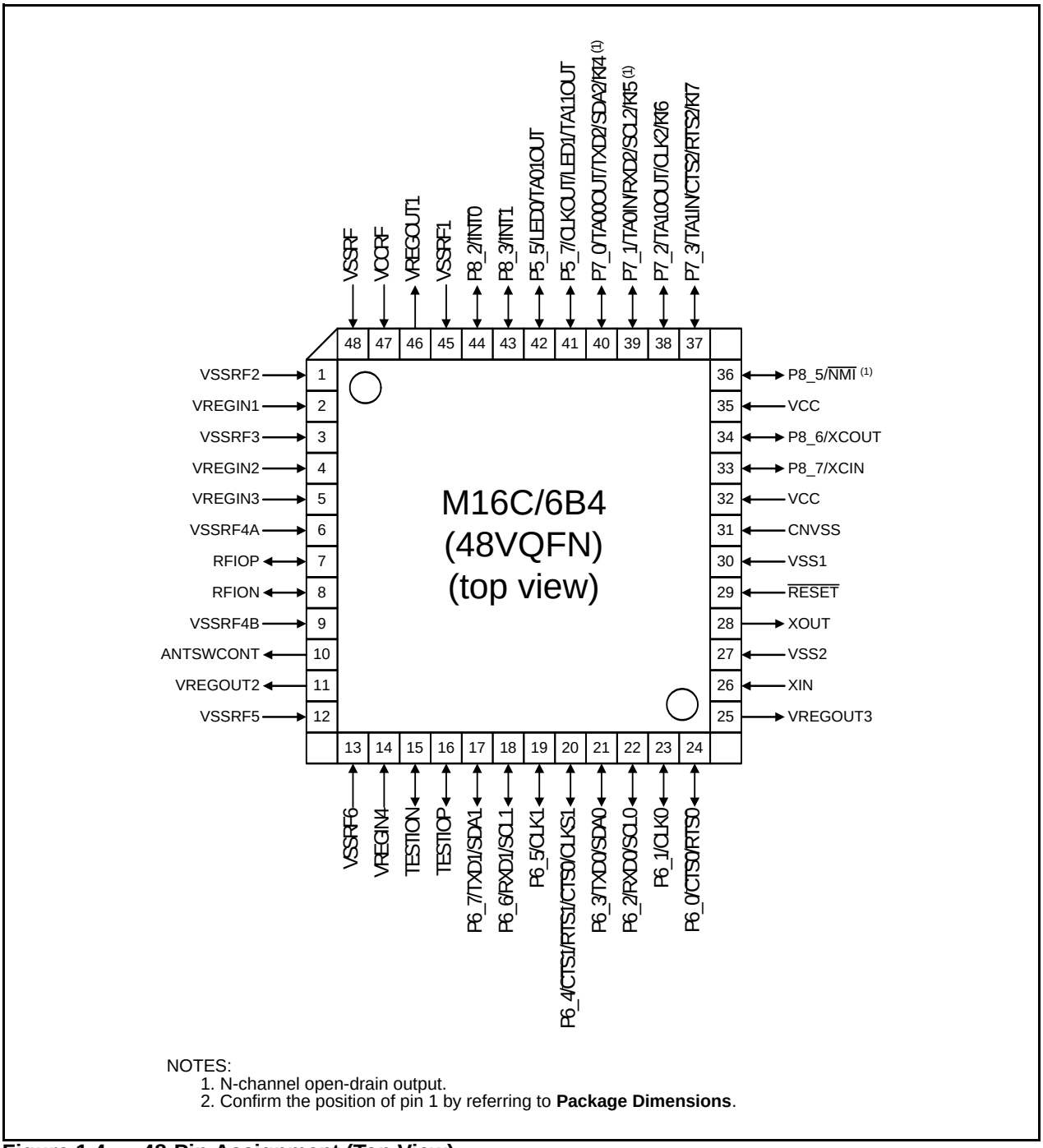
(1) Register Names, Bit Names, and Pin Names
Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word "register," "bit," or "pin" to distinguish the three categories.
Examples the PM03 bit in the PM0 register
P3_5 pin, VCC pin

(2) Notation of Numbers
The indication "b" is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication "h" is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.
Examples Binary: 11b
Hexadecimal: EFA0h
Decimal: 1234

Address	Register	Symbol	Page
0188h	DMA0 Transfer Counter	TCR0	92
0189h			
018Ah			
018Bh			
018Ch	DMA0 Control Register	DM0CON	91
018Dh			
018Eh			
018Fh			
0190h	DMA1 Source Pointer	SAR1	91
0191h			
0192h			
0193h			
0194h	DMA1 Destination Pointer	DAR1	92
0195h			
0196h			
0197h			
0198h	DMA1 Transfer Counter	TCR1	92
0199h			
019Ah			
019Bh			
019Ch	DMA1 Control Register	DM1CON	91
019Dh			
019Eh			
019Fh			
01A0h	DMA2 Source Pointer	SAR2	91
01A1h			
01A2h			
01A3h			
01A4h	DMA2 Destination Pointer	DAR2	92
01A5h			
01A6h			
01A7h			
01A8h	DMA2 Transfer Counter	TCR2	92
01A9h			
01AAh			
01ABh			
01ACh	DMA2 Control Register	DM2CON	91
01ADh			
01AEh			
01AFh			
01B0h	DMA3 Source Pointer	SAR3	91
01B1h			
01B2h			
01B3h			
01B4h	DMA3 Destination Pointer	DAR3	92
01B5h			
01B6h			
01B7h			
01B8h	DMA3 Transfer Counter	TCR3	92
01B9h			
01BAh			
01BBh			
01BCh	DMA3 Control Register	DM3CON	91
01BDh			
01BEh			
01BFh			
01C0h			
01C1h			
01C2h			
01C3h			
01C4h			
01C5h			
01C6h			
01C7h			
01C8h	Timer B Count Source Select Register 0	TBCS0	123
01C9h	Timer B Count Source Select Register 1	TBCS1	123
01CAh			
01CBh			

Address	Register	Symbol	Page
01CCh			
01CDh			
01CEh			
01CFh			
01D0h	Timer A Count Source Select Register 0	TACS0	107
01D1h	Timer A Count Source Select Register 1	TACS1	107
01D2h	Timer A Count Source Select Register 2	TACS2	108
01D3h			
01D4h			
01D5h	Timer A Waveform Output Function Select Register	TAPOFS	108
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DEh			
01DCh			
01DDh			
01DFh			
01E0h			
01E1h			
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h	Timer B Count Source Select Register 2	TBCS2	123
01E9h	Timer B Count Source Select Register 3	TBCS3	123
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h			
01F1h			
01F2h			
01F3h			
01F4h			
01F5h			
01F6h			
01F7h			
01F8h			
01F9h			
01FAh			
01FBh			
01FCh			
01FDh			
01FEh			
01FFh			
0200h			
0201h			
0202h			
0203h			
0204h			
0205h			
0206h	Interrupt Source Select Register 2	IFSR2A	76
0207h	Interrupt Source Select Register	IFSR	76
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh	Address Match Interrupt Enable Register	AIER	81
020Fh	Address Match Interrupt Enable Register 2	AIER2	81

Blank columns are all reserved space. No access is allowed.



NOTES:
1. N-channel open-drain output.
2. Confirm the position of pin 1 by referring to **Package Dimensions**.

Figure 1.4 48-Pin Assignment (Top View)

Table 4.14 SFR Information (14) (1)

Address	Register	Symbol	After Reset
03DAh			
03DBh			
03DCh			
03DDh			
03DEh			
03DFh			
03E0h			
03E1h			
03E2h			
03E3h			
03E4h			
03E5h			
03E6h			
03E7h			
03E8h			
03E9h	Port P5 Register	P5	XXh
03EAh			
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h
03F0h	Port P8 Register	P8	XXh
03F1h			
03F2h	Port P8 Direction Register	PD8	00h
03F3h			
03F4h	Port P10 Register (2)	P10	XXh
03F5h			
03F6h	Port P10 Direction Register (2)	PD10	00h
03F7h			
03F8h			
03F9h			
03FAh			
03FBh			
03FCh			
03FDh			
03FEh			
03FFh			
D000h to D09Fh			
D100h to D17Eh	Transmit RAM	TRANSMIT_RAM_START TRANSMIT_RAM_END	
D17Fh			
D180h to D1FEh	Receive RAM	RECIEVE_RAM_START RECIEVE_RAM_END	
D1FFh to D7FFh			

FFFFFh	Option Function Select Address	OFS1	(NOTE 3)

NOTES: X: Undefined

1. The blank areas are reserved and cannot be accessed by users.
2. Reserved area in the 48-pin version. No access is allowed.
3. The OFS1 address is set to FFh when a block including the OFS1 address is erased.

5.5 Internal Space

Figure 5.3 shows CPU Register Status After Reset. Refer to **4. "Special Function Registers (SFRs)"** for SFR states after reset.

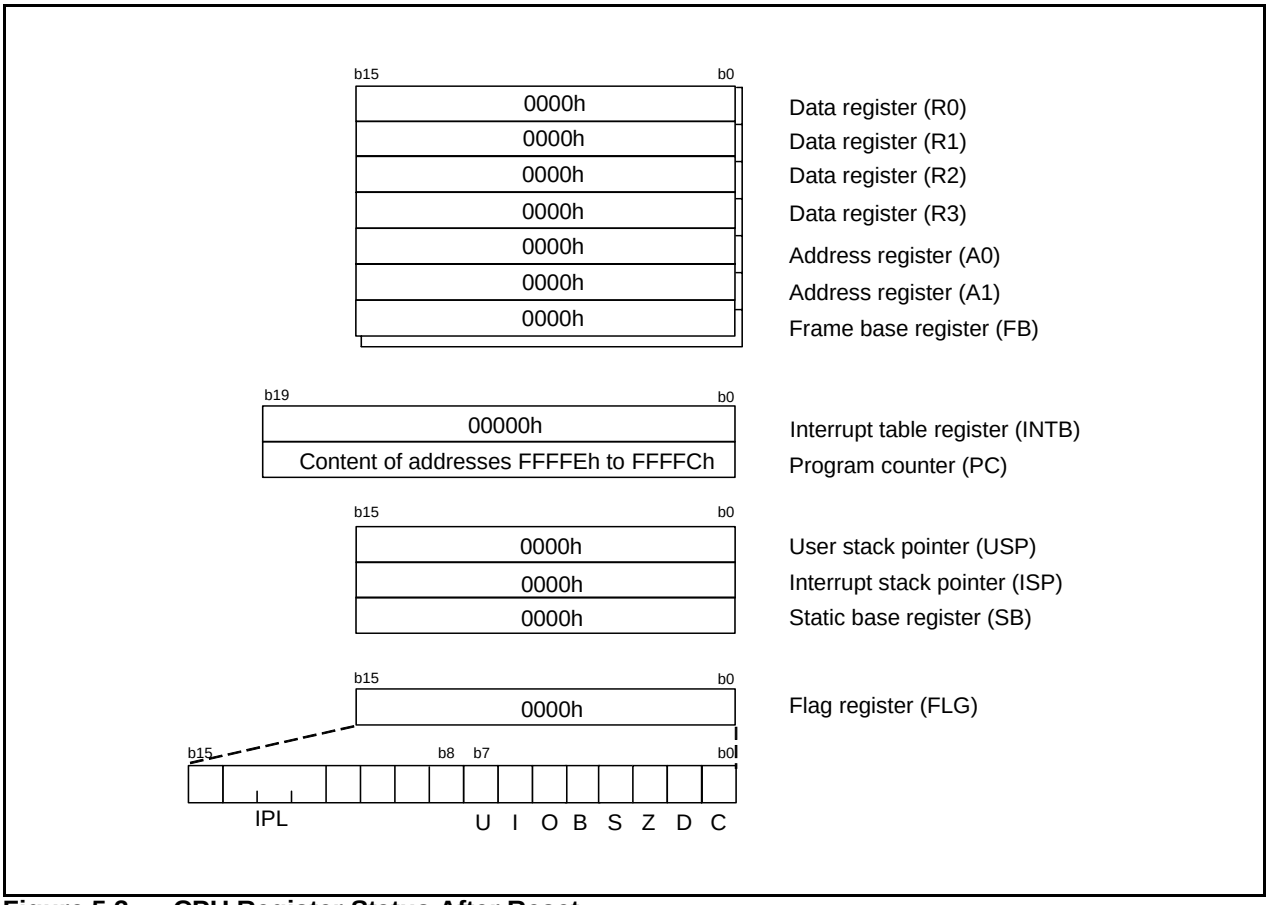


Figure 5.3 CPU Register Status After Reset

6. Processor Mode

6.1 Types of Processor Mode

Three processor modes are available to choose from: single-chip mode. Table 6.1 lists the Features of Processor Modes.

Table 6.1 Features of Processor Modes

Processor Modes	Access Space	Pins Which Are Assigned I/O Ports
Single-chip mode	SFR, internal RAM, internal ROM	All pins are I/O ports or peripheral function I/O pins

6.2 Setting Processor Modes

Processor mode is set by using the CNVSS pin.
Table 6.2 lists the Processor Mode After Hardware Reset.

Table 6.2 Processor Mode After Hardware Reset

CNVSS Pin Input Level	Processor Modes
VSS	Single-chip mode

Figures 6.1 to 6.3 show the processor mode associated registers. Figure 6.4 show the Memory Map in Single-Chip Mode.

Processor Mode Register 0 (1)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0		0		

Symbol	Address	After Reset
PM0	0004h	00000000b

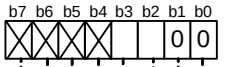
Bit Symbol	Bit Name	Function	RW
PM00	Processor mode bit (2)	b1 b0 0 0: Single-chip mode Other than above: Do not set	RW
PM01			RW
— (b2)	Reserved bit	Set to 0	RW
PM03	Software reset bit	Setting this bit to 1 resets the microcomputer. Read as 0.	RW
— (b7-b4)	Reserved bits	Set to 0	RW

NOTES:
1. Write to this register after setting the PRC1 bit in the PRCR register to 1 (write enabled).
2. Bits PM01 and PM00 do not change at software reset, watchdog timer reset, and oscillation stop detection reset.

Figure 6.1 PM0 Register

7.4.4.2 Flash Memory Control Register 2 (FMR2)

Flash Memory Control Register 2



Symbol: FMR2 | Address: 0222h | After Reset: XXXX0000b

Bit Symbol	Bit Name	Function	RW
— (b1-b0)	Reserved bits	Set to 0	RW
FMR22	Slow read mode enable bit	0: Disabled 1: Enabled	RW
FMR23	Low-current consumption read mode enable bit	0: Disabled 1: Enabled	RW
— (b7-b4)	No register bits. If necessary, set to 0. Read as undefined value.		—

FMR22 (Slow read mode enable bit) (b2)

This bit enables mode which reduces the amount of current consumption when reading the flash memory. When rewriting the flash memory (CPU rewrite mode), set the FMR22 bit to 0 (slow read mode disabled).
To set the FMR22 bit to 1, write 0 and then 1 in succession. Make sure no interrupts or DMA transfers occur before writing 1 and after writing 0.
Set the FMR23 bit to 1 (low current consumption read mode enabled) after the FMR22 bit is set to 1 (slow read mode enabled). Also, set the FMR22 bit to 0 (slow read mode disabled) after the FMR23 bit is set to 0 (slow read mode disabled). Do not change bits FMR22 and FMR23 at the same time.

FMR23 (Low current consumption read mode enable bit) (b3)

When this bit is set, the slow read mode reduces the amount of current consumption when reading the flash memory. When rewriting the flash memory (CPU rewrite mode), set the FMR23 bit to 0 (low current consumption read mode disabled).
Low current consumption read mode can be used when the CM07 bit in the CM0 register is 1 (sub clock used as CPU clock). When the CM07 bit is 0, set the FMR23 bit to 0 (low current consumption read mode disabled).
To set the FMR23 bit to 1, write 0 and then 1 in succession. Make sure no interrupts or DMA transfers occur before writing 1 and after writing 0.
Set the FMR23 bit to 1 (low current consumption read mode enabled) after the FMR22 bit is set to 1 (slow read mode enabled). Also, set the FMR22 bit to 0 (slow read mode disabled) after the FMR23 bit is set to 0 (slow read mode disabled). Do not change bits FMR22 and FMR23 at the same time.
When the FMR23 bit is 1, do not set the FMSTP bit in the FMR0 register to 1 (flash memory stopped). Also, when the FMSTP bit is 1, do not set the FMR23 bit to 1.
When the FMR23 bit in the FMR2 register is 1 (low current consumption read mode enabled), do not enter wait mode or stop mode. To enter wait mode or stop mode, set the FMR23 bit to 0 (low current consumption read mode disabled) before entering.

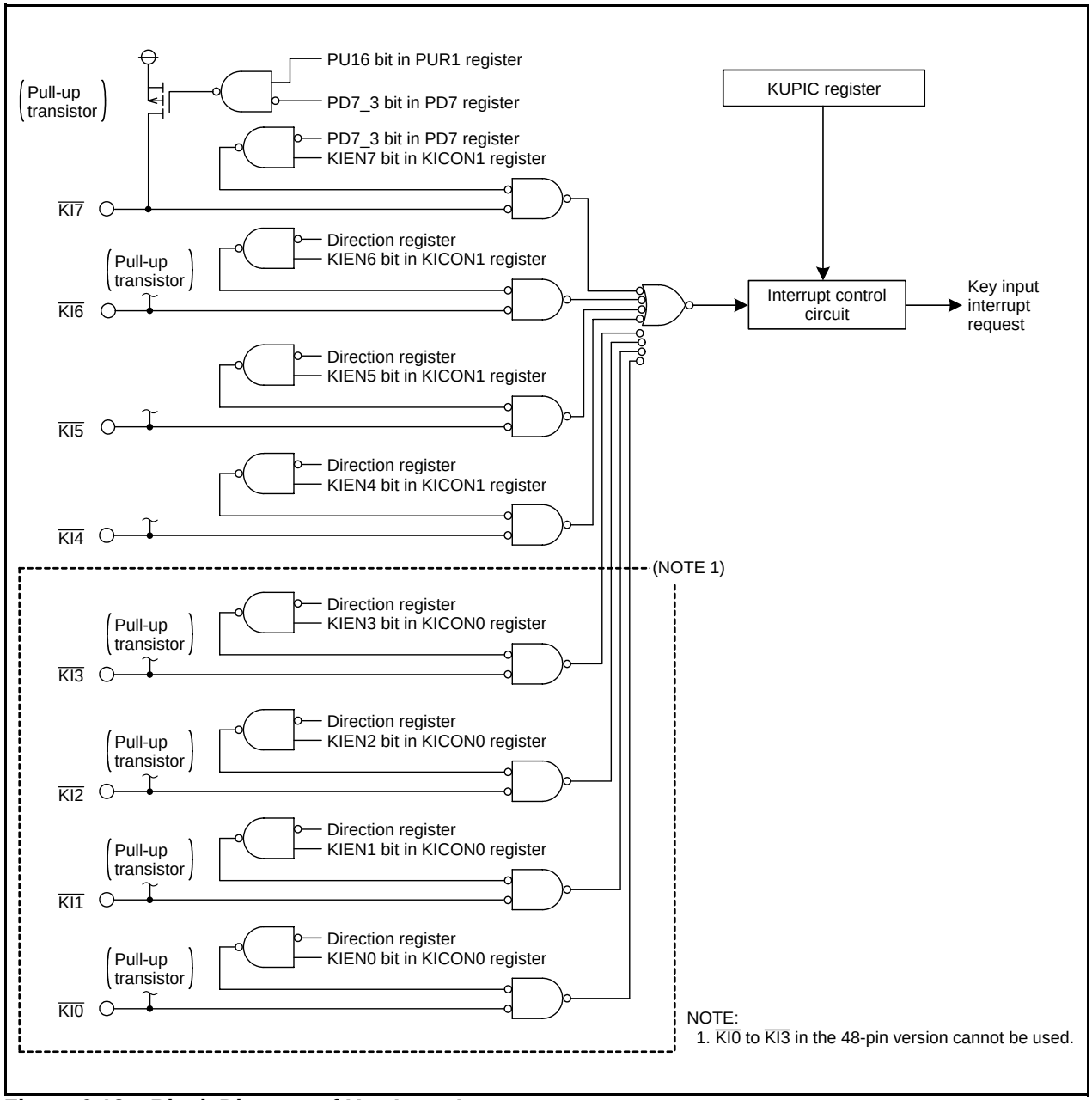


Figure 9.13 Block Diagram of Key Input Interrupt

Count Source Protection Mode Register

b7	b6	b5	b4	b3	b2	b1	b0
	0	0	0	0	0	0	0

Symbol	Address	After Reset (1)
CSPR	037Ch	00h

Bit Symbol	Bit Name	Function	RW
— (b6-b0)	Reserved bits	Set to 0	RW
CSPRO	Count source protection mode select bit (2)	0: Count source protection mode disabled 1: Count source protection mode enabled	RW

NOTES:
1. When a 0 is written to the CSPROINI bit in the OFS1 address, 10000000b is set after reset.
2. Write a 0 and then a 1 to set the CSPRO bit to 1. 0 cannot be set in a program.

Option Function Select Address (1)

b7	b6	b5	b4	b3	b2	b1	b0
	1	1	1		1	1	

Symbol	Address	After Reset
OFS1	FFFFFh	FFh (2)

Bit Symbol	Bit Name	Function	RW
WDTON	Watchdog timer start select bit (3)	0: Watchdog timer starts automatically after reset 1: Watchdog timer is in a stopped state after reset	RW
— (b2-b1)	Reserved bits	Set to 1	RW
ROMCP1	ROM code protection bit	0: ROM code protection enabled 1: ROM code protection disabled	RW
— (b6-b4)	Reserved bits	Set to 1	RW
CSPROINI	After-reset count source protection mode select bit (3)	0: Count source protection mode enabled after reset 1: Count source protection mode disabled after reset	RW

NOTES:
1. The OFS1 address exists in flash memory. Set the values when writing a program.
2. The OFS1 address is set to FFh when the block including the OFS1 address is erased.
3. Set the WDTON bit to 0 (watchdog timer starts automatically after reset) when setting the CSPROINI bit to 0 (count source protection mode enabled after reset).

Figure 10.3 CSPR Register and OFS1 Address

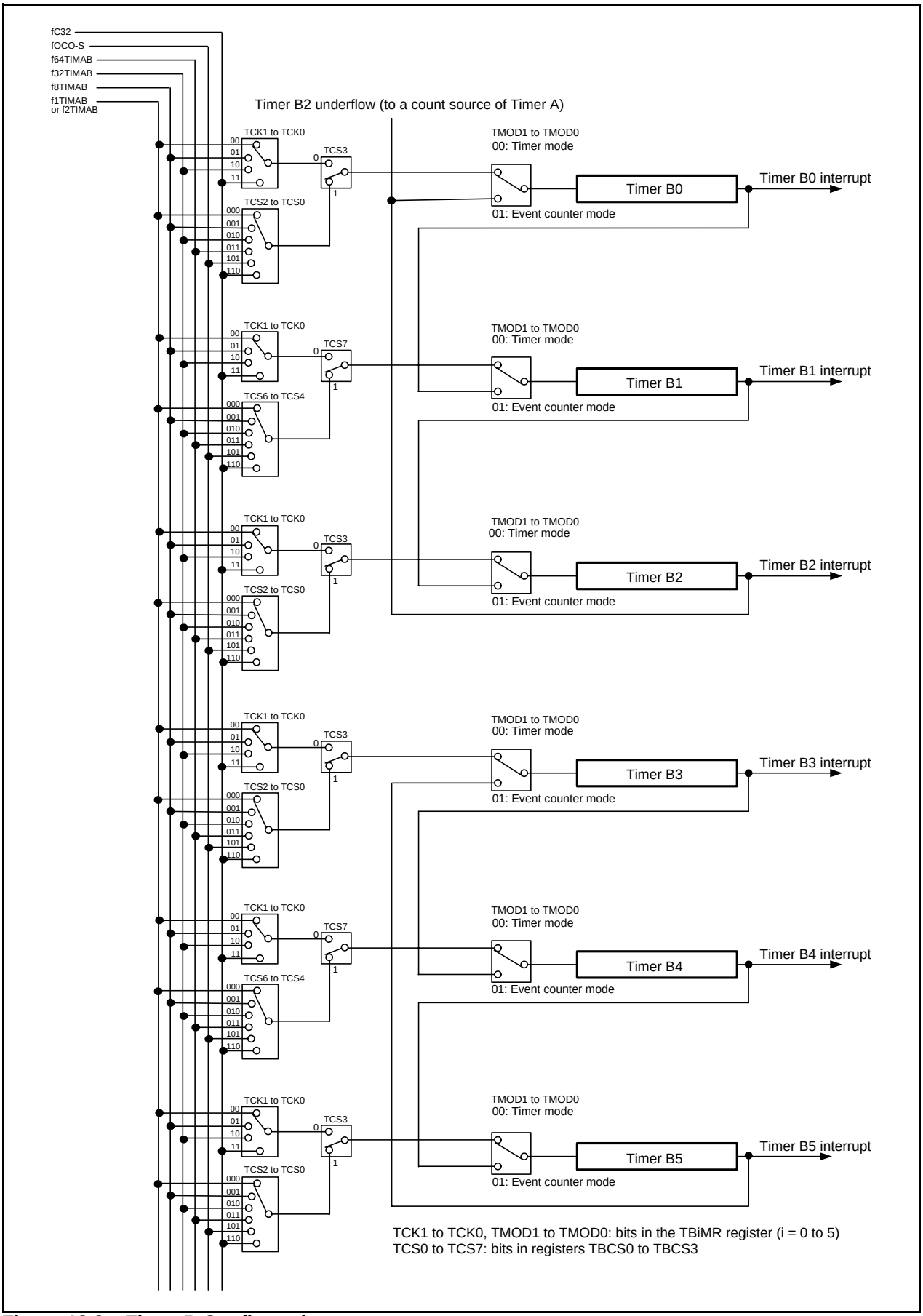


Figure 12.3 Timer B Configuration

Count Start Flag

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TABSR	0320h	00h

Bit Symbol	Bit Name	Function	RW
TA0S	Timer A0 count start flag	0: Stop counting 1: Start counting	RW
TA1S	Timer A1 count start flag		RW
TA2S	Timer A2 count start flag		RW
TA3S	Timer A3 count start flag		RW
TA4S	Timer A4 count start flag		RW
TB0S	Timer B0 count start flag		RW
TB1S	Timer B1 count start flag		RW
TB2S	Timer B2 count start flag		RW

Up/Down Flag

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
UDF	0324h	00h

Bit Symbol	Bit Name	Function	RW
TA0UD	Timer A0 up/down flag	0: Decrement 1: Increment Enabled during event counter mode (when not using two-phase pulse signal)	RW
TA1UD	Timer A1 up/down flag		RW
TA2UD	Timer A2 up/down flag		RW
TA3UD	Timer A3 up/down flag		RW
TA4UD	Timer A4 up/down flag		RW
TA2P	Timer A2 two-phase pulse signal processing select bit (3)	0: Two-phase pulse signal processing disabled 1: Two-phase pulse signal processing enabled (1, 2)	RW
TA3P	Timer A3 two-phase pulse signal processing select bit (3)		RW
TA4P	Timer A4 two-phase pulse signal processing select bit (3)		RW

NOTES:
1. Set the port direction bits for pins TA2IN to TA4IN and pins TA2OUT to TA4OUT to 0 (input mode).
2. When not using the two-phase pulse signal processing function, set the bit corresponding to Timer A2 to Timer A4 to 0.
3. 64-pin version only.

Figure 12.8 Registers TABSR and UDF

13.1.1.5 Serial Data Logic Switching Function

When the UiLCH bit in the UiC1 register (i = 0 to 2) = 1 (reverse), the data written to the UiTB register has its logic reversed before being transmitted. Similarly, the received data has its logic reversed when read from the UiRB register. Figure 13.18 shows Serial Data Logic Switching.

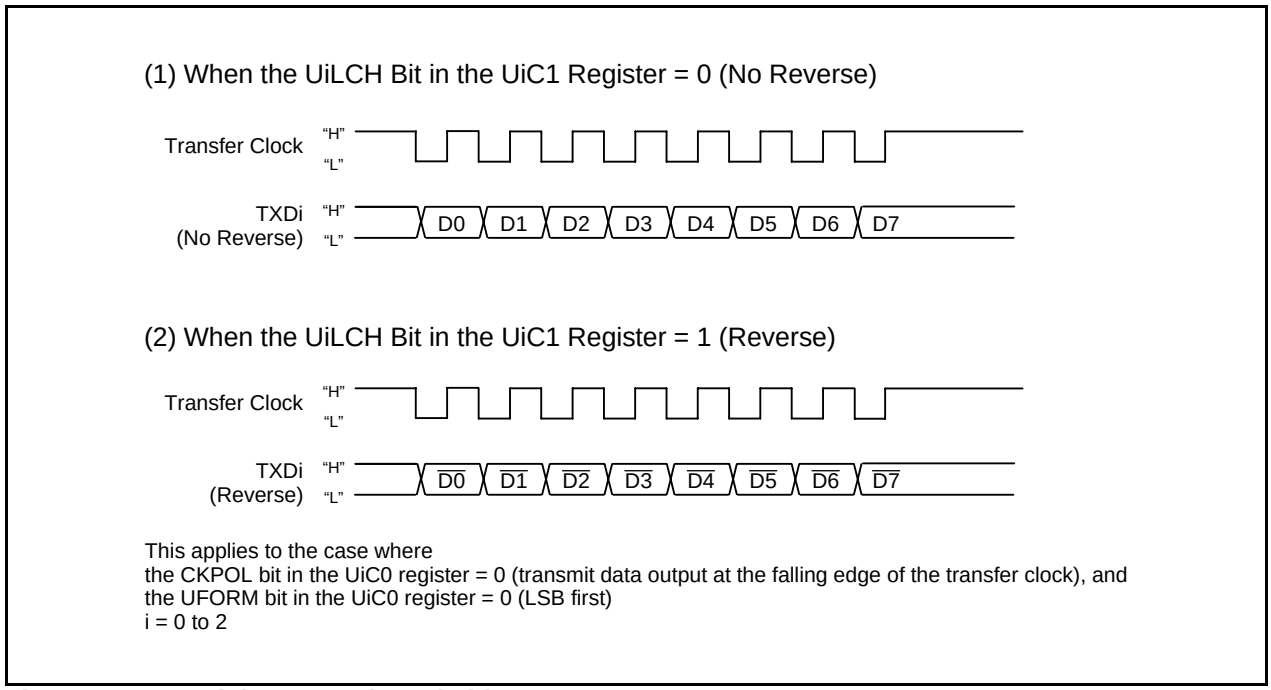


Figure 13.18 Serial Data Logic Switching

13.1.1.6 Transfer Clock Output from Multiple Pins (UART1)

Use bits CLKMD1 to CLKMD0 in the UCON register to select one of the two transfer clock output pins (refer to **Figure 13.19**). This function can be used when the selected transfer clock for UART1 is an internal clock.

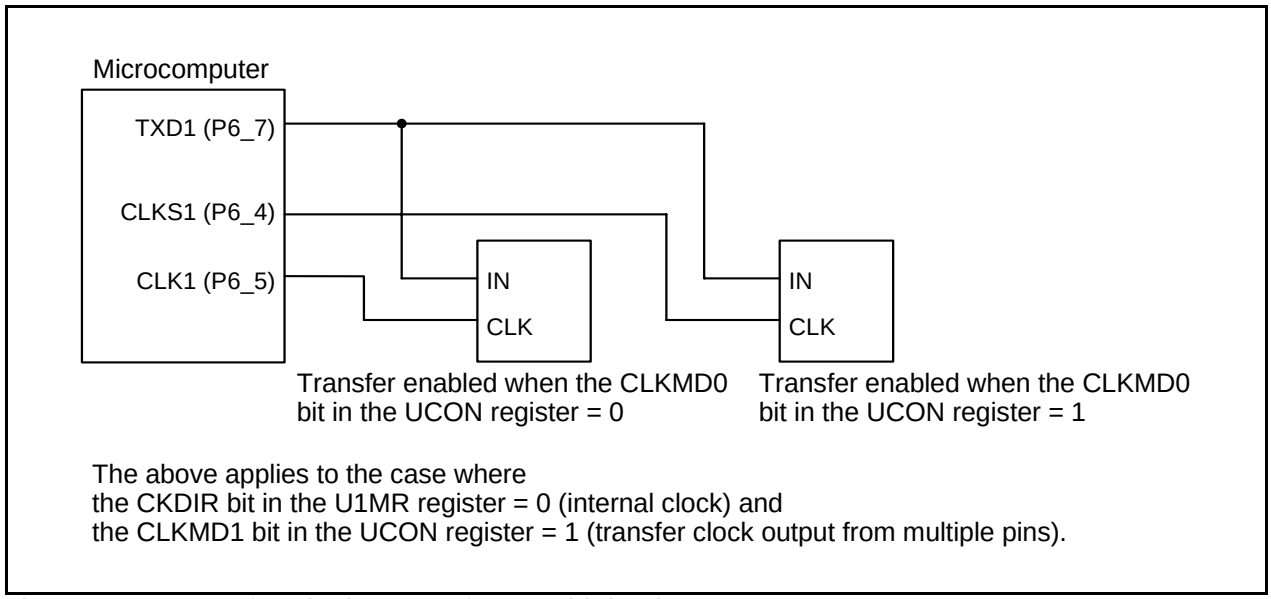
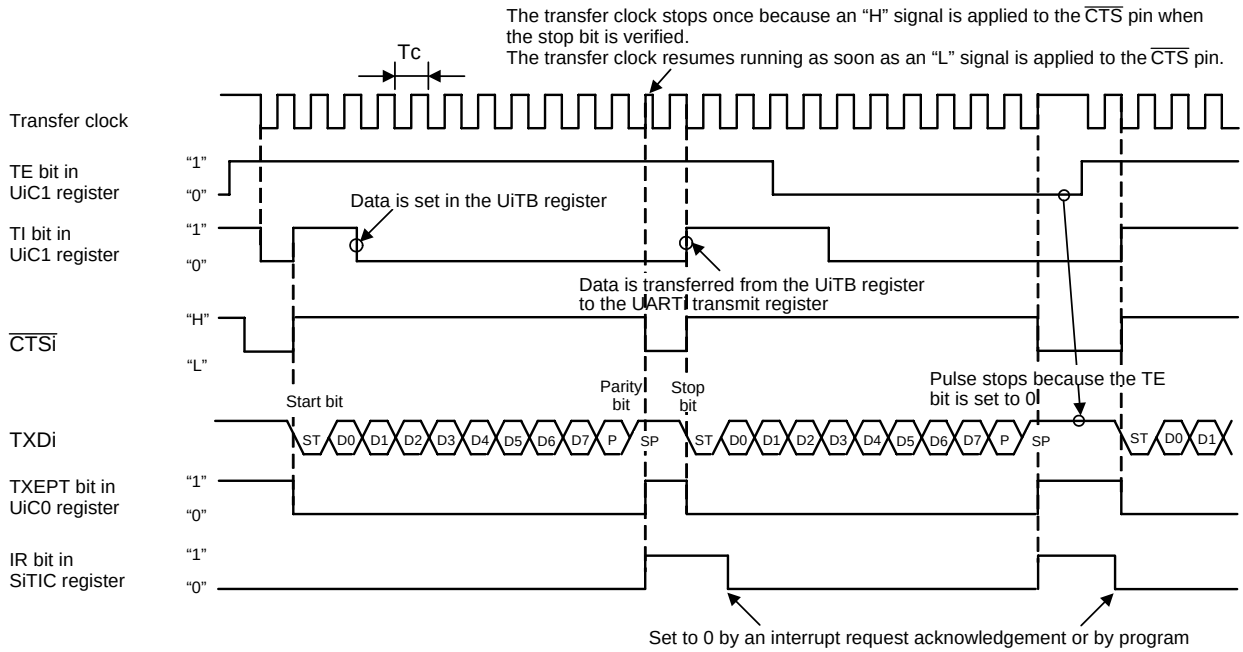


Figure 13.19 Transfer Clock Output from Multiple Pins

(1) 8-bit Data Transmit Timing (with a Parity and 1 Stop Bit)

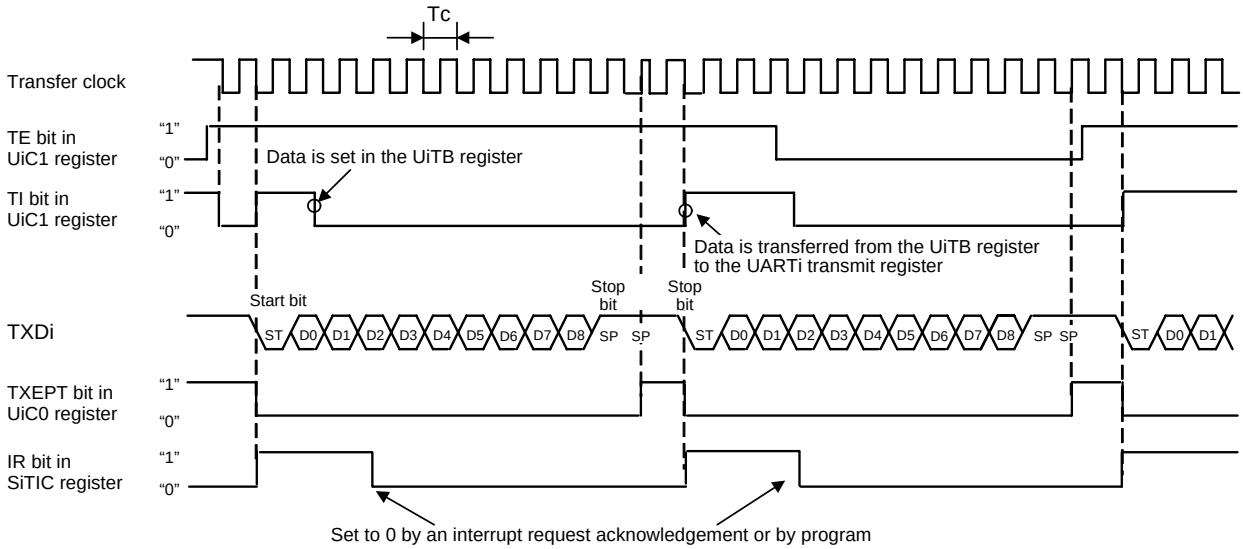


i = 0 to 2

The above timing diagram applies to the case where the register bits are set as follows:
- The PRYE bit in the UiMR register = 1 (parity enabled)
- The STPS bit in the UiMR register = 0 (1 stop bit)
- The CRD bit in the UiC0 register = 0 (CTS/RTS enabled) and the CRS bit = 0 (CTS selected)
- The UiIRS bit in the UiC1 register = 1 (an interrupt request occurs when transmit completed)

Tc = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: frequency of UiBRG count source (f1SIO, f2SIO, f8SIO, f32SIO)
fEXT: frequency of UiBRG count source (external clock)
n: value set to UiBRG

(2) 9-bit Data Transmit Timing (with No Parity and 2 Stop Bits)



i = 0 to 2

The above timing diagram applies to the case where the register bits are set as follows:
- The PRYE bit in the UiMR register = 0 (parity disabled)
- The STPS bit in the UiMR register = 1 (2 stop bits)
- The CRD bit in the UiC0 register = 1 (CTS/RTS disabled)
- The UiIRS bit in the UiC1 register = 0 (an interrupt request occurs when transmit buffer becomes empty)

Tc = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: frequency of UiBRG count source (f1SIO, f2SIO, f8SIO, f32SIO)
fEXT: frequency of UiBRG count source (external clock)
n: value set to UiBRG

Figure 13.21 Transmit Timing in UART Mode

Table 13.11 Registers Used and Settings in I²C Mode (1)

Register	Bit	Function	
		Master	Slave
UiTB	0 to 7	Set transmission data	Set transmission data
UiRB (3)	0 to 7	Reception data can be read	Reception data can be read
	8	ACK or NACK is set in this bit	ACK or NACK is set in this bit
	ABT	Arbitration lost detection flag	Invalid
	OER	Overrun error flag	Overrun error flag
UiBRG	0 to 7	Set a bit rate	Invalid
UiMR (3)	SMD2 to SMD0	Set to 010b	Set to 010b
	CKDIR	Set to 0	Set to 1
	IOPOL	Set to 0	Set to 0
UiC0	CLK1, CLK0	Select the count source for the UiBRG register	Invalid
	CRS	Invalid because CRD = 1	Invalid because CRD = 1
	TXEPT	Transmit register empty flag	Transmit register empty flag
	CRD (4)	Set to 1	Set to 1
	NCH	Set to 1 (2)	Set to 1 (2)
	CKPOL	Set to 0	Set to 0
	UFORM	Set to 1	Set to 1
UiC1	TE	Set this bit to 1 to enable transmission	Set this bit to 1 to enable transmission
	TI	Transmit buffer empty flag	Transmit buffer empty flag
	RE	Set this bit to 1 to enable reception	Set this bit to 1 to enable reception
	RI	Reception complete flag	Reception complete flag
	UiIRS (1)	Invalid	Invalid
	UiRRM (1), UiLCH, UiERE	Set to 0	Set to 0
UiSMR	IICM	Set to 1	Set to 1
	ABC	Select the timing at which arbitration lost is detected	Invalid
	BBS	Bus busy flag	Bus busy flag
	3 to 7	Set to 0	Set to 0
UiSMR2	IICM2	Refer to **Table 13.13 "I²C Mode Functions"**	Refer to **Table 13.13 "I²C Mode Functions"**
	CSC	Set this bit to 1 to enable clock synchronization	Set to 0
	SWC	Set this bit to 1 to have SCLi output fixed to "L" at the falling edge of the 9th bit of clock	Set this bit to 1 to have SCLi output fixed to "L" at the falling edge of the 9th bit of clock
	ALS	Set this bit to 1 to have SDAi output stopped when arbitration lost is detected	Set to 0
	STAC	Set to 0	Set this bit to 1 to initialize UARTi at start condition detection
	SWC2	Set this bit to 1 to have SCLi output forcibly pulled low	Set this bit to 1 to have SCLi output forcibly pulled low
	SDHI	Set this bit to 1 to disable SDAi output	Set this bit to 1 to disable SDAi output
	7	Set to 0	Set to 0

i = 0 to 2

NOTES:

1. Set the bit 4 and bit 5 in registers U0C1 and U1C1 to 0. Bits U0IRS, U1IRS, U0RRM, and U1RRM are in the UCON register.
2. The TXD2 pin is N channel open-drain output. No NCH bit in the U2C0 register is assigned. When write, set to 0.
3. Set the bits not listed above to 0 when writing to the registers in I²C mode.
4. When using UART1 in I²C mode and enabling the $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ separate function of UART0, set the CRD bit in the U1C0 register to 0 ($\overline{\text{CTS}}$/$\overline{\text{RTS}}$ enabled) and the CRS bit to 0 ($\overline{\text{CTS}}$ input).

15.2.26 Time Stamp Registers

These registers are for storing the timer value when frame reception is completed.
The count value on completion of reception is automatically stored in time stamp registers.
The time stamp value is retained until the next reception is completed.
When reading these registers, the time stamp value corresponding to the receive RAM bank specified with the RCVBANKSEL bit in the BBTXRXMODE3 register is read.

Time Stamp Register 0

(b15) (b8) b7 b0 b7 b0

Symbol	Address	After Reset
BBTSTAMP0	0131h, 0130h	0000h

Function	RW
Time stamp register 0 BBTSTAMP0: Lower bits (bits 15 to 0) of the 26-bit stamp value (1)	R

Time Stamp Register 1

(b15) (b8) b7 b0 b7 b0

Symbol	Address	After Reset
BBTSTAMP1	0133h, 0132h	0000h

Function	RW
Time stamp register 1 BBTSTAMP1: Lower bits (bits 25 to 16) of the 26-bit stamp value (1)	R
No register bits. If necessary, set to 0. Read as 0.	—

NOTE:
1. These bits correspond to the receive RAM bank.

Figure 15.35 Timer Stamp Register Configuration

15.3.5 Baseband Startup Procedure Example

[1] Set 1 (baseband functions enabled) in the BBEN bit in the BBCON register.
[2] Set 01h (1 ms) in the BBIDLEWAIT register.
Set 1 (IDLE interrupt) in the BANK0INTSEL bit in the BBTXRXMODE4 register.
Set 1 (RF power ON) in the RFPWRON bit in the BBRFCON register, and 1 (XIN power ON) in the XINPWRON bit.
[3] Allow a delay until the IDLE interrupt is generated (delay until the wait time set in the BBIDLEWAIT register has elapsed from step [2]).

15.3.6 Baseband Shutdown Procedure Example

[1] Set 0 (OFF) in the RFPWRON bit in the BBRFCON register.
[2] Set 0 (baseband functions disabled) in the BBEN bit in the BBCON register.

Setup procedure and CRC operation when generating CRC code “80C4h”

• CRC operation performed by the M16C

CRC code: remainder of a division in which the value written to the CRCIN register with its bit positions reversed is divided by the generator polynomial
Generator polynomial: $X^{16} + X^{12} + X^5 + 1$ (1 0001 0000 0010 0001b)

• Setting procedure

(1) Reverse the bit positions of the value “80C4h” by program in 1-byte units.

80h → 01h, C4h → 23h

(2) Write 0000h (initial value) → b15 b0 CRCD register

(3) Write 01h → b7 b0 CRCIN register
Two cycles later, the CRC code for 80h, i.e., 9188h, has its bit positions reversed to become 1189h which is stored in the CRCD register.
b15 b0 1189h CRCD register

(4) Write 23h → b7 b0 CRCIN register
Two cycles later, the CRC code for 80C4h, i.e., 8250h, has its bit positions reversed to become 0A41h which is stored in the CRCD register.
b15 b0 0A41h CRCD register

• Details of CRC operation

As shown in (3) above, bit position of 01h (00000001b) written to the CRCIN register is reversed and becomes 10000000b.
Add 1000 0000 0000 0000 0000 0000b, as 10000000b plus 16 digits, to 0000 0000 0000 0000 0000 0000b,
as 0000 0000 0000 0000b plus 8 digits as the default value of the CRCD register to perform the modulo-2 division.

```
                                  1000 1000
                 ┌──────────────────────
1 0001 0000 0010 0001 │ 1000 0000 0000 0000 0000 0000   ← Data
                      1000 1000 0001 0000 1
                           1000 0001 0000 1000 0
                           1000 1000 0001 0000 1
                                1001 0001 1000 1000
```

Generator polynomial

CRC code

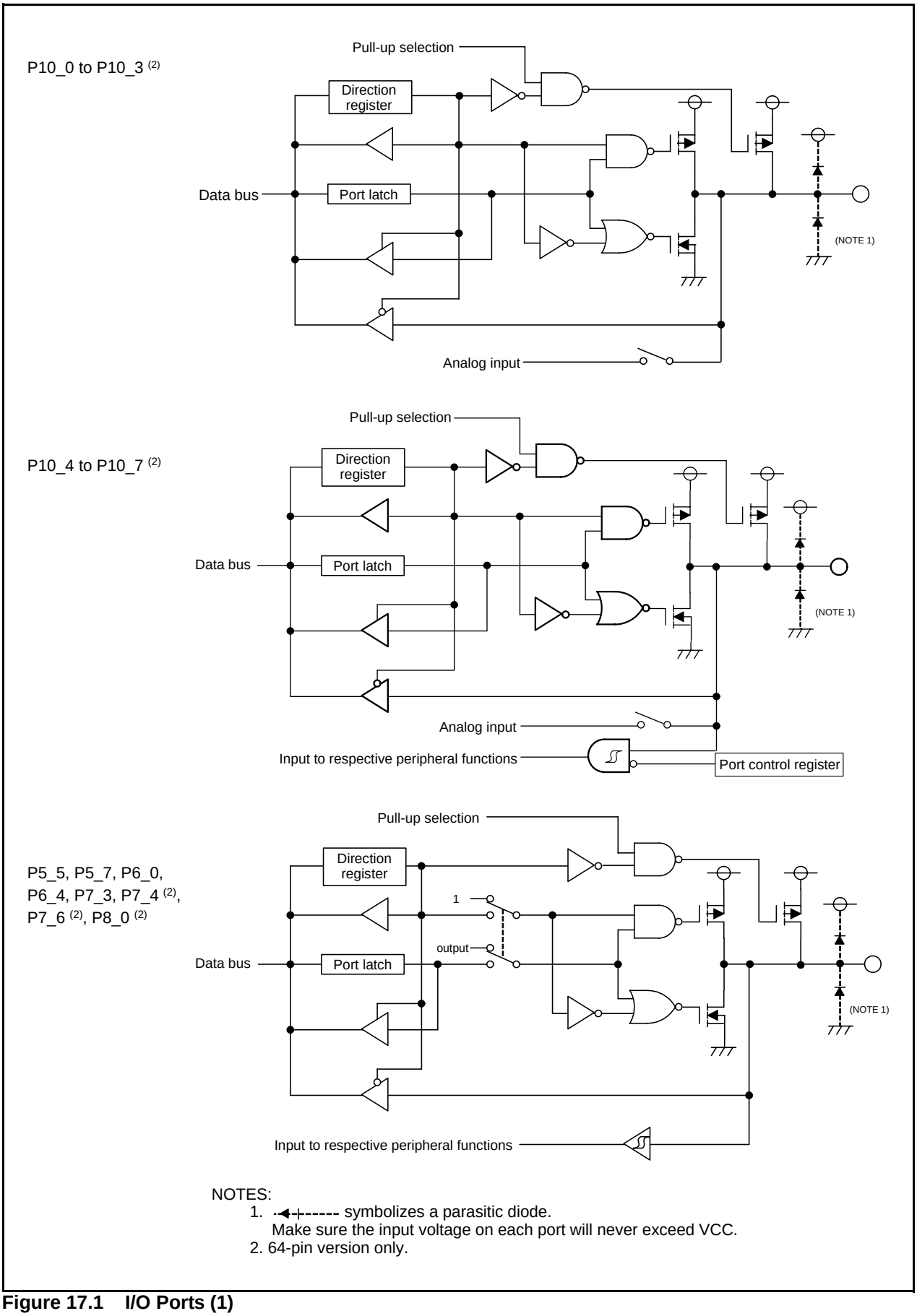
Modulo-2 operation is operation that complies with the law given below.

0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 0
-1 = 1

0001 0001 1000 1001b (1189h), the remainder 1001 0001 1000 1000b (9188h) with inversed bit position, can be read from the CRCD register.

When going on to (4) above, 23h (00100011b) written in the CRCIN register is reversed and becomes 11000100b.
Add 1100 0100 0000 0000 0000 0000b, as 11000100b plus 16 digits, to 1001 0001 1000 1000 0000 0000b, as 1001 0001 1000 1000b plus 8 digits as a remainder of (3) left in the CRCD register to perform the modulo-2 division.
0000 1010 0100 0001b (0A41h), the remainder with reversed bit position, can be read from the CRCD register.

Figure 16.3 Example of Using the CRC Operation



NOTES:
1. -◄-┼------ symbolizes a parasitic diode.
   Make sure the input voltage on each port will never exceed VCC.
2. 64-pin version only.

Figure 17.1 I/O Ports (1)

20. Precautions

20.1 SFR

20.1.1 Register Settings

Table 20.1 lists Registers with Write-Only Bits. Set these registers with immediate values. When establishing a next value by altering the existing value, write the existing value to the RAM as well as to the register. Transfer the next value to the register after making changes in the RAM.

Table 20.1 Registers with Write-Only Bits

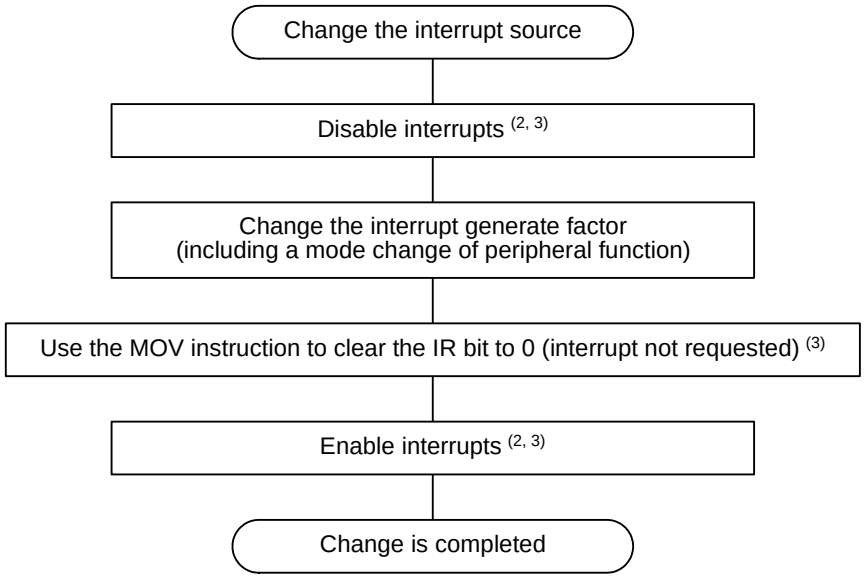
Register	Symbol	Address
Watchdog timer reset register	WDTR	037Dh
Watchdog timer start register	WDTS	037Eh
UART0 bit rate register	U0BRG	0249h
UART1 bit rate register	U1BRG	0259h
UART2 bit rate register	U2BRG	0269h
UART0 transmit buffer register	U0TB	024Bh to 024Ah
UART1 transmit buffer register	U1TB	025Bh to 025Ah
UART2 transmit buffer register	U2TB	026Bh to 026Ah
Timer A0 register	TA0	0327h to 0326h
Timer A1 register	TA1	0329h to 0328h
Timer A2 register	TA2	032Bh to 032Ah
Timer A3 register	TA3	032Dh to 032Ch
Timer A4 register	TA4	032Fh to 032Eh

20.5.4 Changing an Interrupt Generate Factor

If the interrupt generate factor is changed, the IR bit in the interrupt control register for the changed interrupt may inadvertently be set to 1 (interrupt requested). To use an interrupt, change the interrupt generate factor, and then be sure to clear the IR bit for that interrupt to 0 (interrupt not requested).

Changing the interrupt generate factor referred to here means any act of changing the source, polarity or timing of the interrupt assigned to each software interrupt number. Therefore, if a mode change of any peripheral function involves changing the source, polarity or timing of an interrupt, be sure to clear the IR bit for that interrupt to 0 (interrupt not requested) after making such changes. Refer to the description of each peripheral function for details about the interrupts from peripheral functions.

Figure 20.2 shows the Procedure for Changing the Interrupt Generate Factor.



IR bit: A bit in the interrupt control register for the interrupt whose interrupt generate factor is to be changed

NOTES:
1. The above settings must be executed individually. Do not execute two or more settings simultaneously (using one instruction).
2. Use the I flag for the $\overline{\text{INTi}}$ interrupt (i = 0, 1).
   For the interrupts from peripheral functions other than the $\overline{\text{INTi}}$ interrupt, turn off the peripheral function that is the source of the interrupt in order not to generate an interrupt request before changing the interrupt generate factor. In this case, if the maskable interrupts can all be disabled without causing a problem, use the I flag. Otherwise, use the corresponding bits ILVL2 to ILVL0 for the interrupt whose interrupt generate factor is to be changed.
3. Refer to **20.5.6 "Rewrite the Interrupt Control Register"** for details about the instructions to use and the notes to be taken for instruction execution.

Figure 20.2 Procedure for Changing the Interrupt Generate Factor

20.5.5 $\overline{\text{INT}}$ Interrupt

- Either an "L" level of at least tw(INL) width or an "H" level of at least tw(INH) width is necessary for the signal input to pins $\overline{\text{INT0}}$ through $\overline{\text{INT1}}$ regardless of the CPU operation clock.
- If the POL bit in registers INT0IC to INT1IC or bits IFSR1 to IFSR0 in the IFSR register are changed, the IR bit may inadvertently set to 1 (interrupt requested). Be sure to clear the IR bit to 0 (interrupt not requested) after changing any of those register bits.