Renesas Electronics America Inc - R5F36B4BNNP#U0 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	16
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN
Supplier Device Package	48-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f36b4bnnp-u0

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1. Overview

1.1 Features

The M16C/6B Group microcomputers (MCUs) incorporate the M16C/60 Series CPU core and flash memory.
These MCUs also function as low-power-consumption transceivers which support near field communication (2.4 GHz band).
Integrating some of the physical (PHY) and MAC layers compliant to the IEEE802.15.4 standard, the MUCs support various applications ranging from simple communication systems to mesh network systems.

1.1.1 Applications

Home automation, Building automation, Factory automation, Wireless sensor networks, RF remote controllers

1.4 Block Diagram

Figure 1.2 shows a Block Diagram.

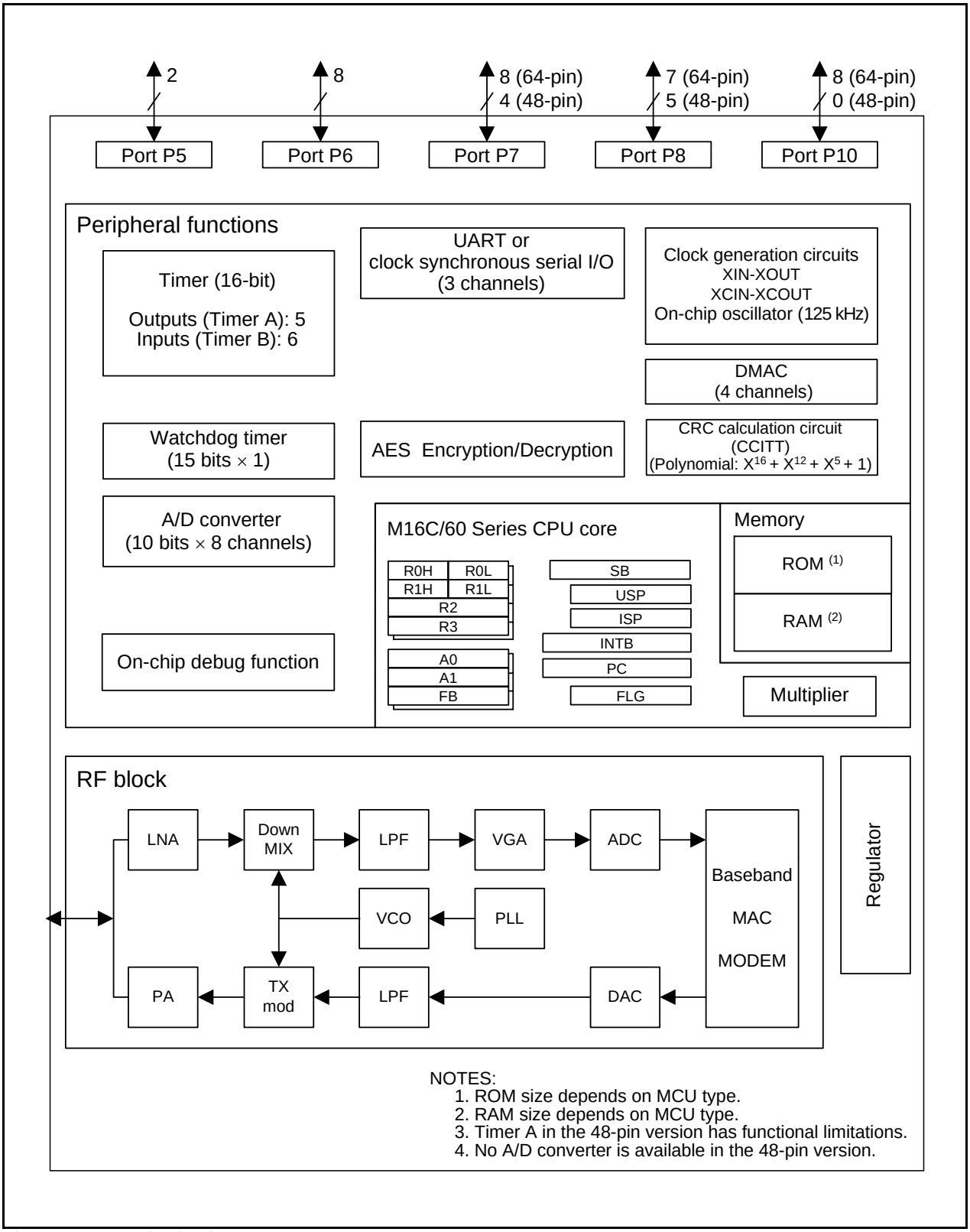


Figure 1.2 Block Diagram

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
0180h	DMA0 Source Pointer	SAR0	XXh
0181h			XXh
0182h			0Xh
0183h			
0184h	DMA0 Destination Pointer	DAR0	XXh
0185h			XXh
0186h			0Xh
0187h			
0188h	DMA0 Transfer Counter	TCR0	XXh
0189h			XXh
018Ah			
018Bh			
018Ch	DMA0 Control Register	DM0CON	00000X00b
018Dh			
018Eh			
018Fh			
0190h	DMA1 Source Pointer	SAR1	XXh
0191h			XXh
0192h			0Xh
0193h			
0194h	DMA1 Destination Pointer	DAR1	XXh
0195h			XXh
0196h			0Xh
0197h			
0198h	DMA1 Transfer Counter	TCR1	XXh
0199h			XXh
019Ah			
019Bh			
019Ch	DMA1 Control Register	DM1CON	00000X00b
019Dh			
019Eh			
019Fh			
01A0h	DMA2 Source Pointer	SAR2	XXh
01A1h			XXh
01A2h			0Xh
01A3h			
01A4h	DMA2 Destination Pointer	DAR2	XXh
01A5h			XXh
01A6h			0Xh
01A7h			
01A8h	DMA2 Transfer Counter	TCR2	XXh
01A9h			XXh
01AAh			
01ABh			
01ACh	DMA2 Control Register	DM2CON	00000X00b
01ADh			
01AEh			
01AFh			
01B0h	DMA3 Source Pointer	SAR3	XXh
01B1h			XXh
01B2h			0Xh
01B3h			
01B4h	DMA3 Destination Pointer	DAR3	XXh
01B5h			XXh
01B6h			0Xh
01B7h			
01B8h	DMA3 Transfer Counter	TCR3	XXh
01B9h			XXh
01BAh			
01BBh			
01BCh	DMA3 Control Register	DM3CON	00000X00b
01BDh			
01BEh			
01BFh			

NOTE: X: Undefined

1. The blank areas are reserved and cannot be accessed by users.

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	After Reset
0340h			
0341h			
0342h			
0343h			
0344h			
0345h			
0346h			
0347h			
0348h			
0349h			
034Ah			
034Bh			
034Ch			
034Dh			
034Eh			
034Fh			
0350h			
0351h			
0352h			
0353h			
0354h			
0355h			
0356h			
0357h			
0358h			
0359h			
035Ah			
035Bh			
035Ch			
035Dh			
035Eh			
035Fh			
0360h			
0361h	Pull-Up Control Register 1	PUR1	00000000b
0362h	Pull-Up Control Register 2	PUR2	00h
0363h			
0364h			
0365h			
0366h			
0367h			
0368h			
0369h			
036Ah			
036Bh			
036Ch			
036Dh			
036Eh			
036Fh			

NOTE: X: Undefined

1. The blank areas are reserved and cannot be accessed by users.

7.6.3 How to Use Oscillation Stop and Re-Oscillation Detect Function

- The oscillation stop and re-oscillation detect interrupt shares the vector with the watchdog timer interrupt. If the oscillation stop, re-oscillation detection and watchdog timer interrupts both are used, read the CM22 bit in an interrupt routine to determine which interrupt source is requesting the interrupt.
- When the main clock re-oscillated after oscillation stop, the clock source for the CPU clock and peripheral functions must be switched to the main clock in a program. Figure 7.12 shows the Procedure to Switch Clock Source from 125 kHz On-Chip Oscillator to Main Clock.
- Simultaneously with oscillation stop and re-oscillation detection interrupt occurrence, the CM22 bit becomes 1. When the CM22 bit is set to 1, oscillation stop and re-oscillation detection interrupt are disabled. By setting the CM22 bit to 0 in a program, oscillation stop and re-oscillation detection interrupt are enabled.
- If the main clock stops during low speed mode where the CM20 bit is 1, an oscillation stop and re-oscillation detection interrupt request is generated. At the same time, the 125 kHz on-chip oscillator starts oscillating. In this case, although the CPU clock is derived from the subclock as it was before the interrupt occurred, the peripheral function clocks now are derived from the 125 kHz on-chip oscillator clock.
- To enter wait mode while using the oscillation stop and re-oscillation detection function, set the CM02 bit to 0 (peripheral function clocks not turned off during wait mode).
- Since the oscillation stop and re-oscillation detection function is provided in preparation for main clock stop due to external factors, set the CM20 bit to 0 (oscillation stop and re-oscillation detection function disabled) where the main clock is stopped or oscillated in a program, that is where the stop mode is selected or the CM05 bit is altered.
- This function cannot be used if the main clock frequency is 2 MHz or less. In that case, set the CM20 bit to 0.

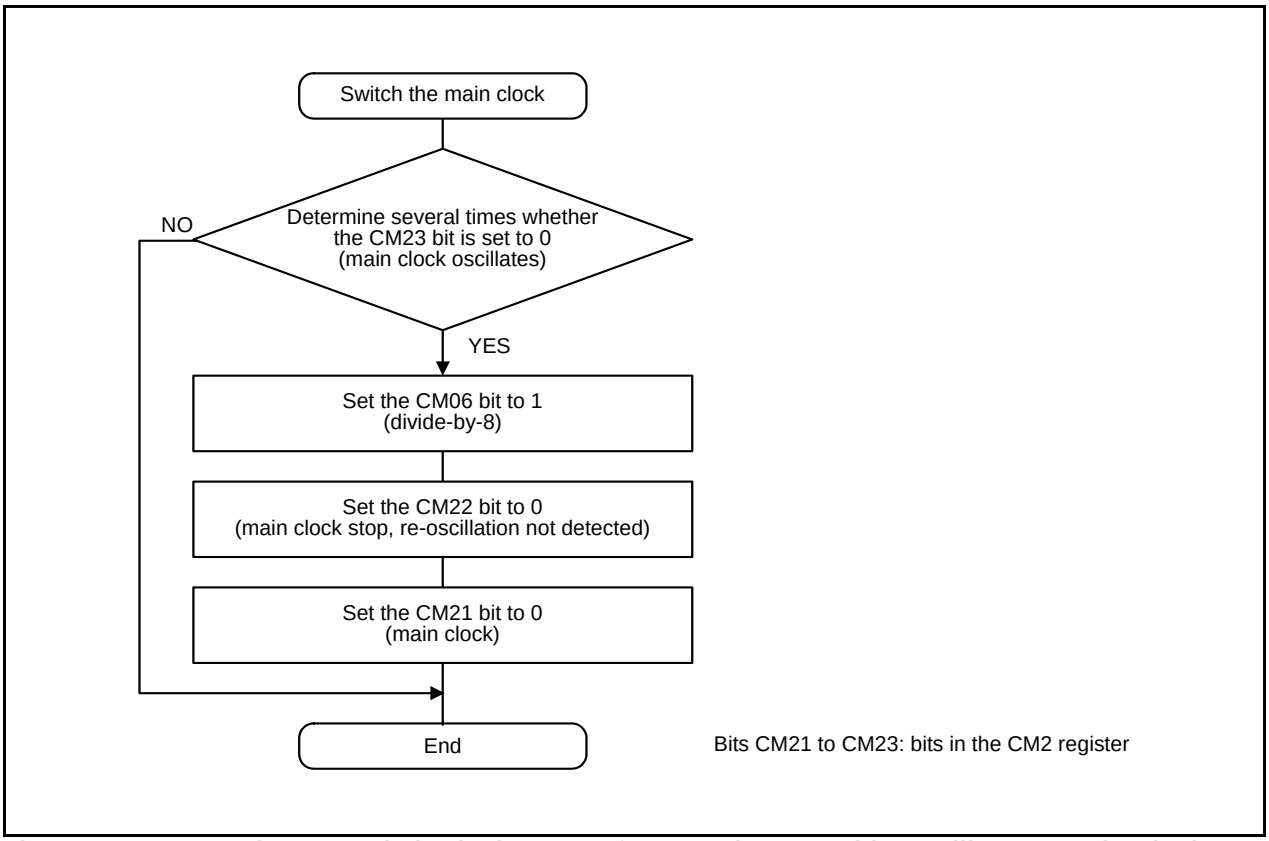


Figure 7.12 Procedure to Switch Clock Source from 125 kHz On-Chip Oscillator to Main Clock

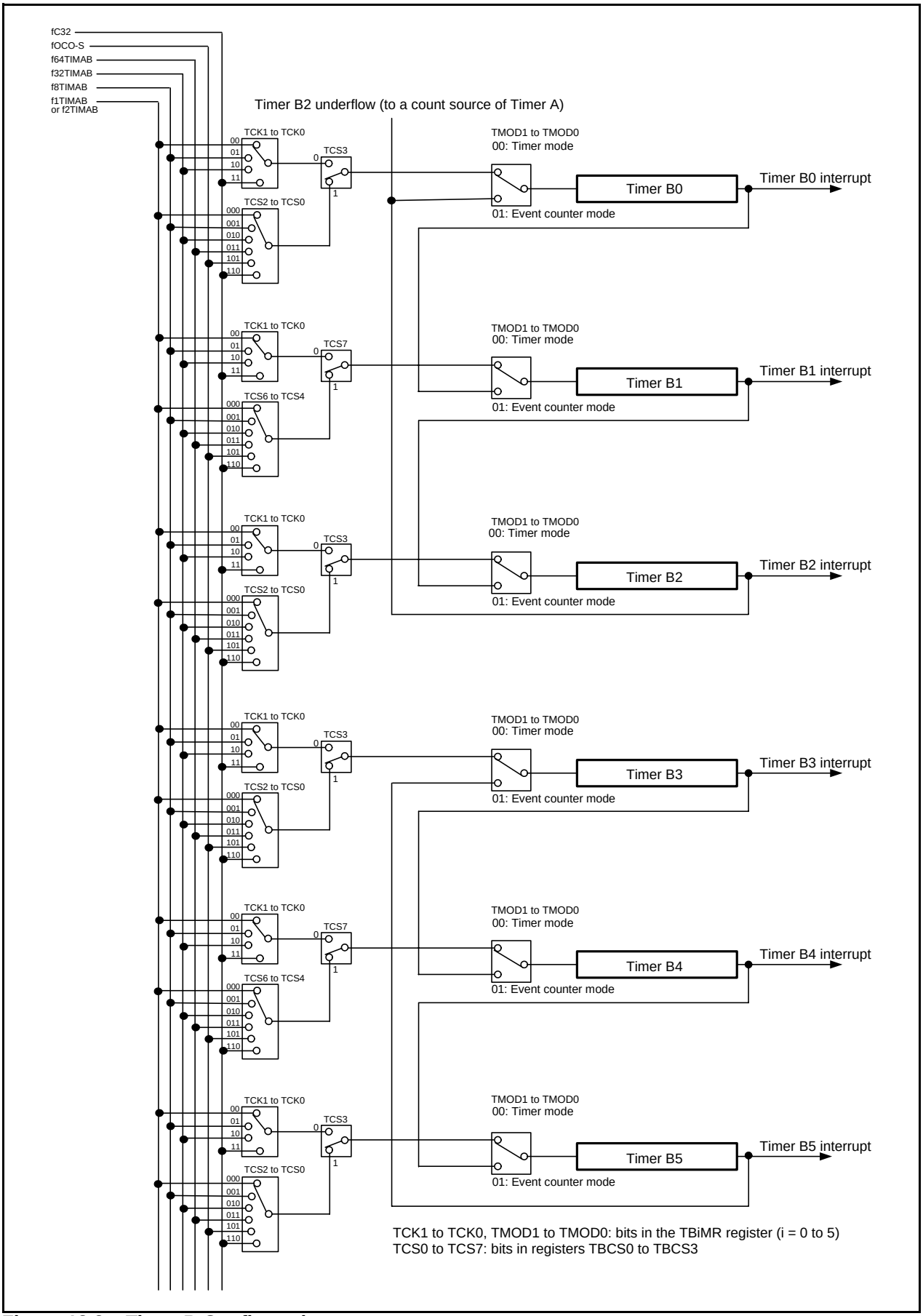


Figure 12.3 Timer B Configuration

Count Start Flag

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TABSR	0320h	00h

Bit Symbol	Bit Name	Function	RW
TA0S	Timer A0 count start flag	0: Stop counting 1: Start counting	RW
TA1S	Timer A1 count start flag		RW
TA2S	Timer A2 count start flag		RW
TA3S	Timer A3 count start flag		RW
TA4S	Timer A4 count start flag		RW
TB0S	Timer B0 count start flag		RW
TB1S	Timer B1 count start flag		RW
TB2S	Timer B2 count start flag		RW

Timer B3, B4, B5 Count Start Flag

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TBSR	0300h	000XXXXXb

Bit Symbol	Bit Name	Function	RW
— (b4-b0)	No register bits. If necessary, set to 0. Read as undefined value.		—
TB3S	Timer B3 count start flag	0: Stop counting 1: Start counting	RW
TB4S	Timer B4 count start flag		RW
TB5S	Timer B5 count start flag		RW

Clock Prescaler Reset Flag

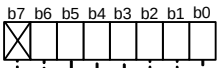
b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
CPSRF	0015h	0XXXXXXXb

Bit Symbol	Bit Name	Function	RW
— (b6-b0)	No register bits. If necessary, set to 0. Read as undefined value.		—
CPSR	Clock prescaler reset flag	Setting this bit to 1 initializes the clock prescaler. (Read as 0)	RW

Figure 12.21 Register TABSR, TBSR, and CPSRF

UARTi Special Mode Register 2 (i = 0 to 2)



Symbol: U0SMR2, U1SMR2, U2SMR2

Address: 0246h, 0256h, 0266h

After Reset: X0000000b

Bit Symbol	Bit Name	Function	RW
IICM2	I^2C mode select bit 2	Refer to **Table 13.13 "I^2C Mode Functions"**	RW
CSC	Clock synchronization bit	0: Disabled 1: Enabled	RW
SWC	SCL wait output bit	0: Disabled 1: Enabled	RW
ALS	SDA output stop bit	0: Disabled 1: Enabled	RW
STAC	UARTi initialization bit	0: Disabled 1: Enabled	RW
SWC2	SCL wait output bit 2	0: Transfer clock 1: "L" output	RW
SDHI	SDA output disable bit	0: Enabled 1: Disabled (high-impedance)	RW
— (b7)	No register bit. If necessary, set to 0. Read as undefined value.		—

Figure 13.12 U0SMR2 to U2SMR2 Register

UARTi Special Mode Register 4 (i = 0 to 2)

b7 b6 b5 b4 b3 b2 b1 b0	Symbol	Address	After Reset
	U0SMR4, U1SMR4, U2SMR4	0244h, 0254h, 0264h	00h

Bit Symbol	Bit Name	Function	RW
STAREQ	Start condition generate bit (1)	0: Clear 1: Start	RW
RSTAREQ	Restart condition generate bit (1)	0: Clear 1: Start	RW
STPREQ	Stop condition generate bit (1)	0: Clear 1: Start	RW
STSPSEL	SCL, SDA output select bit	0: Start and stop conditions not output 1: Start and stop conditions output	RW
ACKD	ACK data bit	0: ACK 1: NACK	RW
ACKC	ACK data output enable bit	0: Serial interface data output 1: ACK data output	RW
SCLHI	SCL output stop enable bit	0: Disabled 1: Enabled	RW
SWC9	SCL wait bit 3	0: SCL “L” hold disabled 1: SCL “L” hold enabled	RW

NOTE:
1. Set to 0 when each condition is generated.

Figure 13.14 Registers U0SMR4 to U2SMR4

Table 13.16 Registers Used and Settings in Special Mode 2

Register	Bit	Function
UiTB	0 to 7	Set transmission data
UiRB (3)	0 to 7	Reception data can be read
	OER	Overrun error flag
UiBRG	0 to 7	Set a bit rate
UiMR (3)	SMD2 to SMD0	Set to 001b
	CKDIR	Set to 0 in master mode or 1 in slave mode
	IOPOL	Set to 0
UiC0	CLK0, CLK1	Select the count source for the UiBRG register
	CRS	Invalid because CRD = 1
	TXEPT	Transmit register empty flag
	CRD	Set to 1
	NCH	Select TXDi pin output format (2)
	CKPOL	Clock phases can be set in combination with the CKPH bit in the UiSMR3 register
	UFORM	Set to 0
UiC1	TE	Set to 1 to enable transmission/reception
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception
	RI	Reception complete flag
	UiIRS (1)	Select UART2 transmit interrupt source
	UiRRM (1), UiLCH, UiERE	Set to 0
UiSMR	0 to 7	Set to 0
UiSMR2	0 to 7	Set to 0
UiSMR3	CKPH	Clock phases can be set in combination with the CKPOL bit in the UiC0 register
	NODC	Set to 0
	0, 2, 4 to 7	Set to 0
UiSMR4	0 to 7	Set to 0
UCON	U0IRS, U1IRS	Select UART0 and UART1 transmit interrupt source
	U0RRM, U1RRM	Set to 0
	CLKMD0	Invalid because CLKMD1 = 0
	CLKMD1, RCSP, 7	Set to 0

i = 0 to 2

NOTES:

1. Set bits 4 and 5 in registers U0C0 and U1C1 to 0. Bits U0IRS, U1IRS, U0RRM, and U1RRM are in the UCON register.
2. The TXD2 pin is N channel open-drain output. No NCH bit in the U2C0 register is assigned. When write, set to 0.
3. Set the bits not listed above to 0 when writing to the registers in special mode 2.

15.2.22 Short Address Register

This register is for setting short addresses. It consists of 16 bits and is used to detect a match with the short address of a receive frame.

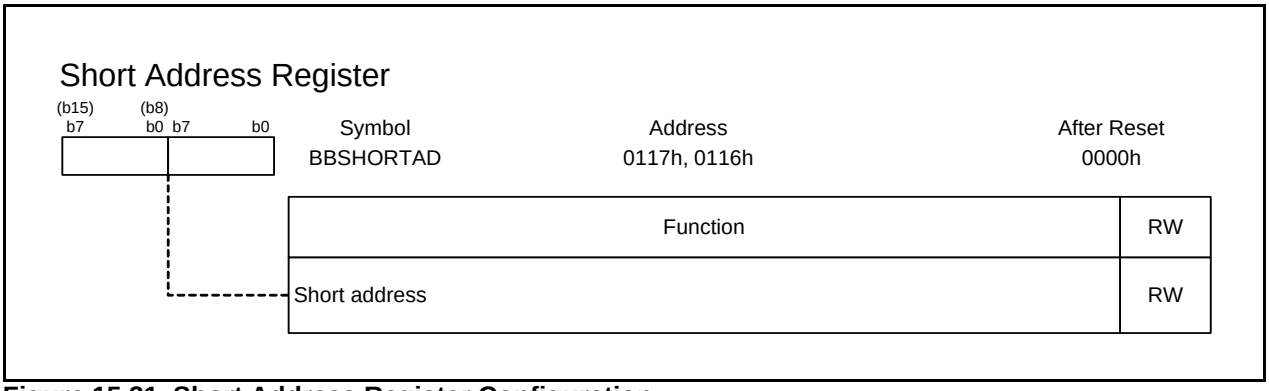


Figure 15.31 Short Address Register Configuration

15.2.23 Extended Address Register

This register is for setting extended addresses. It consists of 64 bits (16 bits × 4) and is used to detect a match with the extended address of a receive frame.

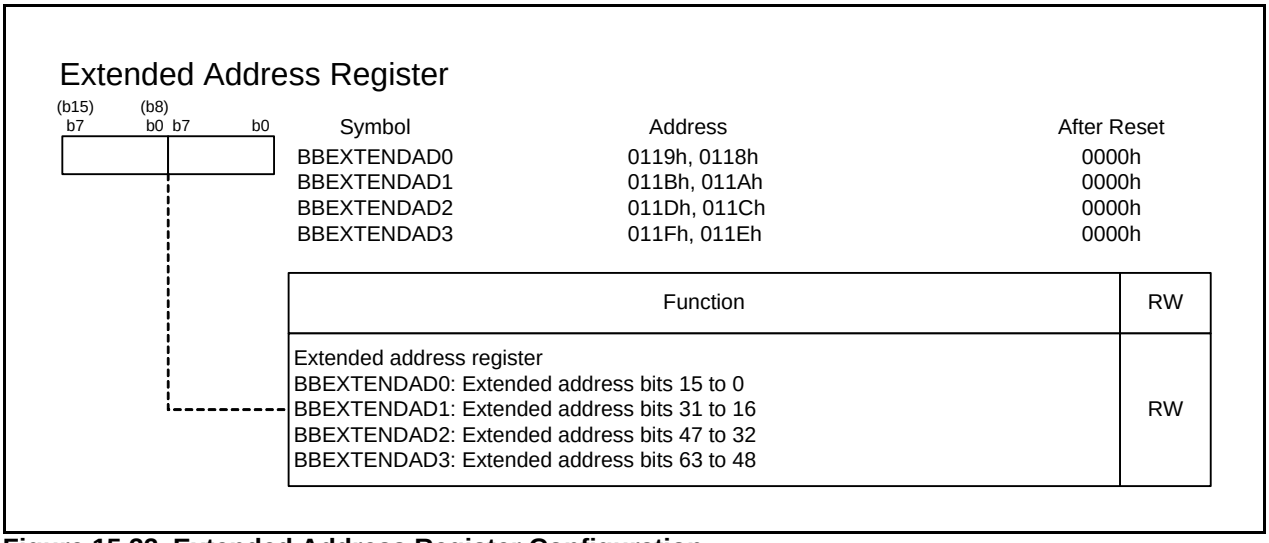


Figure 15.32 Extended Address Register Configuration

15.2.31 RSSI Offset Register

This register can be used to set an offset value as the RSSI value during CCA/ED or reception.
The value can be used to adjust the power value read from the RSSI/CCA result register to the power value input to the antenna.
Set the value to two's complement in dBm units.
The value set in the receive level threshold set register or CCA level threshold set register is compared with the value to be stored in the RSSI/CCA result register (the value added with the offset value set in the RSSI offset register).

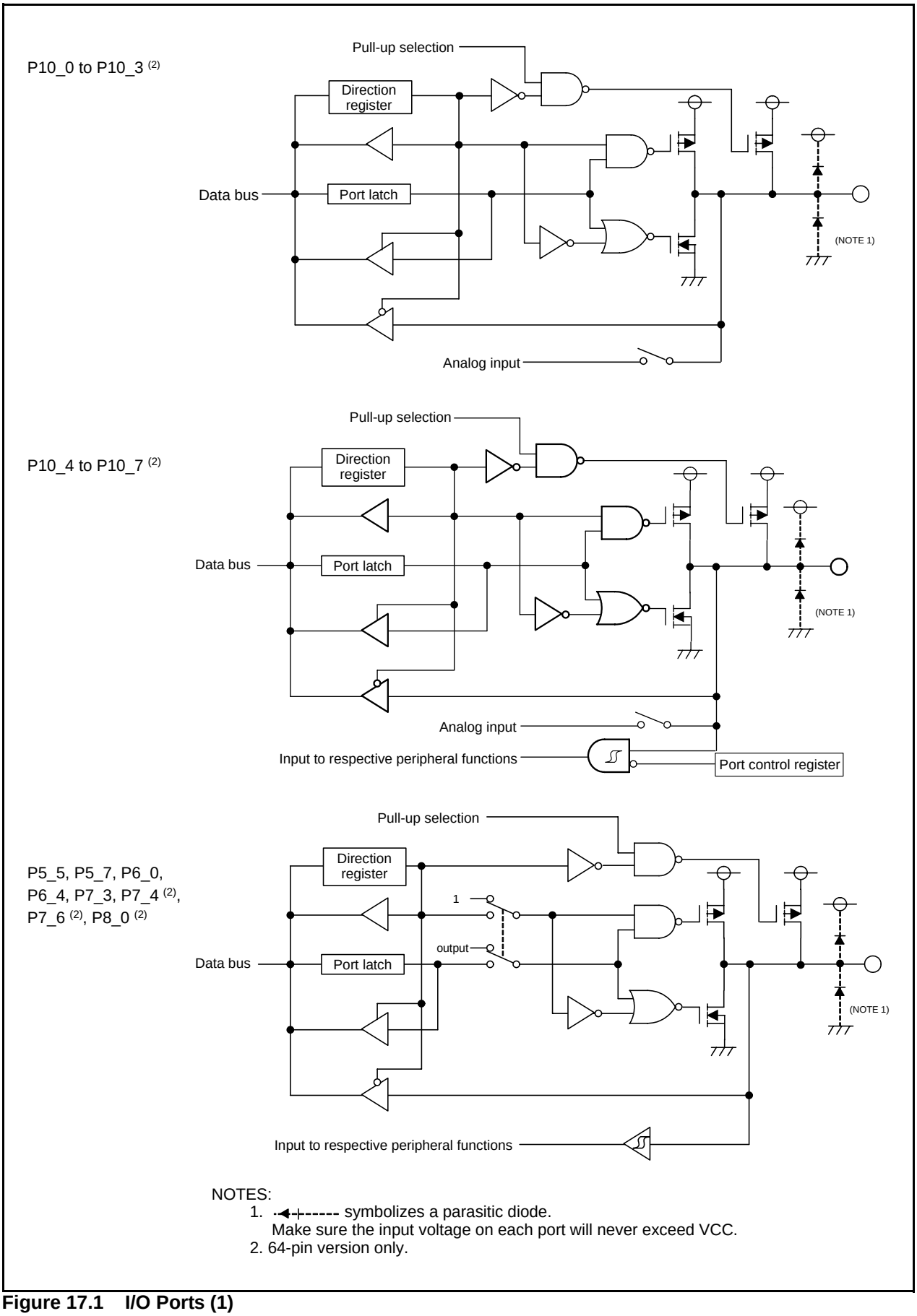
Example:
If the value read from the RSSI/CCA result register is FDh (-3 dBm) while the value set in the RSSI offset register is EEh (initial value) when the power input to the antenna is 0 dBm, the value read from the RSSI/CCA result register can be adjusted to 00h when the input power is the same level by setting EBh (EEh-3h) in the RSSI offset register beforehand.

RSSI Offset Register

b7 b0	Symbol	Address	After Reset
	BBRSSIOFS	013Dh	EEh

Bit Symbol	Bit Name	Function	RW
RSSIOFS	RSSI offset bit	Sets an offset value of RSSI	RW

Figure 15.40 RSSI Offset Register Configuration



NOTES:
1. -◄-┼------ symbolizes a parasitic diode.
   Make sure the input voltage on each port will never exceed VCC.
2. 64-pin version only.

Figure 17.1 I/O Ports (1)

18.3.1 EW0 Mode

The microcomputer enters CPU rewrite mode by setting the FMR01 bit in the FMR0 register to 1 (CPU rewrite mode enabled) and is ready to accept commands. EW0 mode is selected by setting the FMR60 bit in the FMR6 register to 0. Figure 18.5 shows Setting and Resetting of EW0 Mode.
The software commands control programming and erasing. The FMR0 register or the status register indicates whether a program or erase operation is completed as expected or not.

18.3.2 EW1 Mode

EW1 mode is selected by setting the FMR60 bit to 1 after setting the FMR01 bit to 1. Figure 18.6 shows Setting and Resetting of EW1 Mode.
The FMR0 register indicates whether or not a program or erase operation has been completed as expected. The status register cannot be read in EW1 mode.
When a program/erase operation is initiated, the CPU halts all program execution until the operation is completed.

Figure 18.5 shows Setting and Resetting of EW0 Mode. Figure 18.6 shows Setting and Resetting of EW1 Mode.

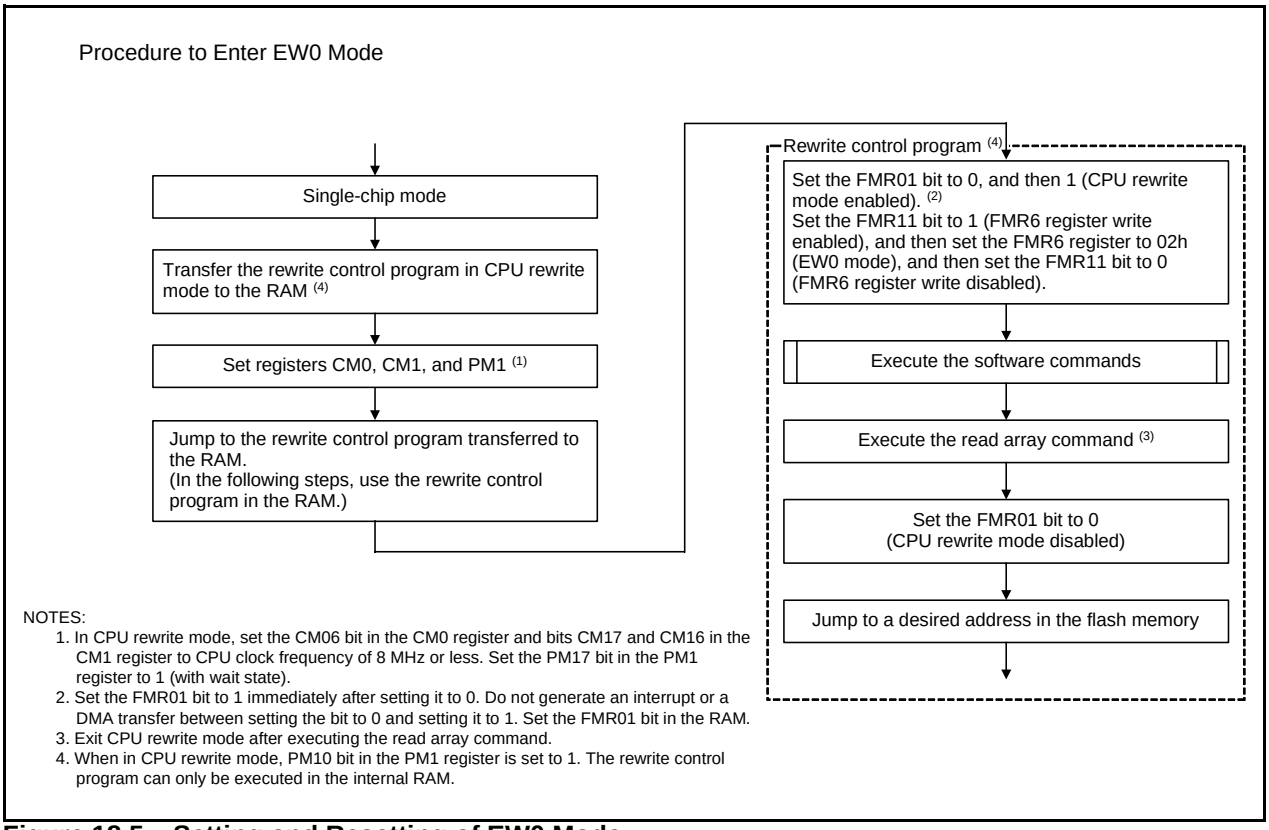


Figure 18.5 Setting and Resetting of EW0 Mode

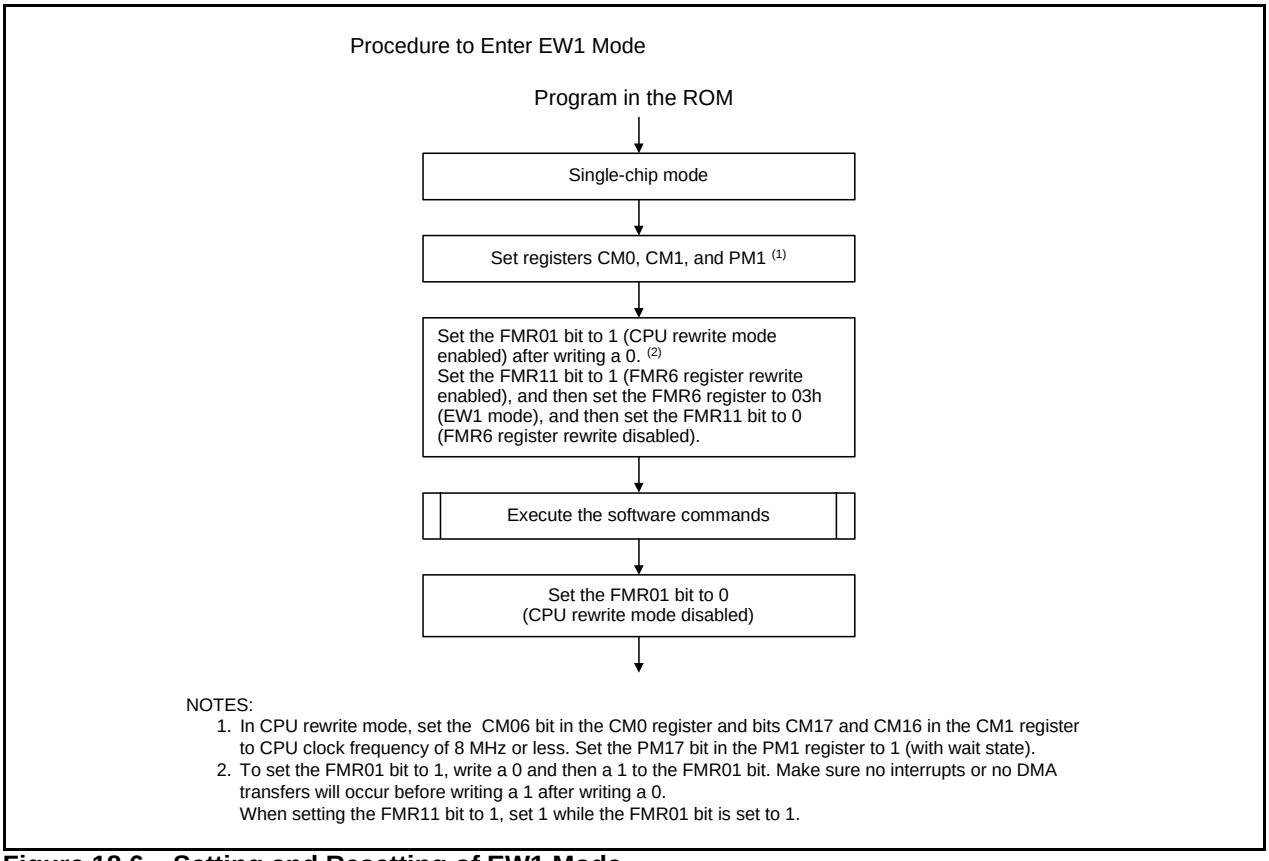


Figure 18.6 Setting and Resetting of EW1 Mode

Table 18.13 Pin Functions (Flash Memory Standard Serial I/O Mode)

Pin	Name	I/O	Description
VCC, VCC1, VSS2	Power input	I	Apply the flash program and erase voltage to the VCC pin, and 0 V to pins VSS1, VSS2.
AVCC (1), AVSS (1)	AD power input	I	Connect the AVCC pin to VCC. Connect the AVSS pin to VSS.
CNVSS	CNVSS	I	Connect to VCC.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin. While the $\overline{\text{RESET}}$ pin is “L” level, input a 20_cycle or longer clock to the XIN pin.
XIN	Clock input	I	I/O pins for the main clock oscillation circuit. Connect a crystal oscillator between pins XIN and XOUT.
XOUT	Clock output	O	
VREF (1)	Reference voltage input	I	Reference voltage input pin for A/D converter.
P5_5	$\overline{\text{EPM}}$ input	I	Input “L” level signal.
P5_7	Input port P5	I	Input “H” or “L” level signal or open.
P6_0 to P6_3	Input port P6	I	Input “H” or “L” level signal or open.
P6_4/$\overline{\text{RTS1}}$	BUSY output	O	Standard serial I/O mode 1: BUSY signal output pin. Standard serial I/O mode 2: Monitor signal output pin to check the boot program operation.
P6_5/CLK1	SCLK input	I	Standard serial I/O mode 1: Serial clock input pin. Standard serial I/O mode 2: Input “L”.
P6_6/RXD1	RXD input	I	Serial data input pin.
P6_6/TXD1	TXD output	O	Serial data output pin.
P7_0 to P7_3	Input port P7	I	Input “H” or “L” level signal or open.
P7_4 to P7_7 (1)	Input port P7	I	Input “H” or “L” level signal or open.
P8_0 (1), P8_1 (1)	Input port P8	I	Input “H” or “L” level signal or open.
P8_2, P8_3	Input port P8	I	Input “H” or “L” level signal or open.
P8_5/$\overline{\text{NMI}}$	$\overline{\text{NMI}}$ input	I	Input “H” or “L” level signal or open.
P8_6, P8_7	Input port P8	I	Input “H” or “L” level signal or open.
P10_0 to P10_7 (1)	Input port P10	I	Input “H” or “L” level signal or open.
VCCRF	Power input	I	Connect to VCC.
VSSRF, VSSRF1	Power input	I	Apply 0 V.
VSSRF2	Power input	I	Apply 0 V.
VSSRF3	Power input	I	Apply 0 V.
VSSRF4A, VSSRF4B	Power input	I	Apply 0 V.
VSSRF5	Power input	I	Apply 0 V.
VSSRF6	Power input	I	Apply 0 V.
VREGIN1	Power input	I	Connect to VREGOUT1.
VREGIN2	Power input	I	Connect to VREGOUT1.
VREGIN3	Power input	I	Connect to VREGOUT1.
VREGIN4	Power input	I	Connect to VREGOUT1.
VREGOUT1	Power output	O	Connect to VREGIN1 to VREGIN4.
VREGOUT2	Power output	O	Connect a bypass capacitor between pins VREGOUT2 and VSS.
VREGOUT3	Power output	O	Connect a bypass capacitor between pins VREGOUT2 and VSS.
RFIOP, RFION	RF I/O	I/O	RF I/O
TESTIOP, TESTION	Testing ports	I/O	Input “L” or open.
ANTSWCONT	Control output	O	Output pin to control the external antenna switch.

NOTE:
1. Not available in the 48 pin version.

20.5 Interrupt

20.5.1 Reading address 00000h

Do not read the address 00000h in a program. When a maskable interrupt request is accepted, the CPU reads interrupt information (interrupt number and interrupt request priority level) from the address 00000h during the interrupt sequence. At this time, the IR bit for the accepted interrupt is cleared to 0.
If the address 00000h is read in a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is cleared to 0. This factors a problem that the interrupt is canceled, or an unexpected interrupt request is generated.

20.5.2 SP Setting

Set any value in the SP (USP, ISP) before accepting an interrupt. The SP (USP, ISP) is cleared to 0000h after reset. Therefore, if an interrupt is accepted before setting any value in the SP (USP, ISP), the program may go out of control.
Especially when using the $\overline{\text{NMI}}$ interrupt, set a value in the ISP at the beginning of the program. Only for the first instruction after reset, all interrupts including the $\overline{\text{NMI}}$ interrupt are disabled.

20.5.3 $\overline{\text{NMI}}$ Interrupt

- The $\overline{\text{NMI}}$ interrupt cannot be disabled. If this interrupt is not used, set the PM24 bit in the PM2 register to 0 (port P8_5 function).
- Stop mode cannot be entered into while input on the $\overline{\text{NMI}}$ pin is “L” because the CM10 bit in the CM1 register is fixed to 0.
- Do not enter wait mode while input on the $\overline{\text{NMI}}$ pin is “L” because the CPU clock remains active even though the CPU stops, and therefore, the current consumption in the chip does not drop. In this case, normal condition is restored by a subsequent interrupt generated.
- Set the “L” and “H” level durations of the input signal to the $\overline{\text{NMI}}$ pin to 2 CPU clock cycles + 300 ns or more.

20.8 Serial Interface

20.8.1 Clock Synchronous Serial I/O

20.8.1.1 Transmission/Reception

When the $\overline{\text{RTS}}$ function is used with an external clock, $\overline{\text{RTSi}}$ pin (i = 0 to 2) outputs “L”, which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{\text{RTSi}}$ pin outputs “H” when a receive operation starts. Therefore, a transmit timing and receive timing can be synchronized by connecting the $\overline{\text{RTSi}}$ pin to the $\overline{\text{CTSi}}$ pin of the transmitting side. The $\overline{\text{RTS}}$ function is disabled when an internal clock is selected.

20.8.2 UART (Clock Asynchronous Serial I/O) Mode

20.8.2.1 Transmission/Reception

When the $\overline{\text{RTS}}$ function is used with an external clock, $\overline{\text{RTSi}}$ pin (i = 0 to 2) outputs “L”, which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{\text{RTSi}}$ pin outputs “H” when a receive operation starts. Therefore, a transmit timing and receive timing can be synchronized by connecting the $\overline{\text{RTSi}}$ pin to the $\overline{\text{CTSi}}$ pin of the transmitting side. The $\overline{\text{RTS}}$ function is disabled when an internal clock is selected.

20.8.2.2 Transmission

If an external clock is selected, the following conditions must be met while the external clock is held “H” when the CKPOL bit in the UiC0 register (i = 0 to 2) is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the serial clock), or while the external clock is held “L” when the CKPOL bit is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the serial clock).

- The TE bit in the UiC1 register = 1 (transmission enabled)
- The TI bit in the UiC1 register = 0 (data present in the UiTB register)
- If $\overline{\text{CTS}}$ function is selected, input on the $\overline{\text{CTSi}}$ pin = “L”

20.8.3 Special Mode 1 (I^2C Mode)

When generating start, stop, and restart conditions, set the STSPSEL bit in the UiSMR4 register (i = 0 to 2) to 0 and wait for more than half cycle of the transfer clock before setting each condition generation bit (STAREQ, RSTAREQ, and STPREQ) from 0 to 1.

20.8.4 Special Mode 4 (SIM Mode)

A transmit interrupt request is generated by setting bits U2IRS and U2ERE in the U2C1 register to 1 (transmission completed) and 1 (error signal output), respectively. Therefore, when using SIM mode, make sure to clear the IR bit to 0 (interrupt not requested) after setting these bits.

20.8.5 Common Items for Multiple Modes

20.8.5.1 CLKi Output

When using the output format of the CLKi pin as N channel open-drain output, follow the procedures below to change the pin function.

When changing to CLKi from a port

(1) Select the mode of the serial interface by setting bits SMD2 to SMD0 in the UiMR register to other than 000b.
(2) Set the NODC bit in the UiSMR3 register to 1.

When changing to a port from CLKi

(1) Set the NODC bit to 0.
(2) Disable the serial interface by setting bits SMD2 to SMD0 to 000b.