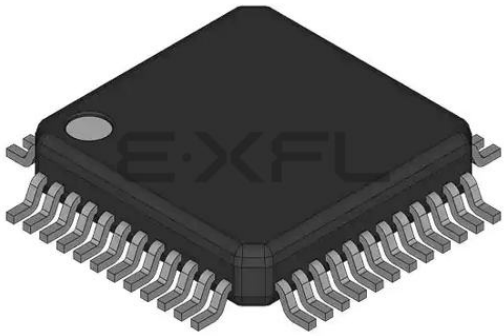


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | - |
| Core Size | - |
| Speed | - |
| Connectivity | - |
| Peripherals | - |
| Number of I/O | - |
| Program Memory Size | - |
| Program Memory Type | - |
| EEPROM Size | - |
| RAM Size | - |
| Voltage - Supply (Vcc/Vdd) | - |
| Data Converters | - |
| Oscillator Type | - |
| Operating Temperature | - |
| Mounting Type | - |
| Package / Case | - |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11u34fbd48-421 |

**Table 1. Ordering information** *…continued*

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| LPC11U36FBD64/401 | LQFP64 | plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |
| LPC11U37FBD48/401 | LQFP48 | plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |
| LPC11U37HFBD64/401 | LQFP64 | plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |
| LPC11U37FBD64/501 | LQFP64 | plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |

## 4.1 Ordering options

**Table 2. Ordering options**

| Type number | Flash in kB | EEPROM in kB | SRAM0 in kB | USB SRAM in kB | SRAM1 in kB | Total SRAM in kB[1] | I/O Handler | USART | I²C-bus FM+ | SSP | USB device | ADC channels | GPIO pins |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LPC11U34FHN33/311 | 40 | 4 | 8 | - | - | 8 | no | 1 | 1 | 2 | 1 | 8 | 26 |
| LPC11U34FBD48/311 | 40 | 4 | 8 | - | - | 8 | no | 1 | 1 | 2 | 1 | 8 | 40 |
| LPC11U34FHN33/421 | 48 | 4 | 8 | 2 | - | 10 | no | 1 | 1 | 2 | 1 | 8 | 26 |
| LPC11U34FBD48/421 | 48 | 4 | 8 | 2 | - | 10 | no | 1 | 1 | 2 | 1 | 8 | 40 |
| LPC11U35FHN33/401 | 64 | 4 | 8 | 2 | - | 10 | no | 1 | 1 | 2 | 1 | 8 | 26 |
| LPC11U35FBD48/401 | 64 | 4 | 8 | 2 | - | 10 | no | 1 | 1 | 2 | 1 | 8 | 40 |
| LPC11U35FBD64/401 | 64 | 4 | 8 | 2 | - | 10 | no | 1 | 1 | 2 | 1 | 8 | 54 |
| LPC11U35FHI33/501 | 64 | 4 | 8 | 2 | 2[1] | 12 | no | 1 | 1 | 2 | 1 | 8 | 26 |
| LPC11U35FET48/501 | 64 | 4 | 8 | 2 | 2[1] | 12 | no | 1 | 1 | 2 | 1 | 8 | 40 |
| LPC11U36FBD48/401 | 96 | 4 | 8 | 2 | - | 10 | no | 1 | 1 | 2 | 1 | 8 | 40 |
| LPC11U36FBD64/401 | 96 | 4 | 8 | 2 | - | 10 | no | 1 | 1 | 2 | 1 | 8 | 54 |
| LPC11U37FBD48/401 | 128 | 4 | 8 | 2 | - | 10 | no | 1 | 1 | 2 | 1 | 8 | 40 |
| LPC11U37HFBD64/401 | 128 | 4 | 8 | 2 | 2[2] | 10 | yes | 1 | 1 | 2 | 1 | 8 | 54 |
| LPC11U37FBD64/501 | 128 | 4 | 8 | 2 | 2[1] | 12 | no | 1 | 1 | 2 | 1 | 8 | 54 |

[1] For general-purpose use.

[2] For I/O Handler use only.

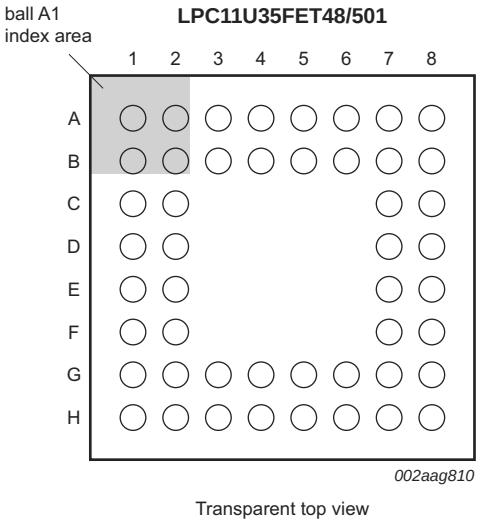



**Fig 3. Pin configuration (TFBGA48)**

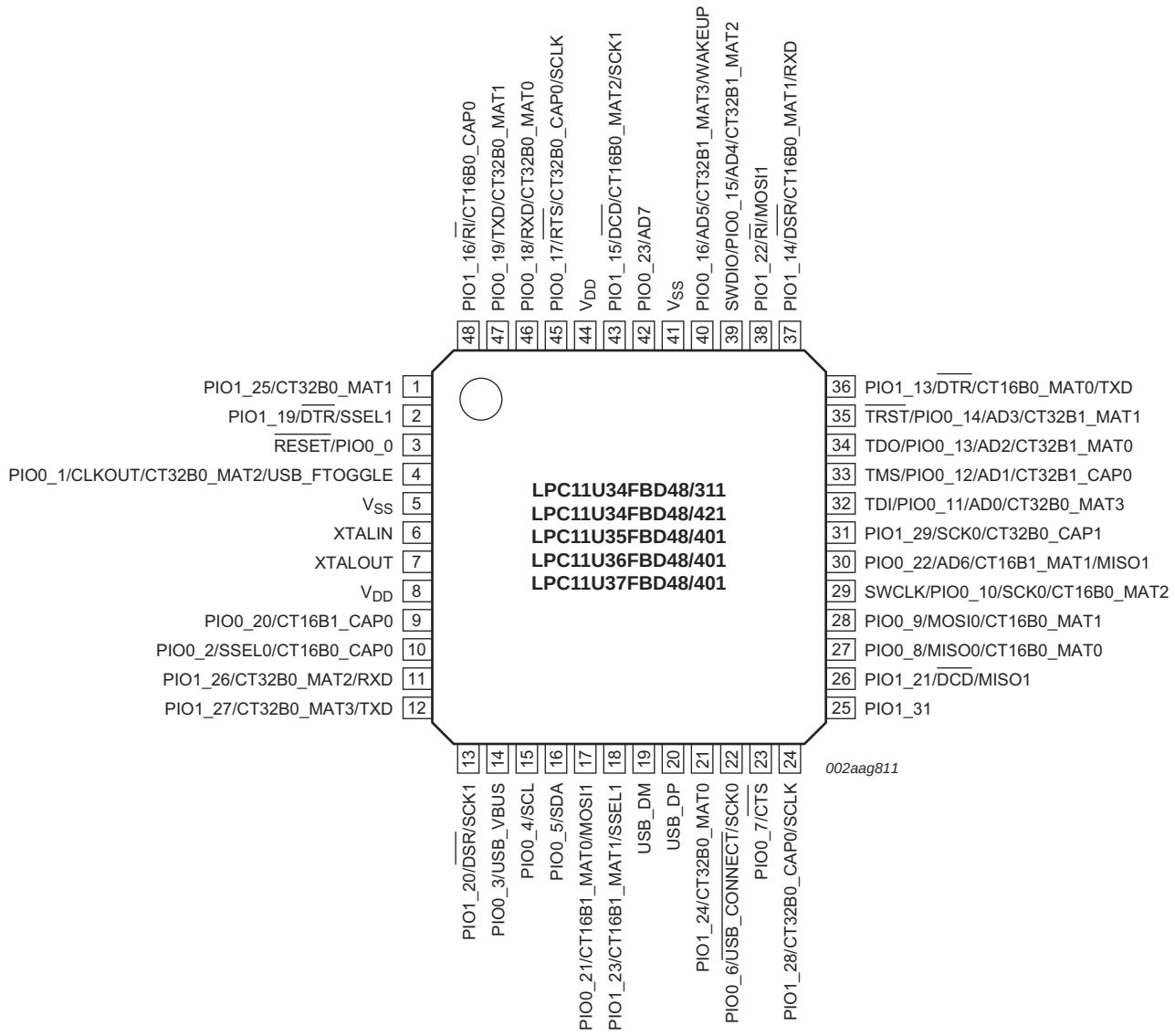



**Fig 4. Pin configuration (LQFP48)**

**Table 3. Pin description**

| Symbol | Pin HVQFN33 | Pin TFBGA48 | Pin LQFP48 | Pin LQFP64 | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|
| PIO0_4/SCL/IOH_2 | 10 | G3 | 15 | 20 [4] | I; IA | I/O | **PIO0_4 —** General purpose digital input/output pin (open-drain). |
| | | | | | - | I/O | **SCL —** $I^2C$-bus clock input/output (open-drain). High-current sink only if $I^2C$ Fast-mode Plus is selected in the I/O configuration register. |
| | | | | | - | I/O | **IOH_2 —** I/O Handler input/output 2. LPC11U37HFBD64/401 only. |
| PIO0_5/SDA/IOH_3 | 11 | H3 | 16 | 21 [4] | I; IA | I/O | **PIO0_5 —** General purpose digital input/output pin (open-drain). |
| | | | | | - | I/O | **SDA —** $I^2C$-bus data input/output (open-drain). High-current sink only if $I^2C$ Fast-mode Plus is selected in the I/O configuration register. |
| | | | | | - | I/O | **IOH_3 —** I/O Handler input/output 3. LPC11U37HFBD64/401 only. |
| PIO0_6/$\overline{\text{USB\_CONNECT}}$/SCK0/IOH_4 | 15 | H6 | 22 | 29 [3] | I; PU | I/O | **PIO0_6 —** General purpose digital input/output pin. |
| | | | | | - | O | **$\overline{\text{USB\_CONNECT}}$ —** Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature. |
| | | | | | - | I/O | **SCK0 —** Serial clock for SSP0. |
| | | | | | - | I/O | **IOH_4 —** I/O Handler input/output 4. LPC11U37HFBD64/401 only. |
| PIO0_7/$\overline{\text{CTS}}$/IOH_5 | 16 | G7 | 23 | 30 [5] | I; PU | I/O | **PIO0_7 —** General purpose digital input/output pin (high-current output driver). |
| | | | | | - | I | **$\overline{\text{CTS}}$ —** Clear To Send input for USART. |
| | | | | | - | I/O | **IOH_5 —** I/O Handler input/output 5. (LPC11U37HFBD64/401 only.) |
| PIO0_8/MISO0/CT16B0_MAT0/R/IOH_6 | 17 | F8 | 27 | 36 [3] | I; PU | I/O | **PIO0_8 —** General purpose digital input/output pin. |
| | | | | | - | I/O | **MISO0 —** Master In Slave Out for SSP0. |
| | | | | | - | O | **CT16B0_MAT0 —** Match output 0 for 16-bit timer 0. |
| | | | | | - | - | Reserved. |
| | | | | | - | I/O | **IOH_6 —** I/O Handler input/output 6. (LPC11U37HFBD64/401 only.) |
| PIO0_9/MOSI0/CT16B0_MAT1/R/IOH_7 | 18 | F7 | 28 | 37 [3] | I; PU | I/O | **PIO0_9 —** General purpose digital input/output pin. |
| | | | | | - | I/O | **MOSI0 —** Master Out Slave In for SSP0. |
| | | | | | - | O | **CT16B0_MAT1 —** Match output 1 for 16-bit timer 0. |
| | | | | | - | - | Reserved. |
| | | | | | - | I/O | **IOH_7 —** I/O Handler input/output 7. (LPC11U37HFBD64/401 only.) |

# 7. Functional description

## 7.1 On-chip flash programming memory

The LPC11U3x contain up to 128 kB on-chip flash program memory. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip boot loader software.

The flash memory is divided into 4 kB sectors with each sector consisting of 16 pages. Individual pages can be erased using the IAP erase page command.

## 7.2 EEPROM

The LPC11U3x contain 4 kB of on-chip byte-erasable and byte-programmable EEPROM data memory. The EEPROM can be programmed using In-Application Programming (IAP) via the on-chip boot loader software.

## 7.3 SRAM

The LPC11U3x contain a total of 8 kB, 10 kB, or 12 kB on-chip static RAM memory.

On the LPC11U37HFBD64/401, the 2 kB SRAM1 region at location 0x2000 0000 to 0x2000 07FFF is used for the I/O Handler software library. Do not use this memory location for data or other user code.

## 7.4 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.
- IAP support for EEPROM
- USB API
- Power profiles for configuring power consumption and PLL settings
- 32-bit integer division routines

## 7.5 Memory map

The LPC11U3x incorporates several distinct memory regions, shown in the following figures. Figure 6 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB (Advanced High-performance Bus) peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB (Advanced Peripheral Bus) peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This addressing scheme allows simplifying the address decoding for each peripheral.

### 7.8.1 Features

- GPIO pins can be configured as input or output by software.
- All GPIO pins default to inputs with interrupt disabled at reset.
- Pin registers allow pins to be sensed and set individually.
- Up to eight GPIO pins can be selected from all GPIO pins to create an edge- or level-sensitive GPIO interrupt request.
- Any pin or pins in each port can trigger a port interrupt.

## 7.9 USB interface

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot-plugging and dynamic configuration of the devices. The host controller initiates all transactions.

The LPC11U3x USB interface consists of a full-speed device controller with on-chip PHY (PHYsical layer) for device functions.

**Remark:** Configure the LPC11U3x in default power mode with the power profiles before using the USB (see Section 7.18.5.1). Do not use the USB with the part in performance, efficiency, or low-power mode.

### 7.9.1 Full-speed USB device controller

The device controller enables 12 Mbit/s data exchange with a USB Host controller. It consists of a register interface, serial interface engine, and endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. If enabled, an interrupt is generated.

#### 7.9.1.1 Features

- Dedicated USB PLL available.
- Fully compliant with *USB 2.0 specification (full speed)*.
- Supports 10 physical (5 logical) endpoints including one control endpoint.
- Single and double buffering supported.
- Each non-control endpoint supports bulk, interrupt, or isochronous endpoint types.
- Supports wake-up from Deep-sleep mode and Power-down mode on USB activity and remote wake-up.
- Supports SoftConnect.

## 7.10 I/O Handler (LPC11U37HFBD64/401 only)

The I/O Handler is a software library-supported hardware engine for emulating serial interfaces and off-loading the CPU for processing-intensive functions. The I/O Handler can emulate, among others, DMA and serial interfaces such as UART, $I^2C$, or $I^2S$ with no or very low additional CPU load. The software libraries are available with supporting

# 8. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*[1]

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage (core and external rail) | [2] | –0.5 | +4.6 | V |
| $V_I$ | input voltage | 5 V tolerant digital I/O pins; $V_{DD} \geq 1.8$ V [5][2] | –0.5 | +5.5 | V |
| | | $V_{DD} = 0$ V | –0.5 | +3.6 | V |
| | | 5 V tolerant open-drain pins PIO0_4 and PIO0_5 [2][4] | –0.5 | +5.5 | |
| $V_{IA}$ | analog input voltage | pin configured as analog input [2] [3] | –0.5 | 4.6 | V |
| $I_{DD}$ | supply current | per supply pin | - | 100 | mA |
| $I_{SS}$ | ground current | per ground pin | - | 100 | mA |
| $I_{latch}$ | I/O latch-up current | $-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C | - | 100 | mA |
| $T_{stg}$ | storage temperature | non-operating [6] | –65 | +150 | °C |
| $T_{j(max)}$ | maximum junction temperature | | - | 150 | °C |
| $P_{tot(pack)}$ | total power dissipation (per package) | based on package heat transfer, not device power consumption | - | 1.5 | W |
| $V_{ESD}$ | electrostatic discharge voltage | human body model; all pins [7] | - | +6500 | V |

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to $V_{SS}$ unless otherwise noted.

c) The limiting values are stress ratings only. Operating the part at these values is not recommended, and proper operation is not guaranteed. The conditions for functional operation are specified in Table 5.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 5) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] See Table 6 for maximum operating voltage.

[4] $V_{DD}$ present or not present. Compliant with the $I^2C$-bus standard. 5.5 V can be applied to this pin when $V_{DD}$ is powered down.

[5] Including voltage on outputs in 3-state mode.

[6] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC spec (J-STD-033B.1) for further details.

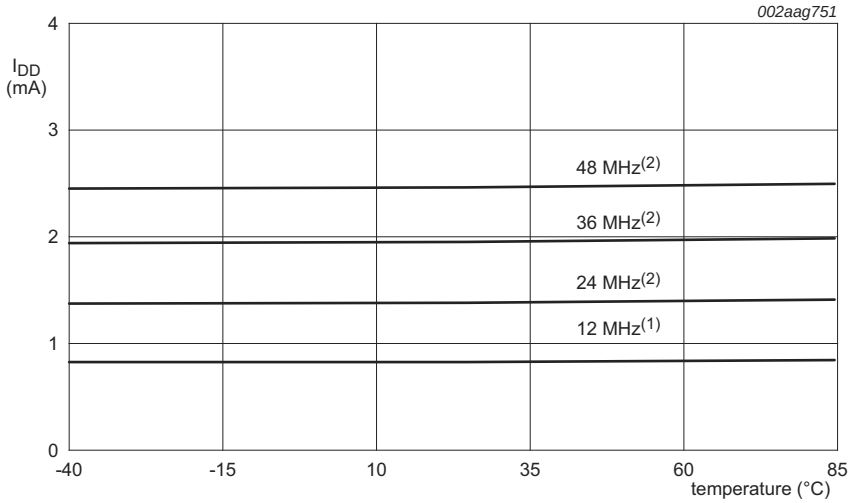
[7] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

# 9. Static characteristics

**Table 5. Static characteristics**

*$T_{amb}$ = −40 °C to +85 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage (core and external rail) | [2] | 1.8 | 3.3 | 3.6 | V |
| $I_{DD}$ | supply current | Active mode; $V_{DD}$ = 3.3 V; $T_{amb}$ = 25 °C; code `while(1){}` executed from flash; | | | | |
| | | system clock = 12 MHz [3][4][5][6][7][8] | - | 2 | - | mA |
| | | system clock = 50 MHz [4][5][6][7][8][9] | - | 7 | - | mA |
| | | Sleep mode; $V_{DD}$ = 3.3 V; $T_{amb}$ = 25 °C; system clock = 12 MHz [3][4][5][6][7][8] | - | 1 | - | mA |
| | | Deep-sleep mode; $V_{DD}$ = 3.3 V; $T_{amb}$ = 25 °C [4][7] | - | 300 | - | μA |
| | | Power-down mode; $V_{DD}$ = 3.3 V; $T_{amb}$ = 25 °C | - | 2 | - | μA |
| | | Deep power-down mode; $V_{DD}$ = 3.3 V; $T_{amb}$ = 25 °C [10] | - | 220 | - | nA |
| **Standard port pins, $\overline{\text{RESET}}$** | | | | | | |
| $I_{IL}$ | LOW-level input current | $V_I$ = 0 V; on-chip pull-up resistor disabled | - | 0.5 | 10 | nA |
| $I_{IH}$ | HIGH-level input current | $V_I$ = $V_{DD}$; on-chip pull-down resistor disabled | - | 0.5 | 10 | nA |
| $I_{OZ}$ | OFF-state output current | $V_O$ = 0 V; $V_O$ = $V_{DD}$; on-chip pull-up/down resistors disabled | - | 0.5 | 10 | nA |
| $V_I$ | input voltage | pin configured to provide a digital function; $V_{DD} \geq 1.8$ V [11][12] | 0 | - | 5.0 | V |
| | | $V_{DD}$ = 0 V | 0 | - | 3.6 | V |
| $V_O$ | output voltage | output active | 0 | - | $V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{DD}$ | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | - | - | $0.3V_{DD}$ | V |
| $V_{hys}$ | hysteresis voltage | | - | 0.4 | - | V |
| $V_{OH}$ | HIGH-level output voltage | 2.0 V ≤ $V_{DD}$ ≤ 3.6 V; $I_{OH}$ = −4 mA | $V_{DD}$ − 0.4 | - | - | V |
| | | 1.8 V ≤ $V_{DD}$ < 2.0 V; $I_{OH}$ = −3 mA | $V_{DD}$ − 0.4 | - | - | V |
| $V_{OL}$ | LOW-level output voltage | 2.0 V ≤ $V_{DD}$ ≤ 3.6 V; $I_{OL}$ = 4 mA | - | - | 0.4 | V |
| | | 1.8 V ≤ $V_{DD}$ < 2.0 V; $I_{OL}$ = 3 mA | - | - | 0.4 | V |
| $I_{OH}$ | HIGH-level output current | $V_{OH}$ = $V_{DD}$ − 0.4 V; 2.0 V ≤ $V_{DD}$ ≤ 3.6 V | −4 | - | - | mA |
| | | 1.8 V ≤ $V_{DD}$ < 2.0 V | −3 | - | - | mA |

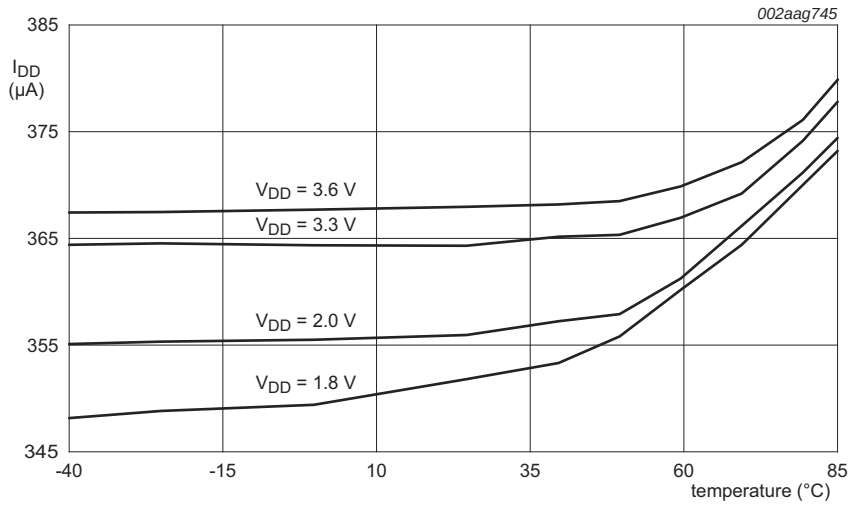



Conditions: $V_{DD}$ = 3.3 V; Sleep mode entered from flash; internal pull-up resistors disabled; BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; low-current mode; USB_DP and USB_DM pulled LOW externally.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

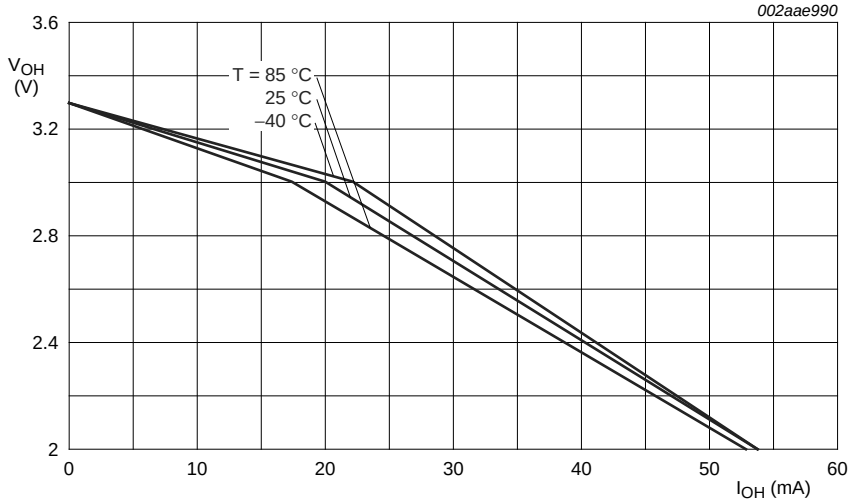
**Fig 11. Typical supply current versus temperature in Sleep mode**




Conditions: BOD disabled; all oscillators and analog blocks turned off in the PDSLEEPCFG register; USB_DP and USB_DM pulled LOW externally.

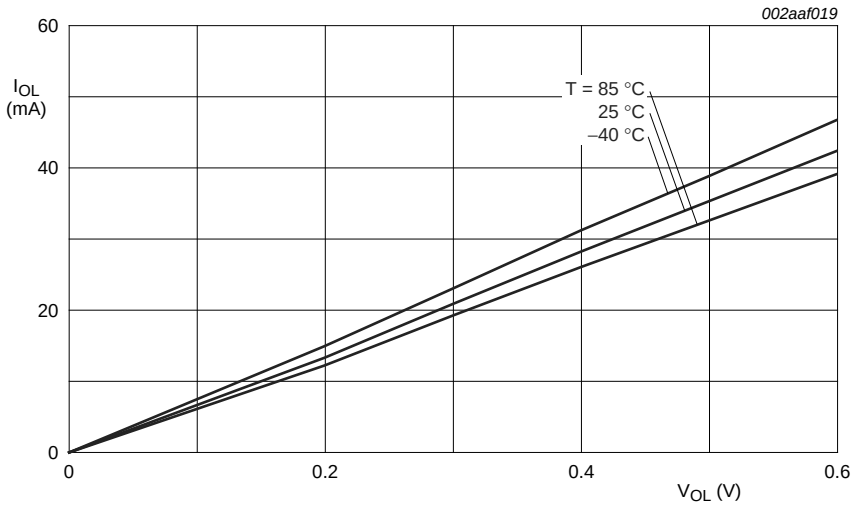
**Fig 12. Typical supply current versus temperature in Deep-sleep mode**

## 9.4 Electrical pin characteristics




Conditions: $V_{DD}$ = 3.3 V; on pin PIO0_7.

**Fig 15. High-drive output: Typical HIGH-level output voltage $V_{OH}$ versus HIGH-level output current $I_{OH}$.**




Conditions: $V_{DD}$ = 3.3 V; on pins PIO0_4 and PIO0_5.

**Fig 16. $I^2C$-bus pins (high current sink): Typical LOW-level output current $I_{OL}$ versus LOW-level output voltage $V_{OL}$**

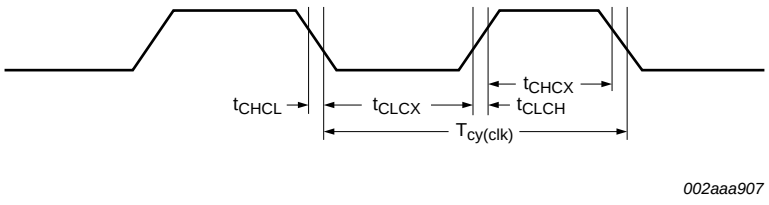



**Fig 21. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)**

## 10.3 Internal oscillators

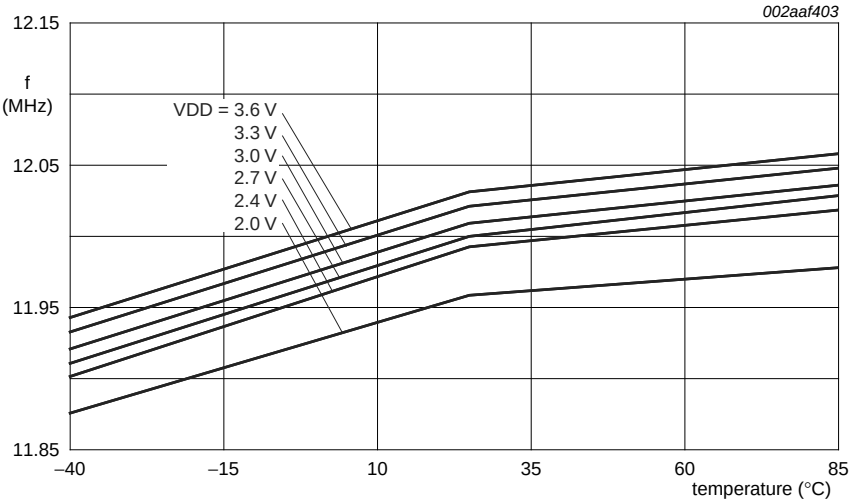
**Table 12. Dynamic characteristics: IRC**

*$T_{amb}$ = −40 °C to +85 °C; 2.7 V ≤ $V_{DD}$ ≤ 3.6 V*[1].

| Symbol | Parameter | Conditions | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{osc(RC)}$ | internal RC oscillator frequency | - | 11.88 | 12 | 12.12 | MHz |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.




Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ $V_{DD}$ ≤ 3.6 V and $T_{amb}$ = −40 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

**Fig 22. Internal RC oscillator frequency versus temperature**

**Table 13. Dynamic characteristics: Watchdog oscillator**

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{osc(int)}$ | internal oscillator frequency | DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register; [2][3] | - | 9.4 | - | kHz |
| | | DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register [2][3] | - | 2300 | - | kHz |

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature ($T_{amb}$ = −40 °C to +85 °C) is ±40 %.

[3] See the *LPC11Uxx user manual.*

## 10.4 I/O pins

**Table 14. Dynamic characteristics: I/O pins[1]**

*$T_{amb}$ = −40 °C to +85 °C; 3.0 V ≤ $V_{DD}$ ≤ 3.6 V.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_r$ | rise time | pin configured as output | 3.0 | - | 5.0 | ns |
| $t_f$ | fall time | pin configured as output | 2.5 | - | 5.0 | ns |

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

## 10.5 I²C-bus

**Table 15. Dynamic characteristic: I²C-bus pins[1]**

*$T_{amb}$ = −40 °C to +85 °C.[2]*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | Standard-mode | 0 | 100 | kHz |
| | | Fast-mode | 0 | 400 | kHz |
| | | Fast-mode Plus | 0 | 1 | MHz |
| $t_f$ | fall time [4][5][6][7] | of both SDA and SCL signals<br>Standard-mode | - | 300 | ns |
| | | Fast-mode | 20 + 0.1 × $C_b$ | 300 | ns |
| | | Fast-mode Plus | - | 120 | ns |
| $t_{LOW}$ | LOW period of the SCL clock | Standard-mode | 4.7 | - | µs |
| | | Fast-mode | 1.3 | - | µs |
| | | Fast-mode Plus | 0.5 | - | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | Standard-mode | 4.0 | - | µs |
| | | Fast-mode | 0.6 | - | µs |
| | | Fast-mode Plus | 0.26 | - | µs |
| $t_{HD;DAT}$ | data hold time [3][4][8] | Standard-mode | 0 | - | µs |
| | | Fast-mode | 0 | - | µs |
| | | Fast-mode Plus | 0 | - | µs |
| $t_{SU;DAT}$ | data set-up time [9][10] | Standard-mode | 250 | - | ns |
| | | Fast-mode | 100 | - | ns |
| | | Fast-mode Plus | 50 | - | ns |

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH}$(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] $C_b$ = total capacitance of one bus line in pF.

[6] The maximum $t_f$ for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage $t_f$ is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified $t_f$.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period ($t_{LOW}$) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode $I^2C$-bus device can be used in a Standard-mode $I^2C$-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode $I^2C$-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

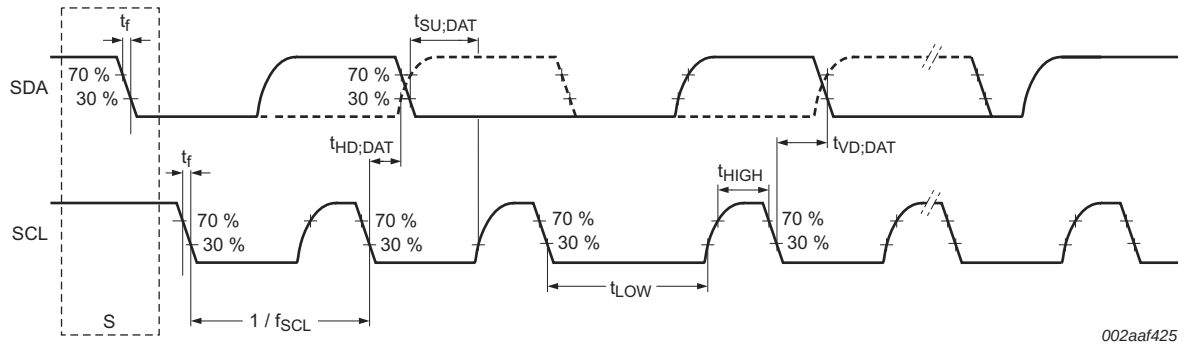



**Fig 23. $I^2C$-bus pins clock timing**

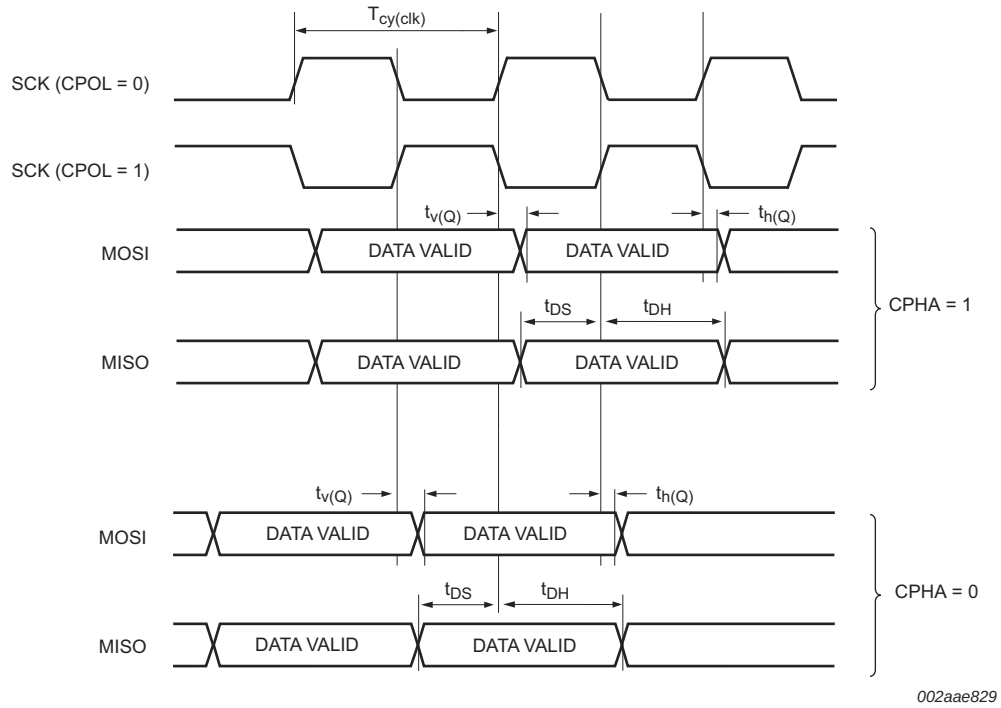



**Fig 24. SSP master timing in SPI mode**

### 11.8.3 I/O Handler I²C

The I/O Handler I²C library allows to have an additional I²C-bus master. I²C read, I²C write and combined I²C read/write are supported. Data is automatically read from and written to user-defined buffers.

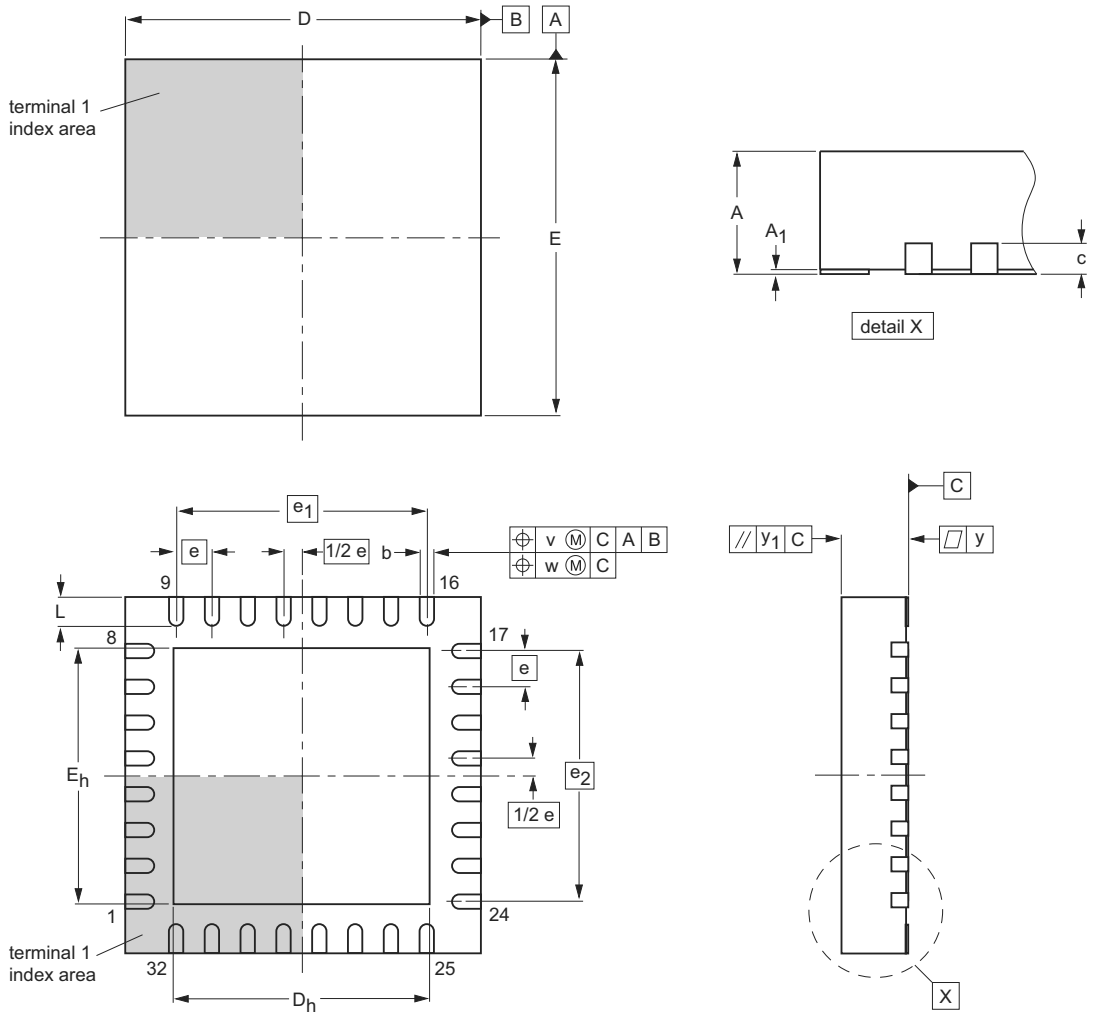
The I/O Handler I²C library combined with the on-chip I²C module allows to have two distinct I²C buses, allowing to separate low-speed from high-speed devices or bridging two I²C buses.

### 11.8.4 I/O Handler DMA

The I/O Handler DMA library offers DMA-like functionality. Four types of transfer are supported: memory to memory, memory to peripheral, peripheral to memory and peripheral to peripheral. Supported peripherals are USART, SSP0/1, ADC and GPIO. DMA transfers can be triggered by the source/target peripheral, software, counter/timer module CT16B1, or I/O Handler pin PIO1_6/IOH_16.

# 12. Package outline

**HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm**




Dimensions (mm are the original dimensions)

| Unit[1] | | A[1] | $A_1$ | b | c | D[1] | $D_h$ | E[1] | $E_h$ | e | $e_1$ | $e_2$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.85 | 0.05 | 0.30 | 0.2 | 5.1 | 3.75 | 5.1 | 3.75 | 0.5 | 3.5 | 3.5 | 0.5 | 0.1 | 0.05 | 0.05 | 0.1 |
| | nom | | | | | | | | | | | | | | | | |
| | min | | 0.00 | 0.18 | | 4.9 | 3.45 | 4.9 | 3.45 | | | | 0.3 | | | | |

Note

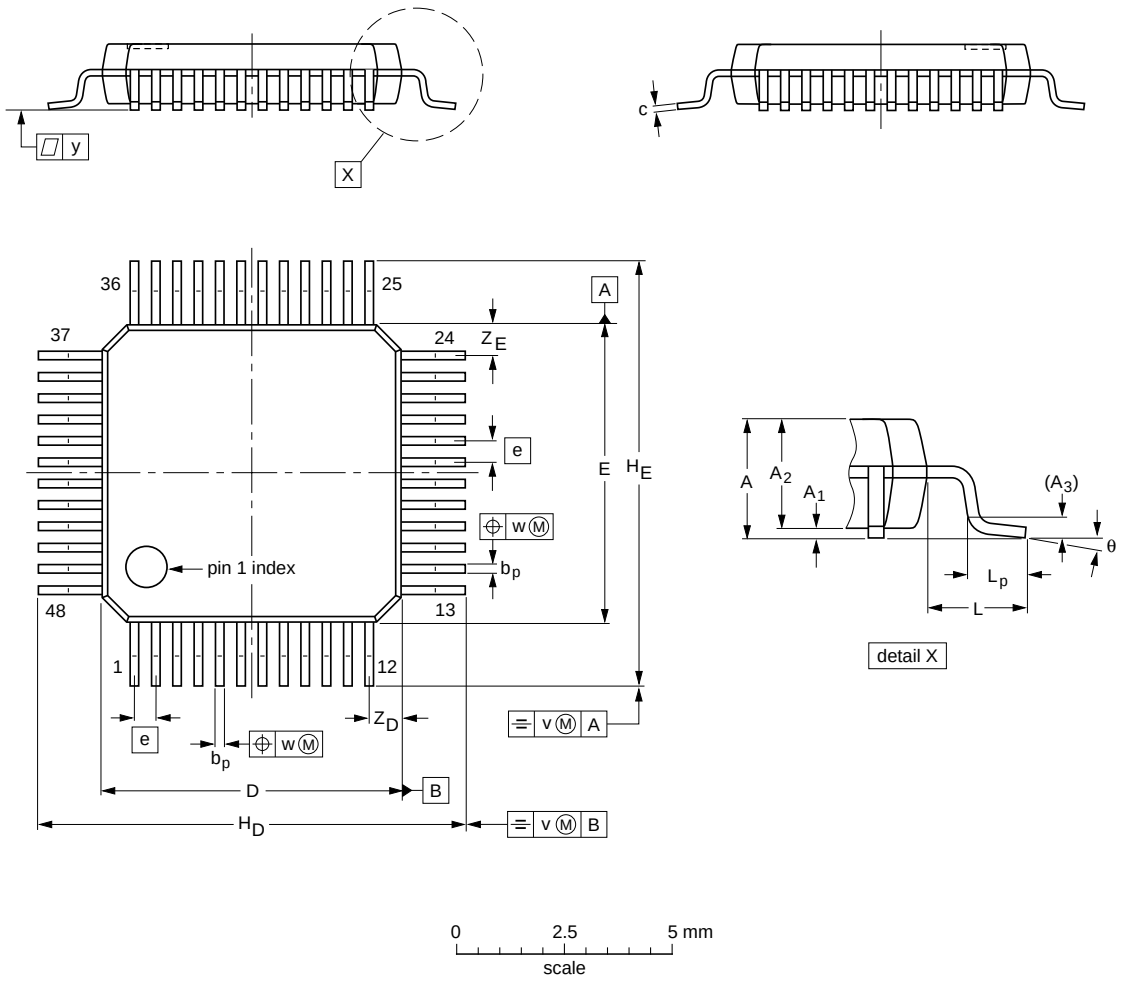
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

*hvqfn33f_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| | | MO-220 | | | | ~~11-10-11~~ 11-10-17 |

**Fig 34. Package outline HVQFN33 (5 x 5 x 0.85 mm)**

**LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm** **SOT313-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.6 | 0.20<br>0.05 | 1.45<br>1.35 | 0.25 | 0.27<br>0.17 | 0.18<br>0.12 | 7.1<br>6.9 | 7.1<br>6.9 | 0.5 | 9.15<br>8.85 | 9.15<br>8.85 | 1 | 0.75<br>0.45 | 0.2 | 0.12 | 0.1 | 0.95<br>0.55 | 0.95<br>0.55 | $7^o$<br>$0^o$ |

**Note**

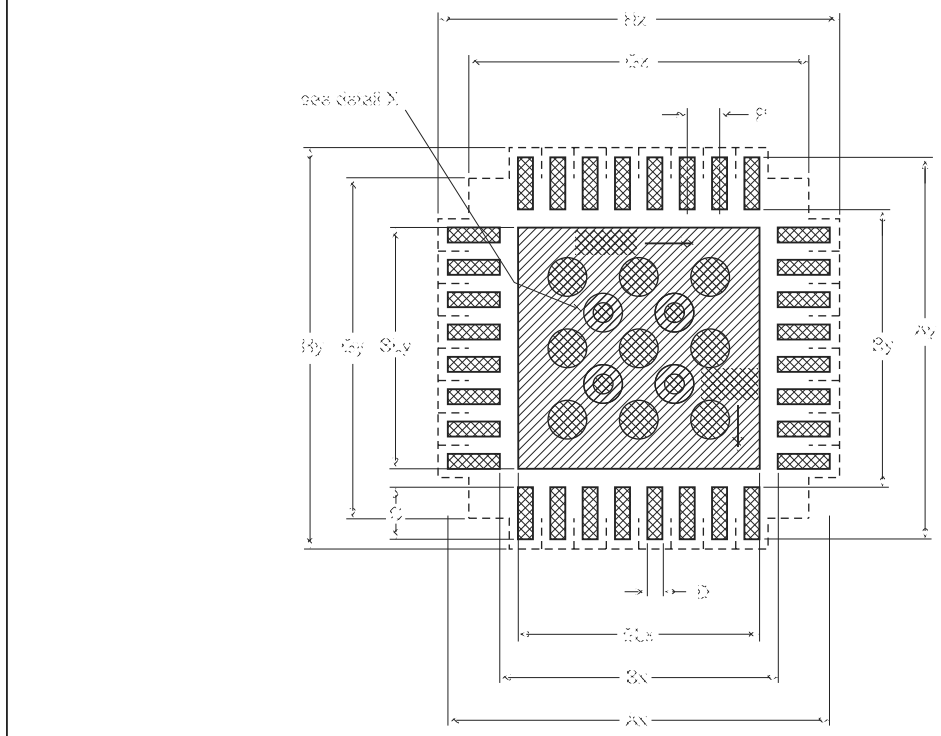
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT313-2 | 136E05 | MS-026 | | | | ~~00-01-19~~<br>03-02-25 |

**Fig 37. Package outline LQFP48 (SOT313-2)**

# 13. Soldering

**Footprint information for reflow soldering of HVQFN33 package**




Dimensions in mm

| P | Ax | Ay | Bx | By | C | D | Gx | Gy | Hx | Hy | SLx | SLy | nSPx | nSPy |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.5 | 5.95 | 5.95 | 4.25 | 4.25 | 0.85 | 0.27 | 5.25 | 5.25 | 6.2 | 6.2 | 3.75 | 3.75 | 3 | 3 |

Issue date ~~11-11-15~~ 11-11-20

002aag766

**Fig 39. Reflow soldering for the HVQFN33 (5x5) package**

# 14. Abbreviations

**Table 20. Abbreviations**

| Acronym | Description |
|---|---|
| A/D | Analog-to-Digital |
| ADC | Analog-to-Digital Converter |
| AHB | Advanced High-performance Bus |
| APB | Advanced Peripheral Bus |
| BOD | BrownOut Detection |
| GPIO | General Purpose Input/Output |
| JTAG | Joint Test Action Group |
| PLL | Phase-Locked Loop |
| RC | Resistor-Capacitor |
| SPI | Serial Peripheral Interface |
| SSI | Serial Synchronous Interface |
| SSP | Synchronous Serial Port |
| TAP | Test Access Port |
| USART | Universal Synchronous Asynchronous Receiver/Transmitter |

# 15. References

[1] LPC11U3x User manual UM10462:
http://www.nxp.com/documents/user_manual/UM10462.pdf

[2] LPC11U3x Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC11U3X.pdf

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 8 February 2017**
**Document identifier: LPC11U3X**