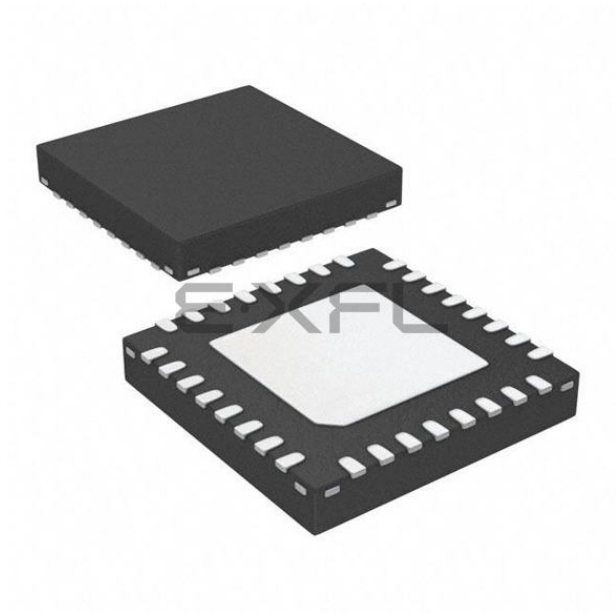

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SmartCard, SPI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	26
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11u34fhn33-421

- 4 kB on-chip EEPROM data memory; byte erasable and byte programmable; on-chip API support.
- Up to 12 kB SRAM data memory.
- 16 kB boot ROM.
- In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
- ROM-based USB drivers. Flash updates via USB supported.
- ROM-based 32-bit integer division routines.

- Debug options:
  - Standard JTAG (Joint Test Action Group) test interface for BSDL (Boundary Scan Description Language).
  - Serial Wire Debug.
- Digital peripherals:
  - Up to 54 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, repeater mode, and open-drain mode.
  - Up to 8 GPIO pins can be selected as edge and level sensitive interrupt sources.
  - Two GPIO grouped interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
  - High-current source output driver (20 mA) on one pin.
  - High-current sink driver (20 mA) on true open-drain pins.
  - Four general purpose counter/timers with a total of up to 8 capture inputs and 13 match outputs.
  - Programmable Windowed WatchDog Timer (WWDT) with a dedicated, internal low-power WatchDog Oscillator (WDO).
- Analog peripherals:
  - 10-bit ADC with input multiplexing among eight pins.
- Serial interfaces:
  - USB 2.0 full-speed device controller.
  - USART with fractional baud rate generation, internal FIFO, a full modem control handshake interface, and support for RS-485/9-bit mode and synchronous mode. USART supports an asynchronous smart card interface (ISO 7816-3).
  - Two SSP controllers with FIFO and multi-protocol capabilities.
  - I^2C-bus interface supporting the full I^2C-bus specification and Fast-mode Plus with a data rate of up to 1 Mbit/s with multiple address recognition and monitor mode.
- I/O Handler for hardware emulation of serial interfaces and DMA; supported through software libraries. (LPC11U37HFBD64/401 only.)
- Clock generation:
  - Crystal Oscillator with an operating range of 1 MHz to 25 MHz (system oscillator).
  - 12 MHz high-frequency Internal RC oscillator (IRC) that can optionally be used as a system clock.
  - Internal low-power, low-frequency WatchDog Oscillator (WDO) with programmable frequency output.
  - PLL allows CPU operation up to the maximum CPU rate with the system oscillator or the IRC as clock sources.
  - A second, dedicated PLL is provided for USB.

- Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.

- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.
  - Power profiles residing in boot ROM provide optimized performance and minimized power consumption for any given application through one simple function call.
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Processor wake-up from Deep-sleep and Power-down modes via reset, selectable GPIO pins, watchdog interrupt, or USB port activity.
  - Processor wake-up from Deep power-down mode using one special function pin.
  - Power-On Reset (POR).
  - Brownout detect with up to four separate thresholds for interrupt and forced reset.
- Unique device serial number for identification.
- Single 3.3 V power supply (1.8 V to 3.6 V).
- Temperature range −40 °C to +85 °C.
- Available as LQFP64, LQFP48, TFBGA48, and HVQFN33 packages.

3. Applications

- Consumer peripherals
- Medical
- Industrial control
- Handheld scanners
- USB audio devices

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC11U34FHN33/311	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11U34FBD48/311	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U34FHN33/421	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11U34FBD48/421	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U35FHN33/401	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11U35FBD48/401	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U35FBD64/401	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11U35FHI33/501	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC11U35FET48/501	TFBGA48	plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 × 4.5 × 0.7 mm	SOT1155-2
LPC11U36FBD48/401	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

Table 1. Ordering information *…continued*

Type number	Package		
	Name	Description	Version
LPC11U36FBD64/401	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11U37FBD48/401	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U37HFBD64/401	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11U37FBD64/501	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

4.1 Ordering options

Table 2. Ordering options

Type number	Flash in kB	EEPROM in kB	SRAM0 in kB	USB SRAM in kB	SRAM1 in kB	Total SRAM in kB[1]	I/O Handler	USART	I²C-bus FM+	SSP	USB device	ADC channels	GPIO pins
LPC11U34FHN33/311	40	4	8	-	-	8	no	1	1	2	1	8	26
LPC11U34FBD48/311	40	4	8	-	-	8	no	1	1	2	1	8	40
LPC11U34FHN33/421	48	4	8	2	-	10	no	1	1	2	1	8	26
LPC11U34FBD48/421	48	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U35FHN33/401	64	4	8	2	-	10	no	1	1	2	1	8	26
LPC11U35FBD48/401	64	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U35FBD64/401	64	4	8	2	-	10	no	1	1	2	1	8	54
LPC11U35FHI33/501	64	4	8	2	2[1]	12	no	1	1	2	1	8	26
LPC11U35FET48/501	64	4	8	2	2[1]	12	no	1	1	2	1	8	40
LPC11U36FBD48/401	96	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U36FBD64/401	96	4	8	2	-	10	no	1	1	2	1	8	54
LPC11U37FBD48/401	128	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U37HFBD64/401	128	4	8	2	2[2]	10	yes	1	1	2	1	8	54
LPC11U37FBD64/501	128	4	8	2	2[1]	12	no	1	1	2	1	8	54

[1] For general-purpose use.

[2] For I/O Handler use only.

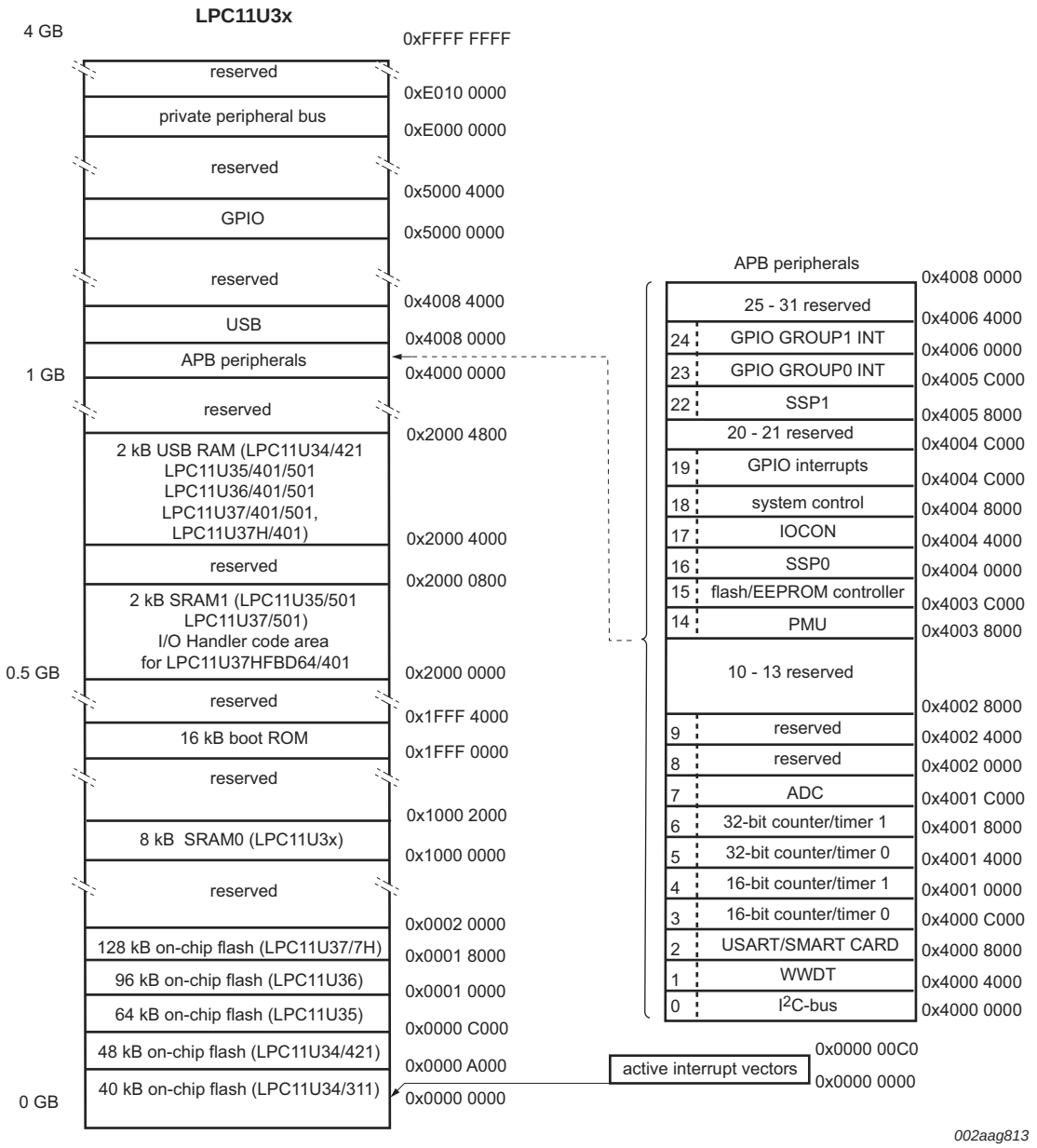


Fig 6. LPC11U3x memory map

7.6 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC11U3x, the NVIC supports 24 vectored interrupts.

7.15 General purpose external event counter/timers

The LPC11U3x includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.15.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- Up to two capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event can also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler can be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.

7.16 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.17 Windowed WatchDog Timer (WWDT)

The purpose of the WWDT is to prevent an unresponsive system state. If software fails to update the watchdog within a programmable time window, the watchdog resets the microcontroller

7.17.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time before watchdog time-out.

7.18.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL. On the LPC11U3x, use the system oscillator to provide the clock source to USB.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

7.18.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over processing and temperature is ±40 % (see also Table 13).

7.18.2 System PLL and USB PLL

The LPC11U3x contain a system PLL and a dedicated PLL for generating the 48 MHz USB clock. The system and USB PLLs are identical.

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. To support this frequency range, an additional divider keeps the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. Software can enable the PLL later. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.18.3 Clock output

The LPC11U3x feature a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.18.4 Wake-up process

The LPC11U3x begin operation by using the 12 MHz IRC oscillator as the clock source at power-up and when awakened from Deep power-down mode . This mechanism allows chip operation to resume quickly. If the application uses the main oscillator or the PLL, software must enable these components and wait for them to stabilize. Only then can the system use the PLL and main oscillator as a clock source.

7.18.5 Power control

The LPC11U3x support various power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate can also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This power control mechanism allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals. This register allows fine-tuning of power

Power-down mode reduces power consumption compared to Deep-sleep mode at the expense of longer wake-up times.

7.18.5.5 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip except for the WAKEUP pin. The LPC11U3x can wake up from Deep power-down mode via the WAKEUP pin.

The LPC11U3x can be prevented from entering Deep power-down mode by setting a lock bit in the PMU block. Locking out Deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. Pull the $\overline{\text{RESET}}$ pin HIGH to prevent it from floating while in Deep power-down mode.

7.18.6 System control

7.18.6.1 Reset

Reset has four sources on the LPC11U3x: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

In Deep power-down mode, an external pull-up resistor is required on the $\overline{\text{RESET}}$ pin.

7.18.6.2 Brownout detection

The LPC11U3x includes up to four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Four threshold levels can be selected to cause a forced reset of the chip.

7.18.6.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details, see the *LPC11Uxx user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details, see the *LPC11Uxx user manual*.

7.18.6.4 APB interface

The APB peripherals are located on one APB bus.

7.18.6.5 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the ROM.

7.18.6.6 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs.

7.19 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0 is configured to support up to four breakpoints and two watch points.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC11U3x is in reset.

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

9. Static characteristics

Table 5. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)	[2]	1.8	3.3	3.6	V
I_{DD}	supply current	Active mode; V_{DD} = 3.3 V; T_{amb} = 25 °C; code `while(1){}` executed from flash;				
		system clock = 12 MHz [3][4][5][6][7][8]	-	2	-	mA
		system clock = 50 MHz [4][5][6][7][8][9]	-	7	-	mA
		Sleep mode; V_{DD} = 3.3 V; T_{amb} = 25 °C; system clock = 12 MHz [3][4][5][6][7][8]	-	1	-	mA
		Deep-sleep mode; V_{DD} = 3.3 V; T_{amb} = 25 °C [4][7]	-	300	-	μA
		Power-down mode; V_{DD} = 3.3 V; T_{amb} = 25 °C	-	2	-	μA
		Deep power-down mode; V_{DD} = 3.3 V; T_{amb} = 25 °C [10]	-	220	-	nA
Standard port pins, $\overline{\text{RESET}}$						
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled	-	0.5	10	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled	-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function; $V_{DD} \geq 1.8$ V [11][12]	0	-	5.0	V
		V_{DD} = 0 V	0	-	3.6	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage		-	0.4	-	V
V_{OH}	HIGH-level output voltage	2.0 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = −4 mA	V_{DD} − 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.0 V; I_{OH} = −3 mA	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.0 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA	-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.0 V; I_{OL} = 3 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 2.0 V ≤ V_{DD} ≤ 3.6 V	−4	-	-	mA
		1.8 V ≤ V_{DD} < 2.0 V	−3	-	-	mA

9.1 BOD static characteristics

Table 7. BOD static characteristics[1]
T_{amb} = 25 °C.

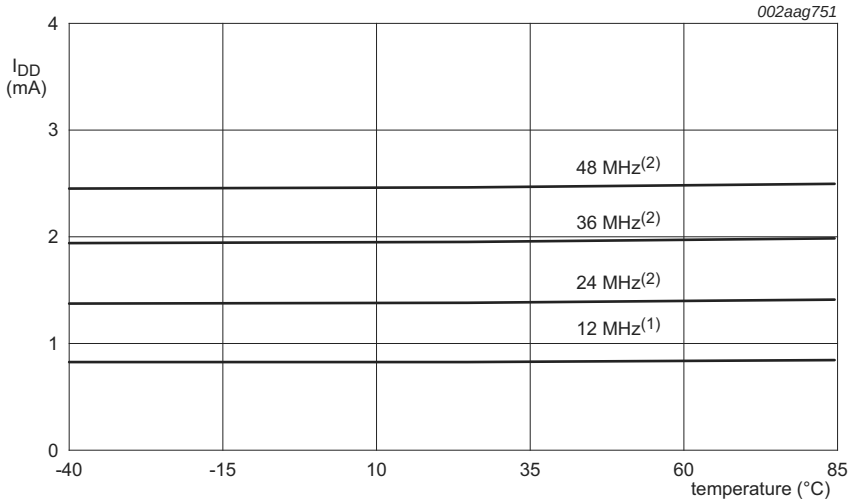
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1				
		assertion	-	2.22	-	V
		de-assertion	-	2.35	-	V
		interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V
		reset level 0				
		assertion	-	1.46	-	V
		de-assertion	-	1.63	-	V
		reset level 1				
		assertion	-	2.06	-	V
		de-assertion	-	2.15	-	V
		reset level 2				
		assertion	-	2.35	-	V
		de-assertion	-	2.43	-	V
		reset level 3				
		assertion	-	2.63	-	V
		de-assertion	-	2.71	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *the LPC11Uxx user manual*.

9.2 Power consumption

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see the *LPC11Uxx user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.

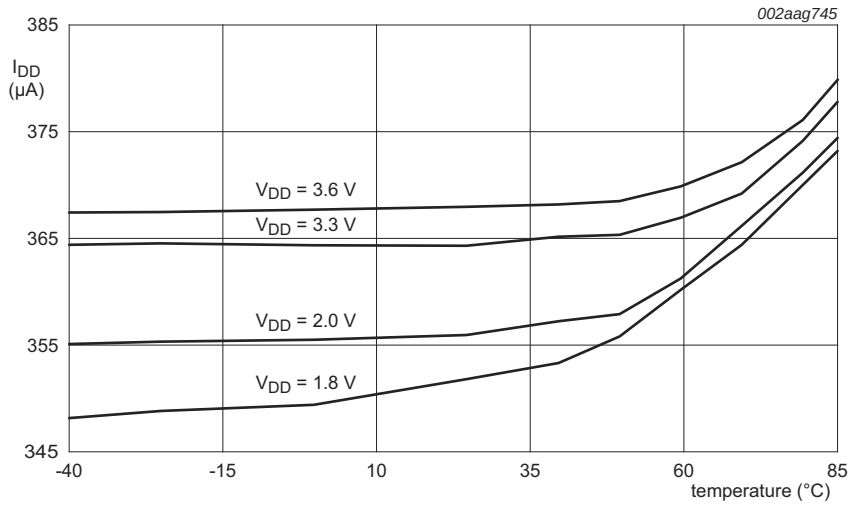


Conditions: V_{DD} = 3.3 V; Sleep mode entered from flash; internal pull-up resistors disabled; BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; low-current mode; USB_DP and USB_DM pulled LOW externally.

(1) System oscillator and system PLL disabled; IRC enabled.

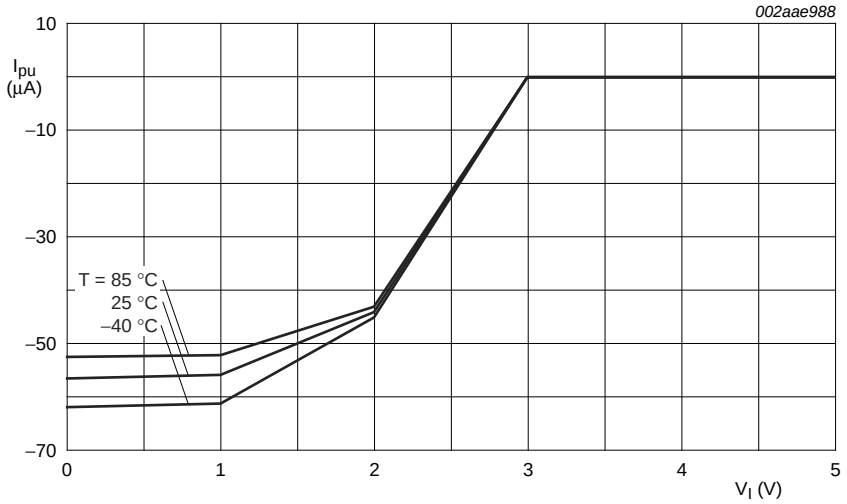
(2) System oscillator and system PLL enabled; IRC disabled.

Fig 11. Typical supply current versus temperature in Sleep mode



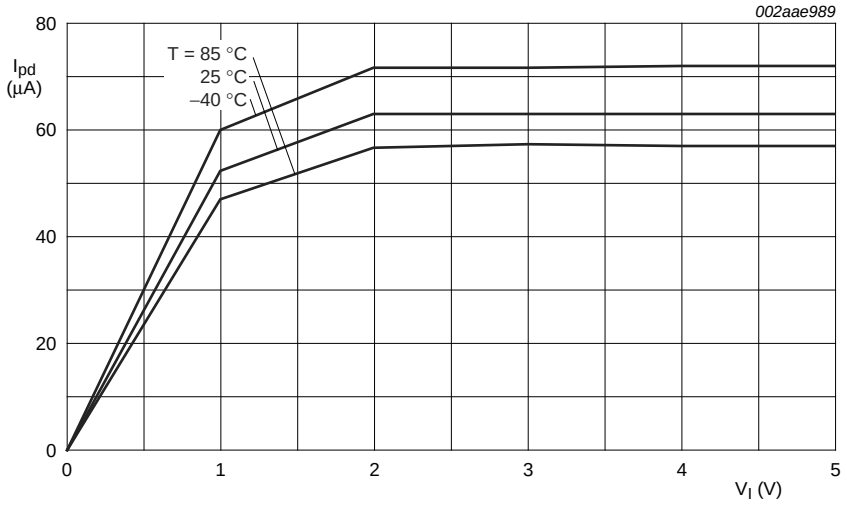
Conditions: BOD disabled; all oscillators and analog blocks turned off in the PDSLEEPCFG register; USB_DP and USB_DM pulled LOW externally.

Fig 12. Typical supply current versus temperature in Deep-sleep mode



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 19. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 20. Typical pull-down current I_{pd} versus input voltage V_I

10. Dynamic characteristics

10.1 Flash memory

Table 9. Flash characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance	[1]	10000	100000	-	cycles
t_{ret}	retention time	powered	10	-	-	years
		unpowered	20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors	95	100	105	ms
t_{prog}	programming time	[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

Table 10. EEPROM characteristics

T_{amb} = −40 °C to +85 °C; V_{DD} = 2.7 V to 3.6 V. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance		100000	1000000	-	cycles
t_{ret}	retention time	powered	100	200	-	years
		unpowered	150	300	-	years
t_{prog}	programming time	64 bytes	-	2.9	-	ms

10.2 External clock

Table 11. Dynamic characteristic: external clock

T_{amb} = −40 °C to +85 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

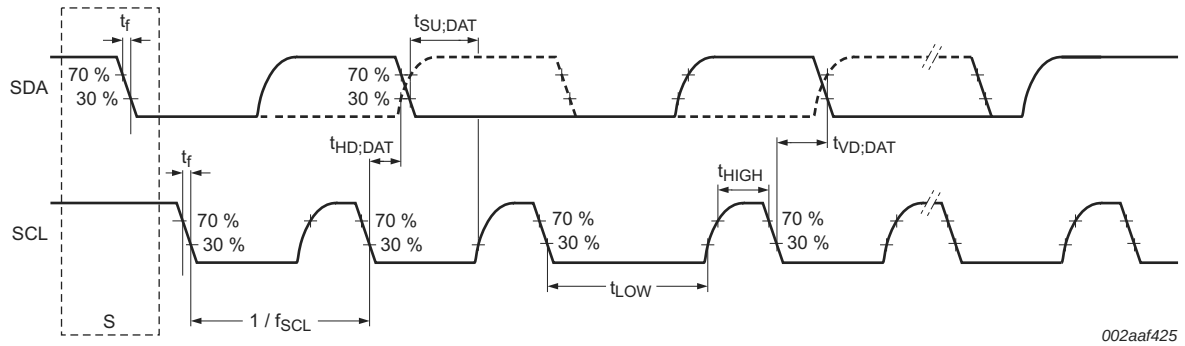


Fig 23. I^2C-bus pins clock timing

10.6 SSP interface

Table 16. Dynamic characteristics of SPI pins in SPI mode

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master (in SPI mode)							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	50	-	-	ns
		when only transmitting	[1]	40			ns
t_{DS}	data set-up time	in SPI mode $2.4\ V \leq V_{DD} \leq 3.6\ V$	[2]	15	-	-	ns
		$2.0\ V \leq V_{DD} < 2.4\ V$	[2]	20			ns
		$1.8\ V \leq V_{DD} < 2.0\ V$	[2]	24	-	-	ns
t_{DH}	data hold time	in SPI mode	[2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	0	-	-	ns
SPI slave (in SPI mode)							
$T_{cy(PCLK)}$	PCLK cycle time			20	-	-	ns
t_{DS}	data set-up time	in SPI mode	[3][4]	0	-	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	$3 \times T_{cy(PCLK)} + 4$	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	-	$3 \times T_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	-	$2 \times T_{cy(PCLK)} + 5$	ns

[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2] $T_{amb} = -40\ °C$ to $85\ °C$.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] $T_{amb} = 25\ °C$; for normal voltage supply range: $V_{DD} = 3.3\ V$.

11.8.3 I/O Handler I²C

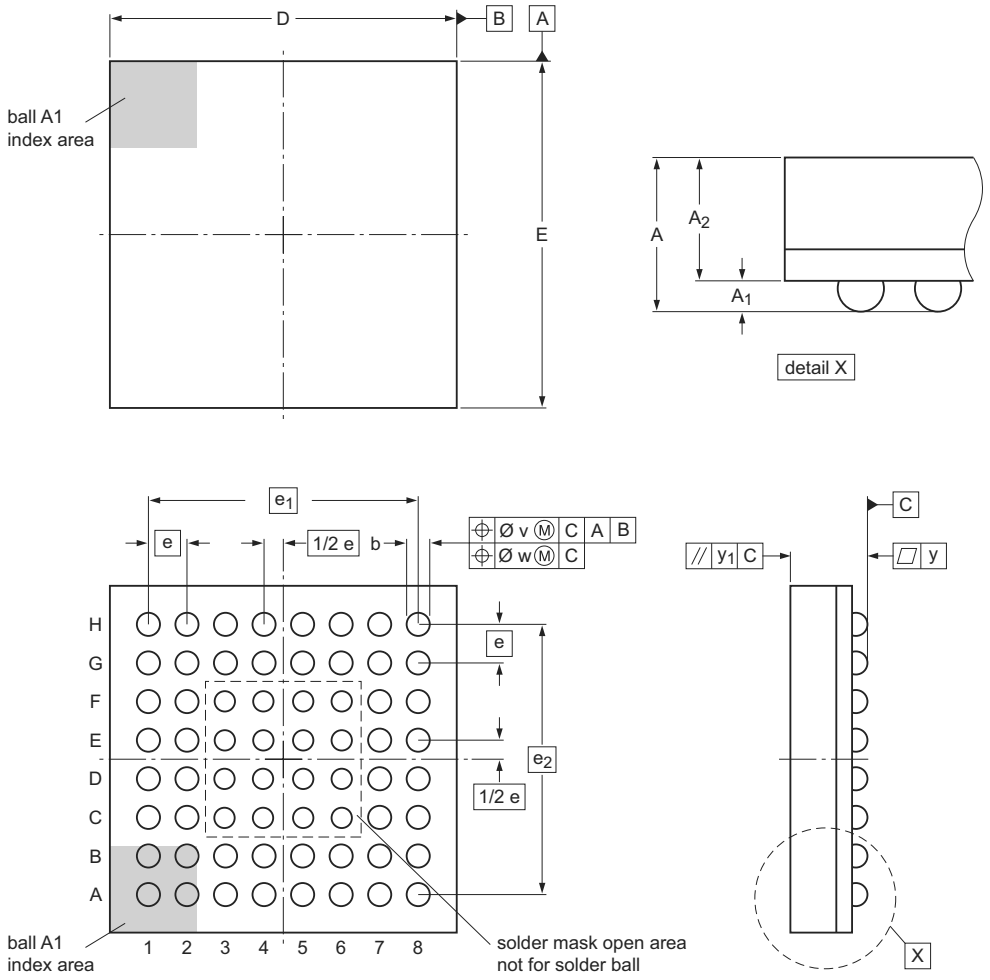
The I/O Handler I²C library allows to have an additional I²C-bus master. I²C read, I²C write and combined I²C read/write are supported. Data is automatically read from and written to user-defined buffers.

The I/O Handler I²C library combined with the on-chip I²C module allows to have two distinct I²C buses, allowing to separate low-speed from high-speed devices or bridging two I²C buses.

11.8.4 I/O Handler DMA

The I/O Handler DMA library offers DMA-like functionality. Four types of transfer are supported: memory to memory, memory to peripheral, peripheral to memory and peripheral to peripheral. Supported peripherals are USART, SSP0/1, ADC and GPIO. DMA transfers can be triggered by the source/target peripheral, software, counter/timer module CT16B1, or I/O Handler pin PIO1_6/IOH_16.

TFBGA48: plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 x 4.5 x 0.7 mm **SOT1155-2**



Dimensions

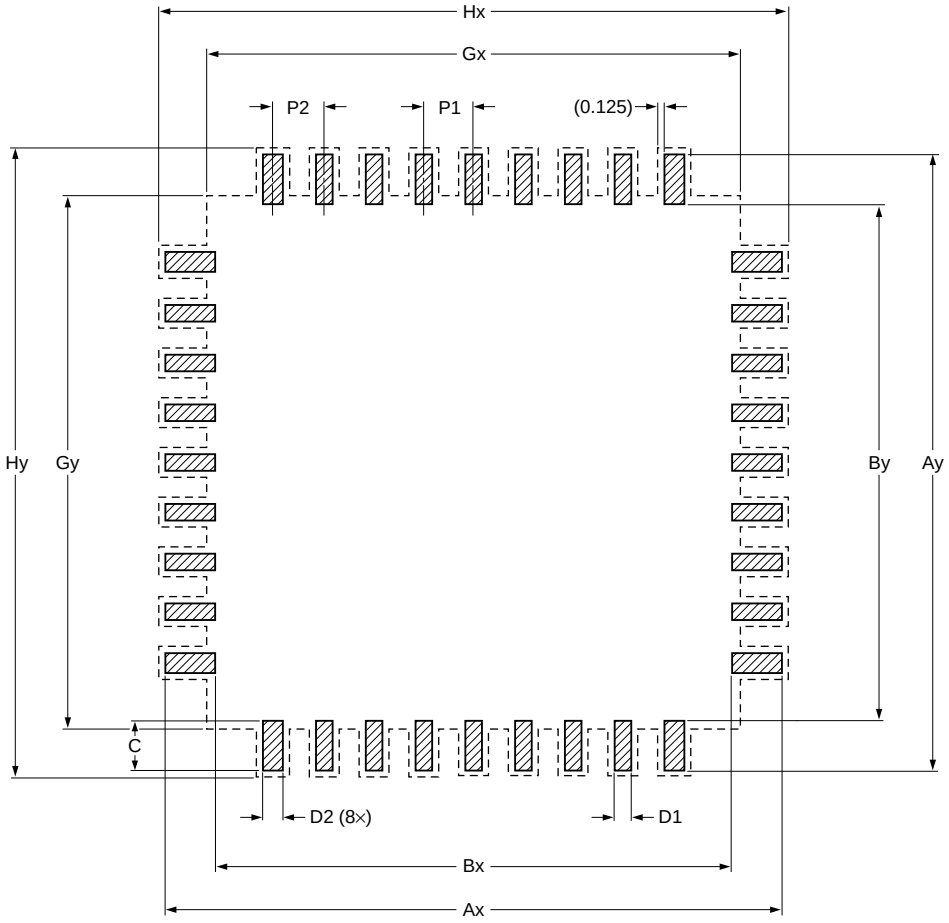
Unit	A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
max	1.10	0.30	0.80	0.35	4.6	4.6							
mm nom	0.95	0.25	0.70	0.30	4.5	4.5	0.5	3.5	3.5	0.15	0.05	0.08	0.1
min	0.85	0.20	0.65	0.25	4.4	4.4							

sot1155-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1155-2		- - -				~~13-06-17~~ 13-06-19

Fig 36. Package outline TFBGA48 (SOT1155-2)

Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2_fr

Fig 43. Reflow soldering for the LQFP64 package

16. Revision history

Table 21. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC11U3X v.2.3	20170208	Product data sheet	-	LPC11U3X v.2.2
Modifications:	• Updated Section 1 “General description”: Software libraries for multiple I/O Handler applications are available on nxp.com.			
LPC11U3X v.2.2	20140311	Product data sheet	-	LPC11U3X v.2.1
Modifications:	• Use of USB_CONNECT signal explained in Section 11.1 “Suggested USB interface solutions”. • Open-drain I^2C-bus and $\overline{\text{RESET}}$ pin descriptions clarified. See Table 3.			
LPC11U3X v.2.1	20131230	Product data sheet	-	LPC11U3X v.2
Modifications:		Add reserved function to pins PIO0_8/MISO0/CT16B0_MAT0/R/IOH_6 and PIO0_9/MOSI0/CT16B0_MAT1/R/IOH_7.		
LPC11U3X v.2	20131125	Product data sheet	-	LPC11U3X v.1.1
Modifications:		• Part LPC11U37HFBD64/401 with I/O handler added. • Additional I/O Handler pin functions added in Table 3. • Typical range of watchdog oscillator frequency changed to 9.4 kHz to 2.3 MHz.See Table 13. • Section 11.8 “I/O Handler software library applications” added. • Updated Section 11.1 “Suggested USB interface solutions” for clarity. • Condition V_{DD} = 0 V added to Parameter V_I in Table 5 for clarity.		
LPC11U3X v.1.1	20130924	Product data sheet	-	LPC11U3X v.1
Modifications:		• Removed the footnote “The peak current is limited to 25 times the corresponding maximum current.” in Table 4. • Table 3: Added “5 V tolerant pad” to $\overline{\text{RESET}}$/PIO0_0 table note. • Table 7: Removed BOD interrupt level 0. • Programmable glitch filter is enabled by default. See Section 7.7.1. • Added Section 11.6 “ADC effective input impedance”. • Table 5 “Static characteristics” added Pin capacitance section. • Updated Section 11.1 “Suggested USB interface solutions”. • Table 4 “Limiting values”: – Updated V_{DD} min and max. – Updated V_I conditions. • Table 10 “EEPROM characteristics”: – Removed f_{clk} and t_{er}; the user does not have control over these parameters. – Changed the t_{prog} from 1.1 ms to 2.9 ms; the EEPROM IAP always does an erase and program, thus the total program time is $t_{er} + t_{prog}$. • Changed title of Figure 29 from “USB interface on a self-powered device” to “USB interface with soft-connect”. • Section 10.7 “USB interface” added. Parameter t_{EOPR1} and t_{EOPR2} renamed to t_{EOPR}.		
LPC11U3X v.1	20120420	Product data sheet	-	-