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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, Microwire, SmartCard, SPI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11u35fbd48-401

- ◆ Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
 - ◆ Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.
 - ◆ Power profiles residing in boot ROM provide optimized performance and minimized power consumption for any given application through one simple function call.
 - ◆ Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
 - ◆ Processor wake-up from Deep-sleep and Power-down modes via reset, selectable GPIO pins, watchdog interrupt, or USB port activity.
 - ◆ Processor wake-up from Deep power-down mode using one special function pin.
 - ◆ Power-On Reset (POR).
 - ◆ Brownout detect with up to four separate thresholds for interrupt and forced reset.
- Unique device serial number for identification.
- Single 3.3 V power supply (1.8 V to 3.6 V).
- Temperature range -40°C to $+85^{\circ}\text{C}$.
- Available as LQFP64, LQFP48, TFBGA48, and HVQFN33 packages.

3. Applications

- Consumer peripherals
- Medical
- Industrial control
- Handheld scanners
- USB audio devices

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC11U34FHN33/311	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body $7 \times 7 \times 0.85$ mm	n/a
LPC11U34FBD48/311	LQFP48	plastic low profile quad flat package; 48 leads; body $7 \times 7 \times 1.4$ mm	SOT313-2
LPC11U34FHN33/421	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body $7 \times 7 \times 0.85$ mm	n/a
LPC11U34FBD48/421	LQFP48	plastic low profile quad flat package; 48 leads; body $7 \times 7 \times 1.4$ mm	SOT313-2
LPC11U35FHN33/401	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body $7 \times 7 \times 0.85$ mm	n/a
LPC11U35FBD48/401	LQFP48	plastic low profile quad flat package; 48 leads; body $7 \times 7 \times 1.4$ mm	SOT313-2
LPC11U35FBD64/401	LQFP64	plastic low profile quad flat package; 64 leads; body $10 \times 10 \times 1.4$ mm	SOT314-2
LPC11U35FHI33/501	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body $5 \times 5 \times 0.85$ mm	n/a
LPC11U35FET48/501	TFBGA48	plastic thin fine-pitch ball grid array package; 48 balls; body $4.5 \times 4.5 \times 0.7$ mm	SOT1155-2
LPC11U36FBD48/401	LQFP48	plastic low profile quad flat package; 48 leads; body $7 \times 7 \times 1.4$ mm	SOT313-2

Table 1. Ordering information ...continued

Type number	Package		
	Name	Description	Version
LPC11U36FBD64/401	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11U37FBD48/401	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U37HFBD64/401	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11U37FBD64/501	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

4.1 Ordering options

Table 2. Ordering options

Type number	Flash in kB	EEPROM in kB	SRAM0 in kB	USB SRAM in kB	SRAM1 in kB	Total SRAM in kB ^[1]	I/O Handler	USART	I ² C-bus FM+	SSP	USB device	ADC channels	GPIO pins
LPC11U34FHN33/311	40	4	8	-	-	8	no	1	1	2	1	8	26
LPC11U34FBD48/311	40	4	8	-	-	8	no	1	1	2	1	8	40
LPC11U34FHN33/421	48	4	8	2	-	10	no	1	1	2	1	8	26
LPC11U34FBD48/421	48	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U35FHN33/401	64	4	8	2	-	10	no	1	1	2	1	8	26
LPC11U35FBD48/401	64	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U35FBD64/401	64	4	8	2	-	10	no	1	1	2	1	8	54
LPC11U35FHI33/501	64	4	8	2	2 ^[1]	12	no	1	1	2	1	8	26
LPC11U35FET48/501	64	4	8	2	2 ^[1]	12	no	1	1	2	1	8	40
LPC11U36FBD48/401	96	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U36FBD64/401	96	4	8	2	-	10	no	1	1	2	1	8	54
LPC11U37FBD48/401	128	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U37HFBD64/401	128	4	8	2	2 ^[2]	10	yes	1	1	2	1	8	54
LPC11U37FBD64/501	128	4	8	2	2 ^[1]	12	no	1	1	2	1	8	54

[1] For general-purpose use.

[2] For I/O Handler use only.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
PIO0_17/RTS/ CT32B0_CAP0/SCLK	30	A3	45	60 [3]	I; PU	I/O	PIO0_17 — General purpose digital input/output pin.
					-	O	RTS — Request To Send output for USART.
					-	I	CT32B0_CAP0 — Capture input 0 for 32-bit timer 0.
					-	I/O	SCLK — Serial clock input/output for USART in synchronous mode.
PIO0_18/RXD/ CT32B0_MAT0	31	B3	46	61 [3]	I; PU	I/O	PIO0_18 — General purpose digital input/output pin.
					-	I	RXD — Receiver input for USART. Used in UART ISP mode.
					-	O	CT32B0_MAT0 — Match output 0 for 32-bit timer 0.
PIO0_19/TXD/ CT32B0_MAT1	32	B2	47	62 [3]	I; PU	I/O	PIO0_19 — General purpose digital input/output pin.
					-	O	TXD — Transmitter output for USART. Used in UART ISP mode.
					-	O	CT32B0_MAT1 — Match output 1 for 32-bit timer 0.
PIO0_20/CT16B1_CAP0	7	F2	9	11 [3]	I; PU	I/O	PIO0_20 — General purpose digital input/output pin.
					-	I	CT16B1_CAP0 — Capture input 0 for 16-bit timer 1.
PIO0_21/CT16B1_MAT0/ MOSI1	12	G4	17	22 [3]	I; PU	I/O	PIO0_21 — General purpose digital input/output pin.
					-	O	CT16B1_MAT0 — Match output 0 for 16-bit timer 1.
					-	I/O	MOSI1 — Master Out Slave In for SSP1.
PIO0_22/AD6/ CT16B1_MAT1/MISO1	20	E8	30	40 [6]	I; PU	I/O	PIO0_22 — General purpose digital input/output pin.
					-	I	AD6 — A/D converter, input 6.
					-	O	CT16B1_MAT1 — Match output 1 for 16-bit timer 1.
					-	I/O	MISO1 — Master In Slave Out for SSP1.
PIO0_23/AD7/IOH_9	27	A5	42	56 [6]	I; PU	I/O	PIO0_23 — General purpose digital input/output pin.
					-	I	AD7 — A/D converter, input 7.
					-	I/O	IOH_9 — I/O Handler input/output 9. (LPC11U37HFBD64/401 only.)
PIO1_0/CT32B1_MAT0/ IOH_10	-	-	-	1 [3]	I; PU	I/O	PIO1_0 — General purpose digital input/output pin.
					-	O	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
					-	I/O	IOH_10 — I/O Handler input/output 10. (LPC11U37HFBD64/401 only.)
PIO1_1/CT32B1_MAT1/ IOH_11	-	-	-	17 [3]	I; PU	I/O	PIO1_1 — General purpose digital input/output pin.
					-	O	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
					-	I/O	IOH_11 — I/O Handler input/output 11. (LPC11U37HFBD64/401 only.)
PIO1_2/CT32B1_MAT2/ IOH_12	-	-	-	34 [3]	I; PU	I/O	PIO1_2 — General purpose digital input/output pin.
					-	O	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
					-	I/O	IOH_12 — I/O Handler input/output 12. (LPC11U37HFBD64/401 only.)

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
PIO1_16/ $\overline{\text{RI}}$ / CT16B0_CAP0	-	A2	48	63 [3]	I; PU	I/O	PIO1_16 — General purpose digital input/output pin.
					-	I	$\overline{\text{RI}}$ — Ring Indicator input for USART.
					-	I	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.
PIO1_17/CT16B0_CAP1/ RXD	-	-	-	23 [3]	I; PU	I/O	PIO1_17 — General purpose digital input/output pin.
					-	I	CT16B0_CAP1 — Capture input 1 for 16-bit timer 0.
					-	I	RXD — Receiver input for USART.
PIO1_18/CT16B1_CAP1/ TXD	-	-	-	28 [3]	I; PU	I/O	PIO1_18 — General purpose digital input/output pin.
					-	I	CT16B1_CAP1 — Capture input 1 for 16-bit timer 1.
					-	O	TXD — Transmitter output for USART.
PIO1_19/ $\overline{\text{DTR}}$ /SSEL1	1	B1	2	3 [3]	I; PU	I/O	PIO1_19 — General purpose digital input/output pin.
					-	O	$\overline{\text{DTR}}$ — Data Terminal Ready output for USART.
					-	I/O	SSEL1 — Slave select for SSP1.
PIO1_20/ $\overline{\text{DSR}}$ /SCK1	-	H1	13	18 [3]	I; PU	I/O	PIO1_20 — General purpose digital input/output pin.
					-	I	$\overline{\text{DSR}}$ — Data Set Ready input for USART.
					-	I/O	SCK1 — Serial clock for SSP1.
PIO1_21/ $\overline{\text{DCD}}$ /MISO1	-	G8	26	35 [3]	I; PU	I/O	PIO1_21 — General purpose digital input/output pin.
					-	I	$\overline{\text{DCD}}$ — Data Carrier Detect input for USART.
					-	I/O	MISO1 — Master In Slave Out for SSP1.
PIO1_22/ $\overline{\text{RI}}$ /MOSI1	-	A7	38	51 [3]	I; PU	I/O	PIO1_22 — General purpose digital input/output pin.
					-	I	$\overline{\text{RI}}$ — Ring Indicator input for USART.
					-	I/O	MOSI1 — Master Out Slave In for SSP1.
PIO1_23/CT16B1_MAT1/ SSEL1	-	H4	18	24 [3]	I; PU	I/O	PIO1_23 — General purpose digital input/output pin.
					-	O	CT16B1_MAT1 — Match output 1 for 16-bit timer 1.
					-	I/O	SSEL1 — Slave select for SSP1.
PIO1_24/CT32B0_MAT0	-	G6	21	27 [3]	I; PU	I/O	PIO1_24 — General purpose digital input/output pin.
					-	O	CT32B0_MAT0 — Match output 0 for 32-bit timer 0.
PIO1_25/CT32B0_MAT1	-	A1	1	2 [3]	I; PU	I/O	PIO1_25 — General purpose digital input/output pin.
					-	O	CT32B0_MAT1 — Match output 1 for 32-bit timer 0.
PIO1_26/CT32B0_MAT2/ RXD/IOH_19	-	G2	11	14 [3]	I; PU	I/O	PIO1_26 — General purpose digital input/output pin.
					-	O	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.
					-	I	RXD — Receiver input for USART.
					-	I/O	IOH_19 — I/O Handler input/output 19. (LPC11U37HFBD64/401 only.)
PIO1_27/CT32B0_MAT3/ TXD/IOH_20	-	G1	12	15 [3]	I; PU	I/O	PIO1_27 — General purpose digital input/output pin.
					-	O	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
					-	O	TXD — Transmitter output for USART.
					-	I/O	IOH_20 — I/O Handler input/output 20. (LPC11U37HFBD64/401 only.)

7. Functional description

7.1 On-chip flash programming memory

The LPC11U3x contain up to 128 kB on-chip flash program memory. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip boot loader software.

The flash memory is divided into 4 kB sectors with each sector consisting of 16 pages. Individual pages can be erased using the IAP erase page command.

7.2 EEPROM

The LPC11U3x contain 4 kB of on-chip byte-erasable and byte-programmable EEPROM data memory. The EEPROM can be programmed using In-Application Programming (IAP) via the on-chip boot loader software.

7.3 SRAM

The LPC11U3x contain a total of 8 kB, 10 kB, or 12 kB on-chip static RAM memory.

On the LPC11U37HFB64/401, the 2 kB SRAM1 region at location 0x2000 0000 to 0x2000 07FFF is used for the I/O Handler software library. Do not use this memory location for data or other user code.

7.4 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.
- IAP support for EEPROM
- USB API
- Power profiles for configuring power consumption and PLL settings
- 32-bit integer division routines

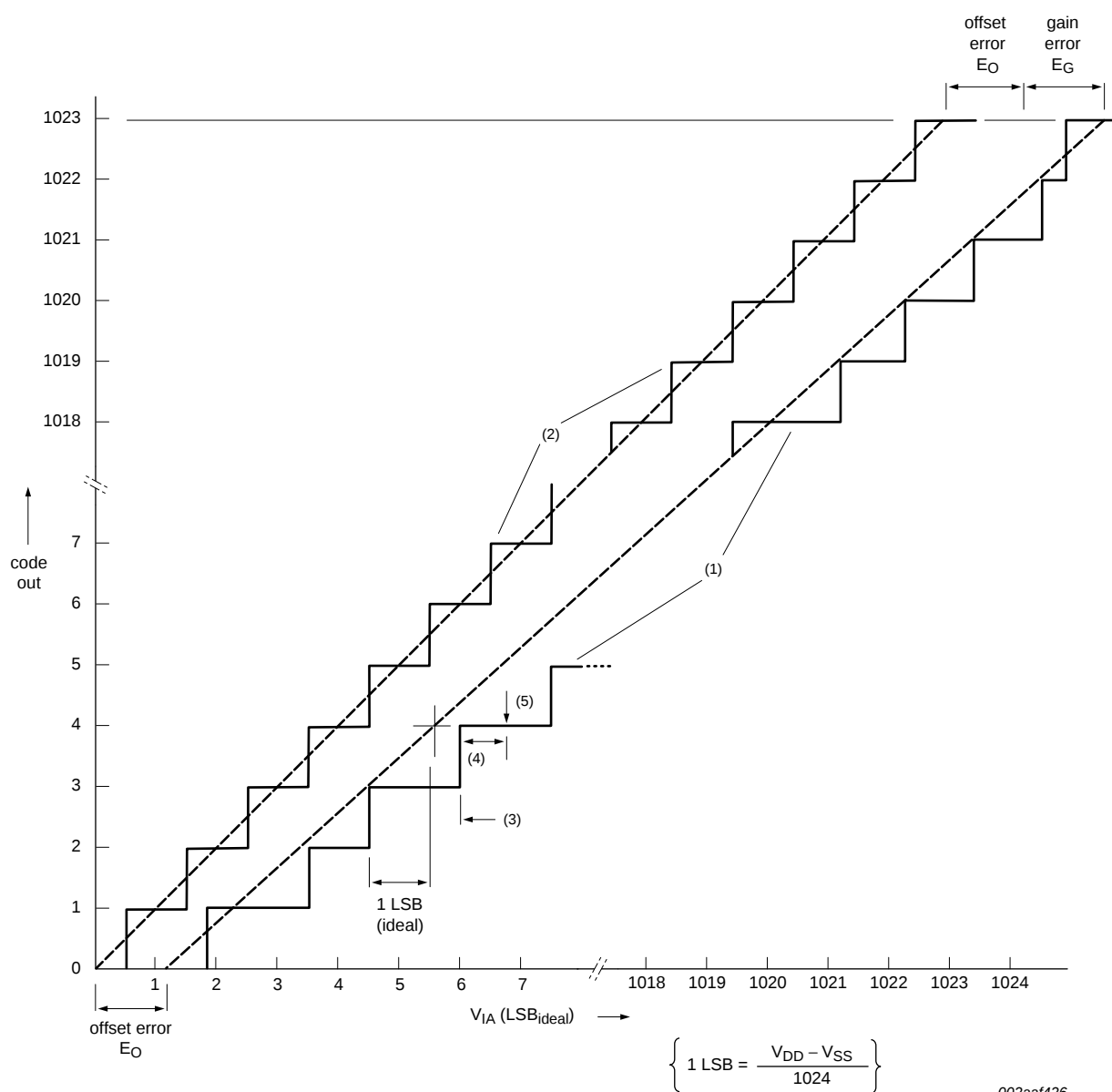
7.5 Memory map

The LPC11U3x incorporates several distinct memory regions, shown in the following figures. [Figure 6](#) shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB (Advanced High-performance Bus) peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB (Advanced Peripheral Bus) peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This addressing scheme allows simplifying the address decoding for each peripheral.

Table 5. Static characteristics ...continued
 $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.

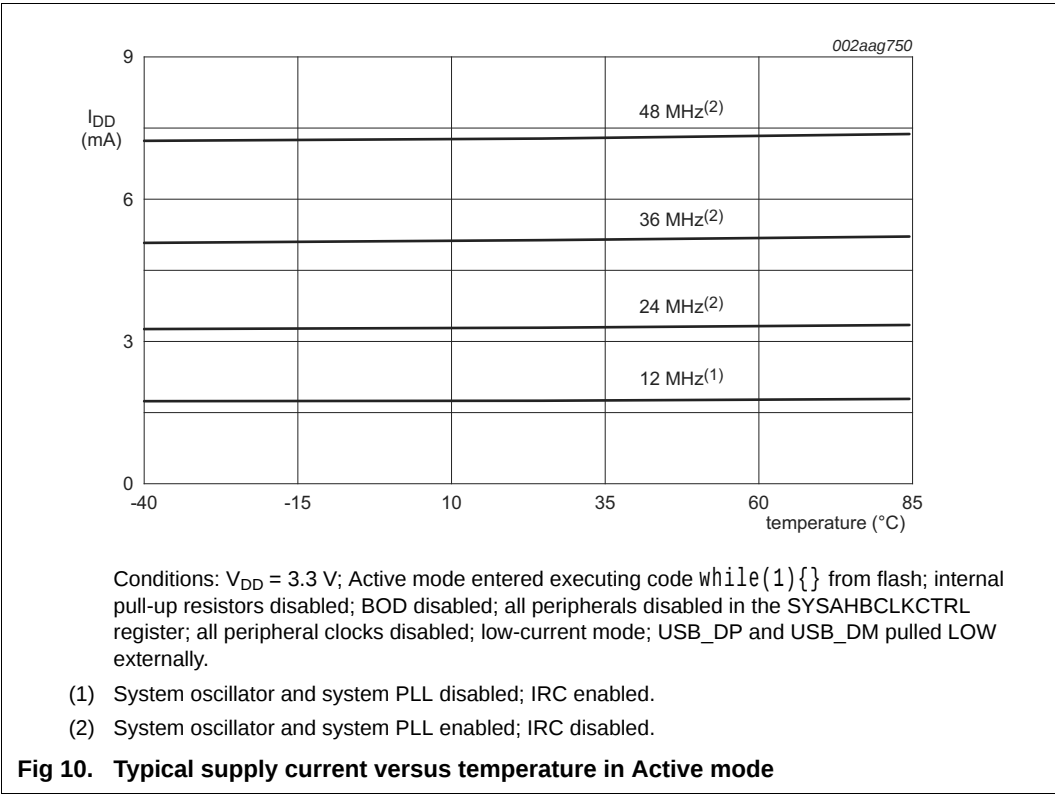
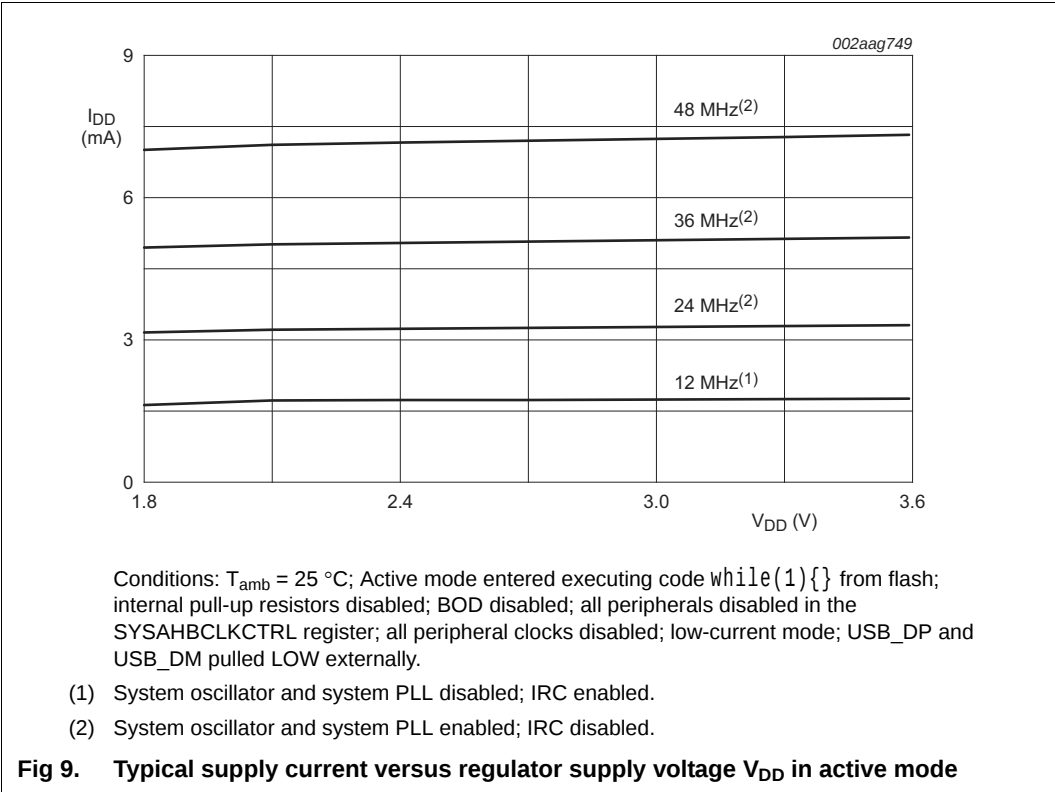
Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
I _{OL}	LOW-level output current	V _{OL} = 0.4 V 2.0 V ≤ V _{DD} ≤ 3.6 V	4	-	-	mA
		1.8 V ≤ V _{DD} < 2.0 V	3	-	-	mA
I _{OHS}	HIGH-level short-circuit output current	V _{OH} = 0 V ^[13]	-	-	−45	mA
I _{OLS}	LOW-level short-circuit output current	V _{OL} = V _{DD} ^[13]	-	-	50	mA
I _{pd}	pull-down current	V _I = 5 V	10	50	150	μA
I _{pu}	pull-up current	V _I = 0 V; 2.0 V ≤ V _{DD} ≤ 3.6 V	−15	−50	−85	μA
		1.8 V ≤ V _{DD} < 2.0 V	−10	−50	−85	μA
		V _{DD} < V _I < 5 V	0	0	0	μA
High-drive output pin (PIO0_7)						
I _{IL}	LOW-level input current	V _I = 0 V; on-chip pull-up resistor disabled	-	0.5	10	nA
I _{IH}	HIGH-level input current	V _I = V _{DD} ; on-chip pull-down resistor disabled	-	0.5	10	nA
I _{OZ}	OFF-state output current	V _O = 0 V; V _O = V _{DD} ; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V _I	input voltage	pin configured to provide a digital function; V _{DD} ≥ 1.8 V ^[11] ^[12]	0	-	5.0	V
		V _{DD} = 0 V	0	-	3.6	V
V _O	output voltage	output active	0	-	V _{DD}	V
V _{IH}	HIGH-level input voltage		0.7V _{DD}	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.3V _{DD}	V
V _{hys}	hysteresis voltage		0.4	-	-	V
V _{OH}	HIGH-level output voltage	2.5 V ≤ V _{DD} ≤ 3.6 V; I _{OH} = −20 mA	V _{DD} − 0.4	-	-	V
		1.8 V ≤ V _{DD} < 2.5 V; I _{OH} = −12 mA	V _{DD} − 0.4	-	-	V
V _{OL}	LOW-level output voltage	2.0 V ≤ V _{DD} ≤ 3.6 V; I _{OL} = 4 mA	-	-	0.4	V
		1.8 V ≤ V _{DD} < 2.0 V; I _{OL} = 3 mA	-	-	0.4	V
I _{OH}	HIGH-level output current	V _{OH} = V _{DD} − 0.4 V; 2.5 V ≤ V _{DD} ≤ 3.6 V	20	-	-	mA
		1.8 V ≤ V _{DD} < 2.5 V	12	-	-	mA
I _{OL}	LOW-level output current	V _{OL} = 0.4 V 2.0 V ≤ V _{DD} ≤ 3.6 V	4	-	-	mA
		1.8 V ≤ V _{DD} < 2.0 V	3	-	-	mA
I _{OLS}	LOW-level short-circuit output current	V _{OL} = V _{DD} ^[13]	-	-	50	mA
I _{pd}	pull-down current	V _I = 5 V	10	50	150	μA

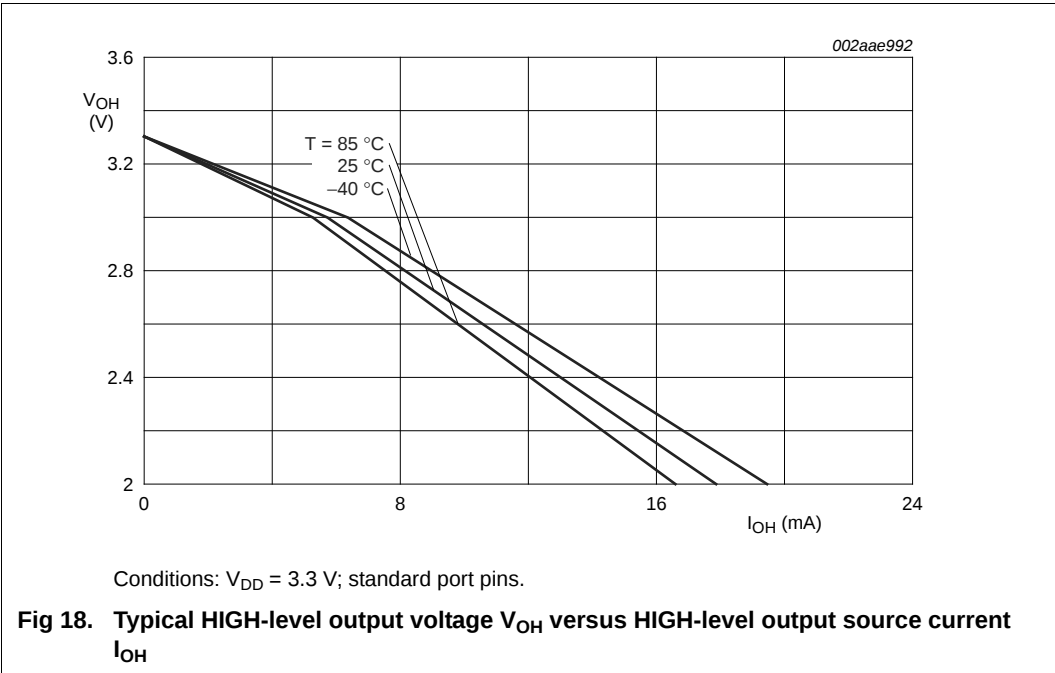
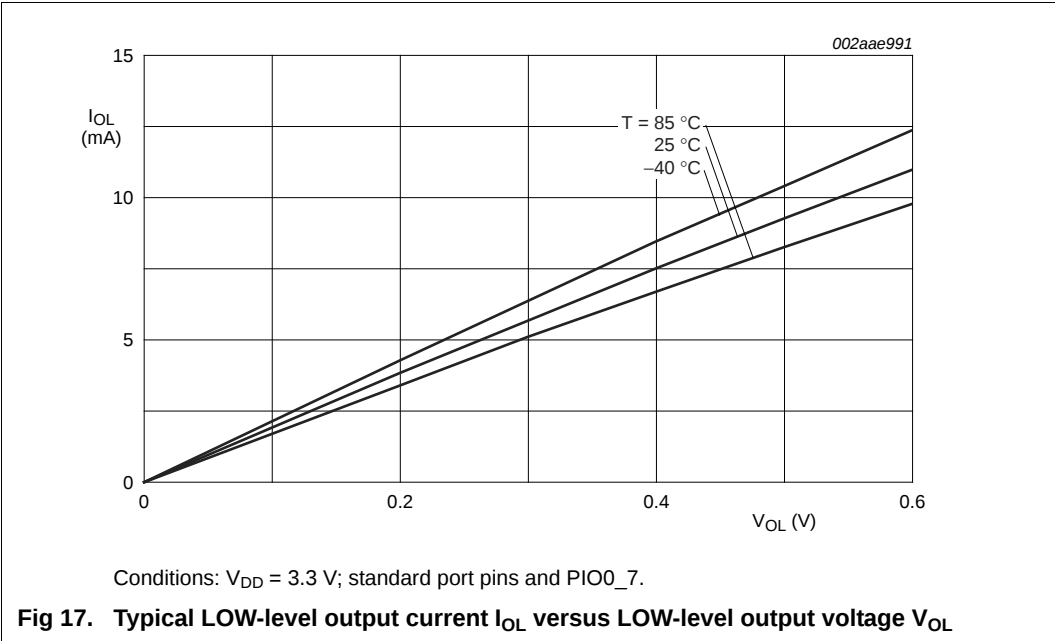


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- (1) Example of an actual transfer curve.
- (2) The ideal transfer curve.
- (3) Differential linearity error (E_D).
- (4) Integral non-linearity ($E_{L(adj)}$).
- (5) Center of a step of the actual transfer curve.

Fig 8. ADC characteristics





10. Dynamic characteristics

10.1 Flash memory

Table 9. Flash characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance	[1]	10000	100000	-	cycles
t_{ret}	retention time	powered	10	-	-	years
		unpowered	20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors	95	100	105	ms
t_{prog}	programming time	[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

Table 10. EEPROM characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{DD} = 2.7\text{ V}$ to 3.6 V . Based on JEDEC NVM qualification. Failure rate $< 10\text{ ppm}$ for parts as specified below.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance		100000	1000000	-	cycles
t_{ret}	retention time	powered	100	200	-	years
		unpowered	150	300	-	years
t_{prog}	programming time	64 bytes	-	2.9	-	ms

10.2 External clock

Table 11. Dynamic characteristic: external clock

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature ($25\text{ }^{\circ}\text{C}$), nominal supply voltages.

For a bus-powered device, the VBUS signal does not need to be connected to the USB_VBUS pin (see Figure 28). The USB_CONNECT function can additionally be connected as shown in Figure 27 to prevent the USB from timing out when there is a significant delay between power-up and handling USB traffic.

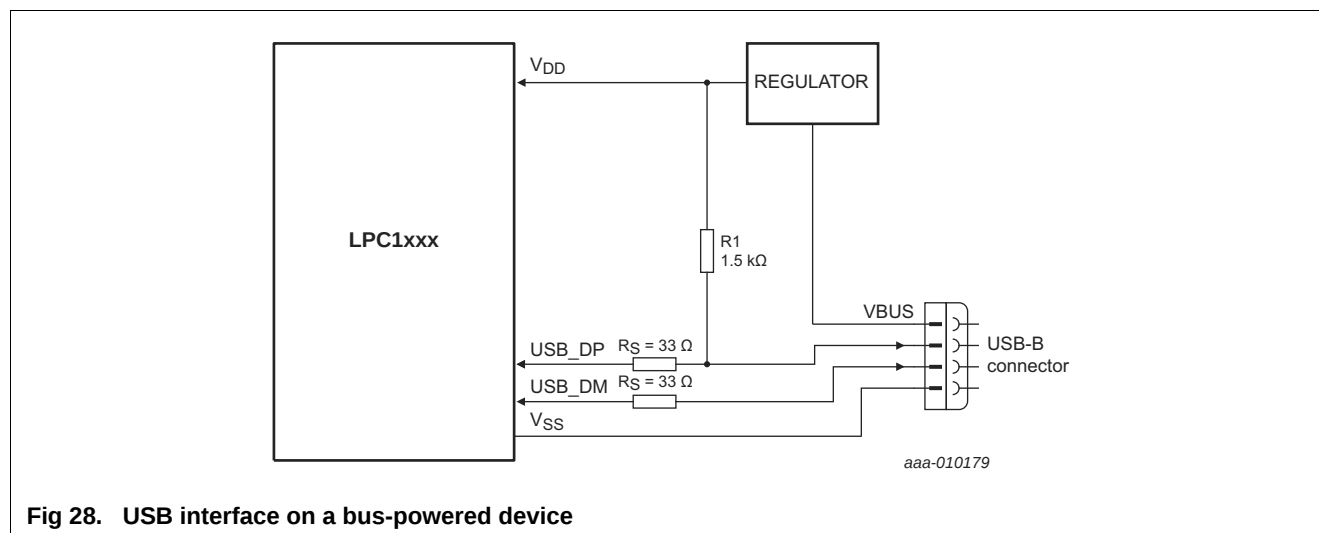


Fig 28. USB interface on a bus-powered device

Remark: When a bus-powered circuit as shown in Figure 28 is used, configure the `PIO0_3/USB_VBUS` pin for GPIO (`PIO0_3`) in the `IOCON` block to ensure that the `USB_CONNECT` signal can still be controlled by software. For details on the soft-connect feature, see the *LPC11U3x user manual* (Ref. 1).

Remark: When a self-powered circuit is used without connecting VBUS, configure the `PIO0_3/USB_VBUS` pin for GPIO (`PIO0_3`) and provide software that can detect the host presence through some other mechanism before enabling `USB_CONNECT` and the soft-connect feature. Enabling the soft-connect without host presence will lead to USB compliance failure.

11.4 Standard I/O pad configuration

Figure 31 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input

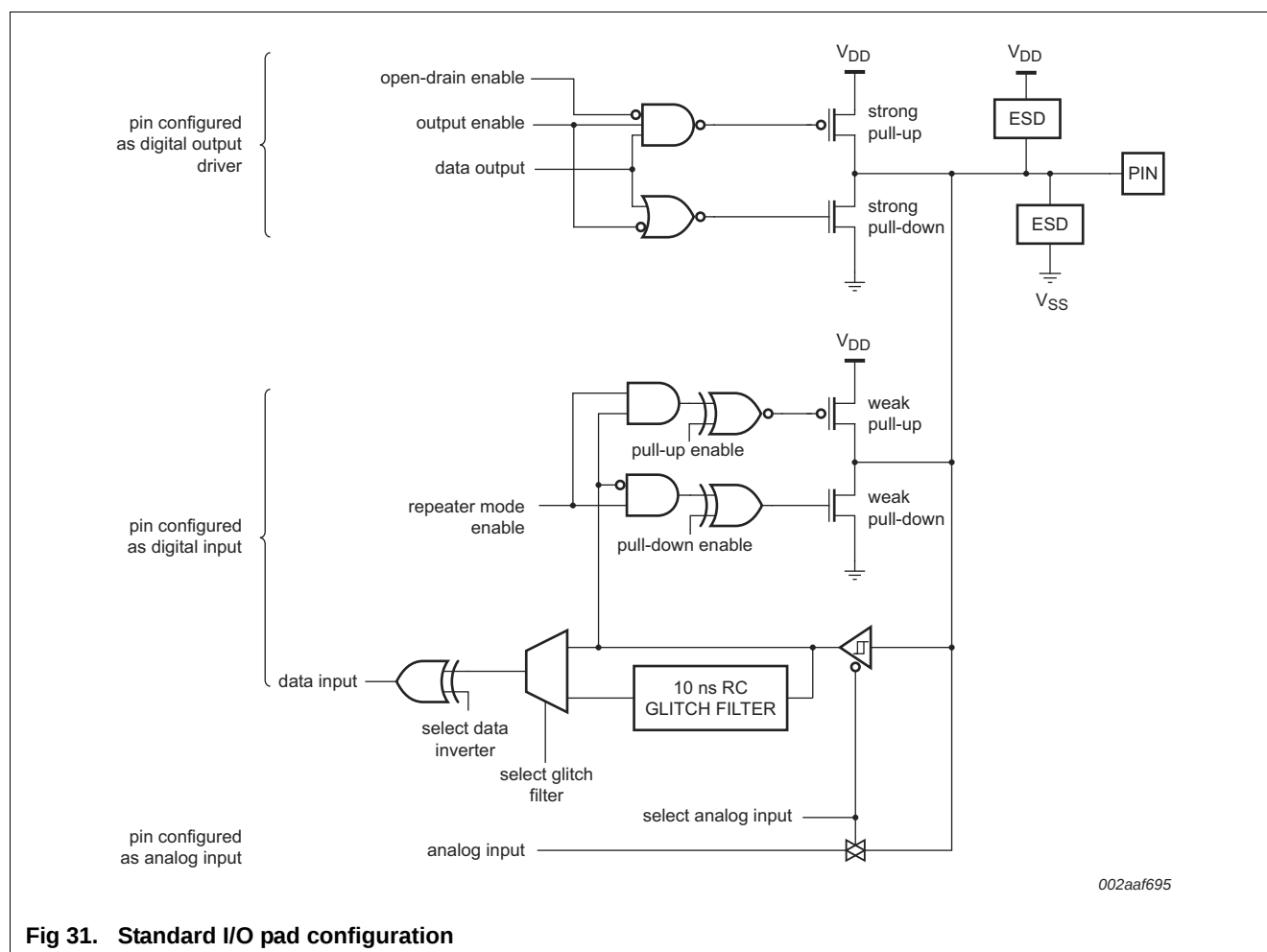


Fig 31. Standard I/O pad configuration

11.5 Reset pad configuration

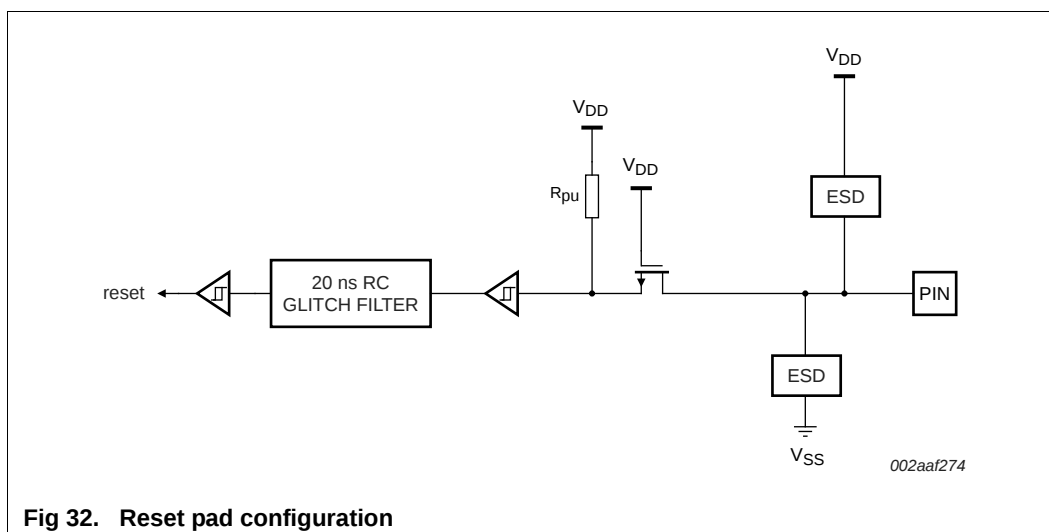


Fig 32. Reset pad configuration

11.6 ADC effective input impedance

A simplified diagram of the ADC input channels can be used to determine the effective input impedance seen from an external voltage source. See [Figure 33](#).

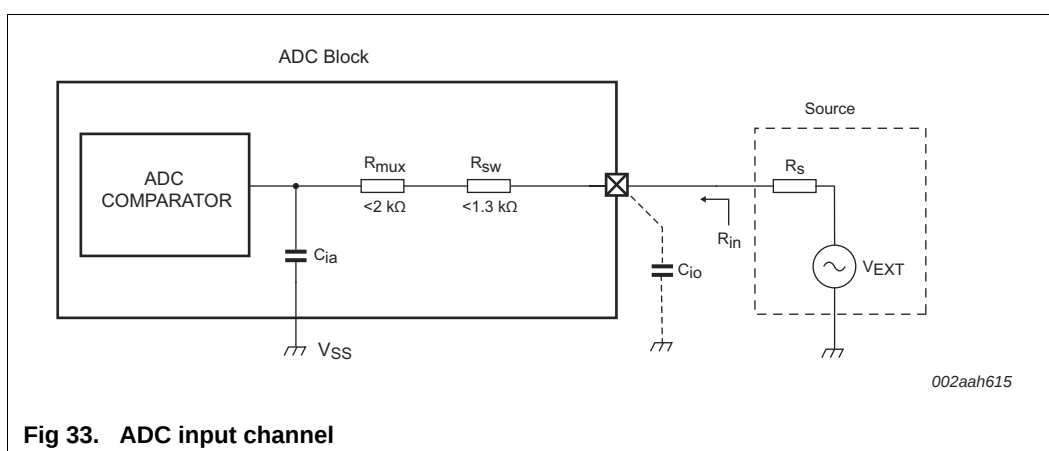


Fig 33. ADC input channel

The effective input impedance, R_{in} , seen by the external voltage source, V_{EXT} , is the parallel impedance of $((1/f_s \times C_{ia}) + R_{mux} + R_{sw})$ and $(1/f_s \times C_{io})$, and can be calculated using [Equation 1](#) with

f_s = sampling frequency

C_{ia} = ADC analog input capacitance

R_{mux} = analog mux resistance

R_{sw} = switch resistance

C_{io} = pin capacitance

$$R_{in} = \left(\frac{1}{f_s \times C_{ia}} + R_{mux} + R_{sw} \right) \parallel \left(\frac{1}{f_s \times C_{io}} \right) \quad (1)$$

Under nominal operating condition $V_{DD} = 3.3\text{ V}$ and with the maximum sampling frequency $f_s = 400\text{ kHz}$, the parameters assume the following values:

$$\begin{aligned}C_{ia} &= 1\text{ pF (max)} \\ R_{mux} &= 2\text{ k}\Omega\text{ (max)} \\ R_{sw} &= 1.3\text{ k}\Omega\text{ (max)} \\ C_{io} &= 7.1\text{ pF (max)}\end{aligned}$$

The effective input impedance with these parameters is $R_{in} = 308\text{ k}\Omega$.

11.7 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in [Table 6](#):

- The ADC input trace must be short and as close as possible to the LPC11U3x chip.
- Shield The ADC input traces from fast switching digital signals and noisy power supply lines.
- The ADC and the digital core share the same power supply. Therefore, filter the power supply line adequately.
- To improve the ADC performance in a noisy environment, put the device in Sleep mode during the ADC conversion.

11.8 I/O Handler software library applications

The following sections provide application examples for the I/O Handler software library. All library examples make use of the I/O Handler hardware to extend the functionality of the part through software library calls. The libraries are available on <http://www.LPCware.com>.

11.8.1 I/O Handler I²S

The I/O Handler software library provides functions to emulate an I²S master transmit interface using the I/O Handler hardware block.

The emulated I²S interface loops over a 1 kB buffer, transmitting the datawords according to the I²S protocol. Interrupts are generated every time when the first 512 bytes have been transmitted and when the last 512 bytes have been transmitted. This allows the ARM core to load the free portion of the buffer with new data, thereby enabling streaming audio.

Two channels with 16-bit per channel are supported. The code size of the software library is 1 kB and code must be executed from the SRAM1 memory area reserved for the I/O Handler code.

11.8.2 I/O Handler UART

The I/O Handler UART library emulates one additional full-duplex UART. The emulated UART can be configured for 7 or 8 data bits, no parity, and 1 or 2 stop bits. The baud rate is configurable up to 115200 baud. The RXD signal is available on three I/O Handler pins (IOH_6, IOH_16, IOH_20), while TXD and CTS are available on all 21 I/O Handler pins.

The code size of the software library is about 1.2 kB and code must be executed from the SRAM1 memory area reserved for the I/O Handler code.

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads;
33 terminals; body 7 x 7 x 0.85 mm

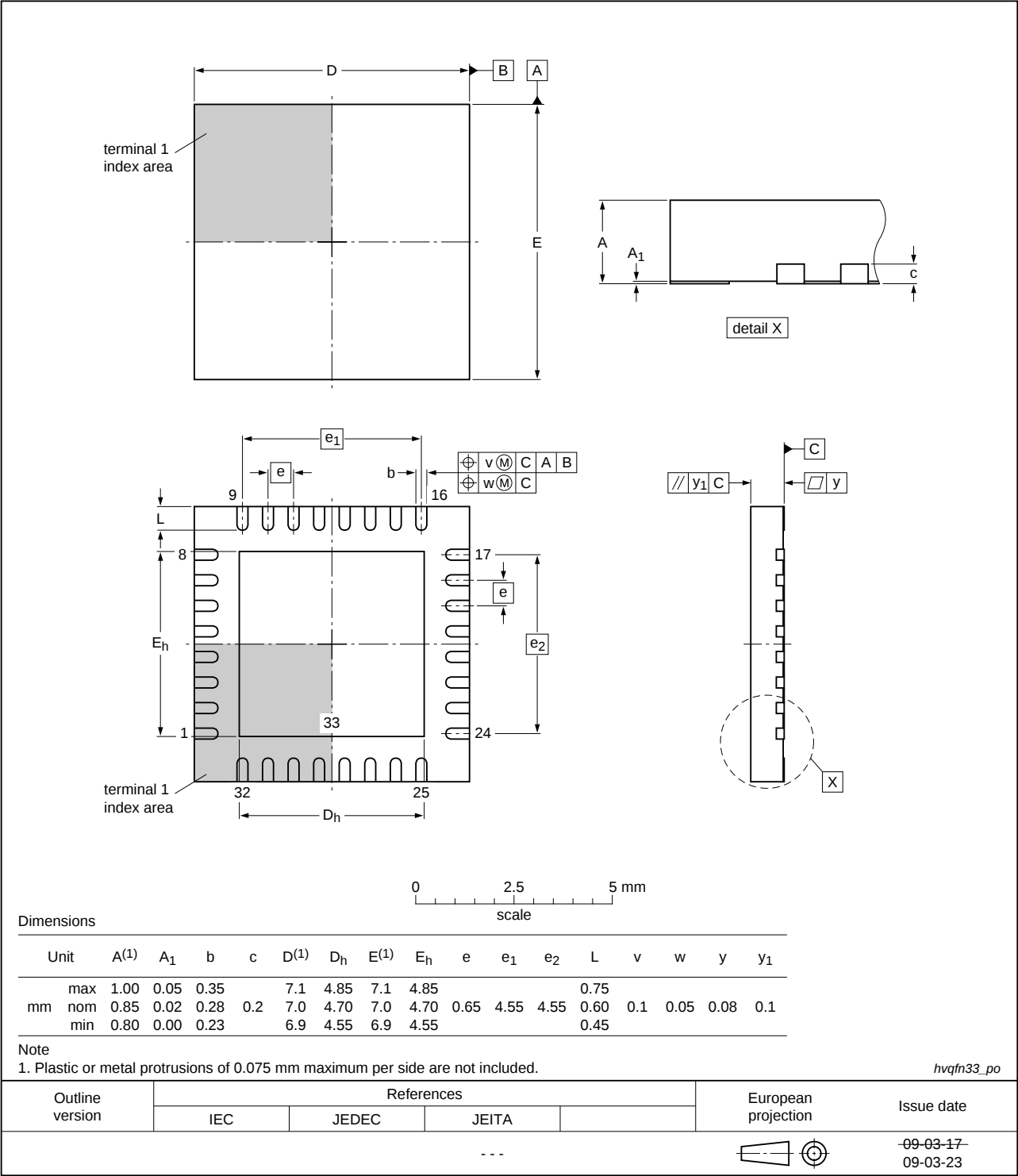


Fig 35. Package outline HVQFN33 (7 x 7 x 0.85 mm)

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm

SOT313-2

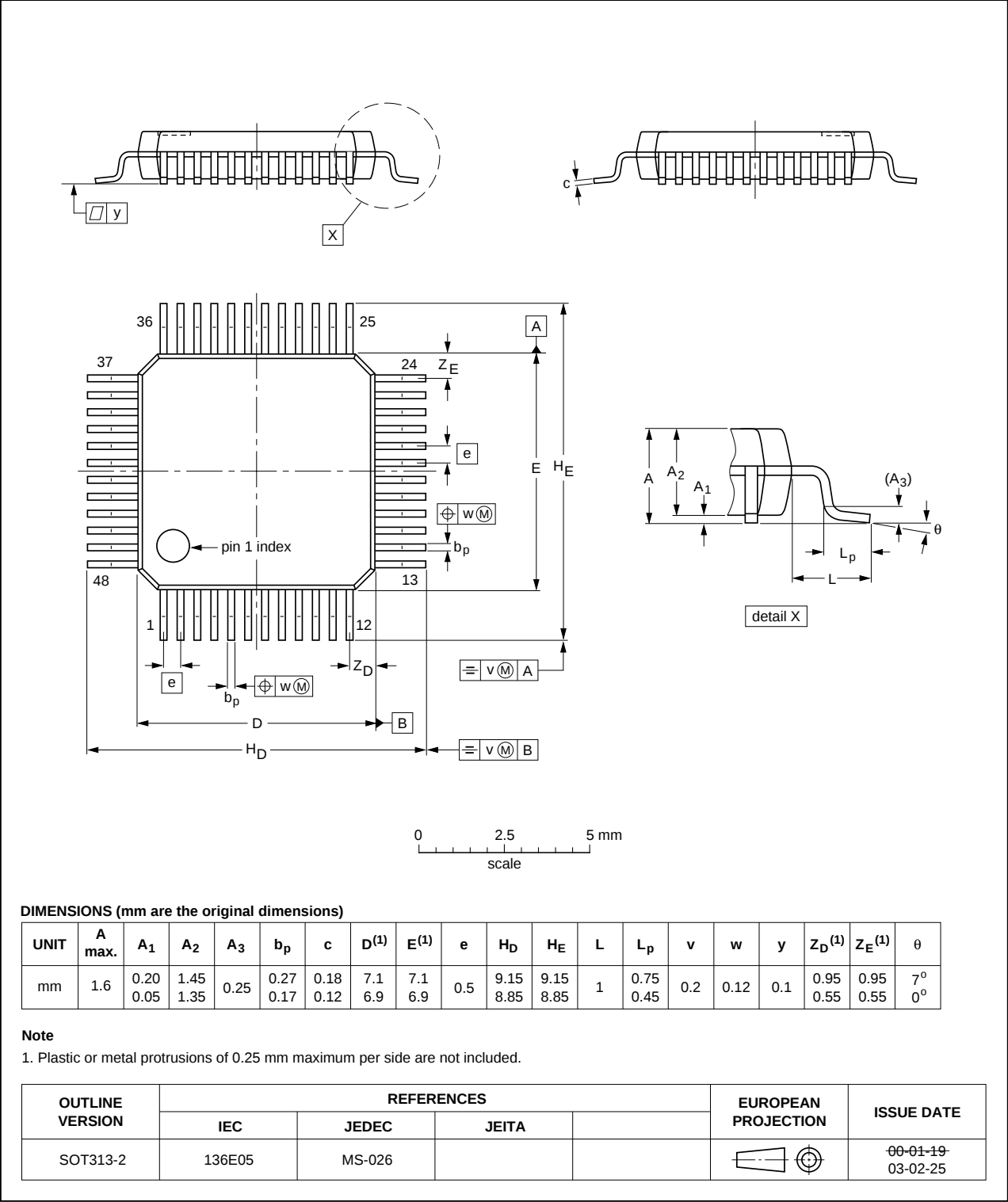
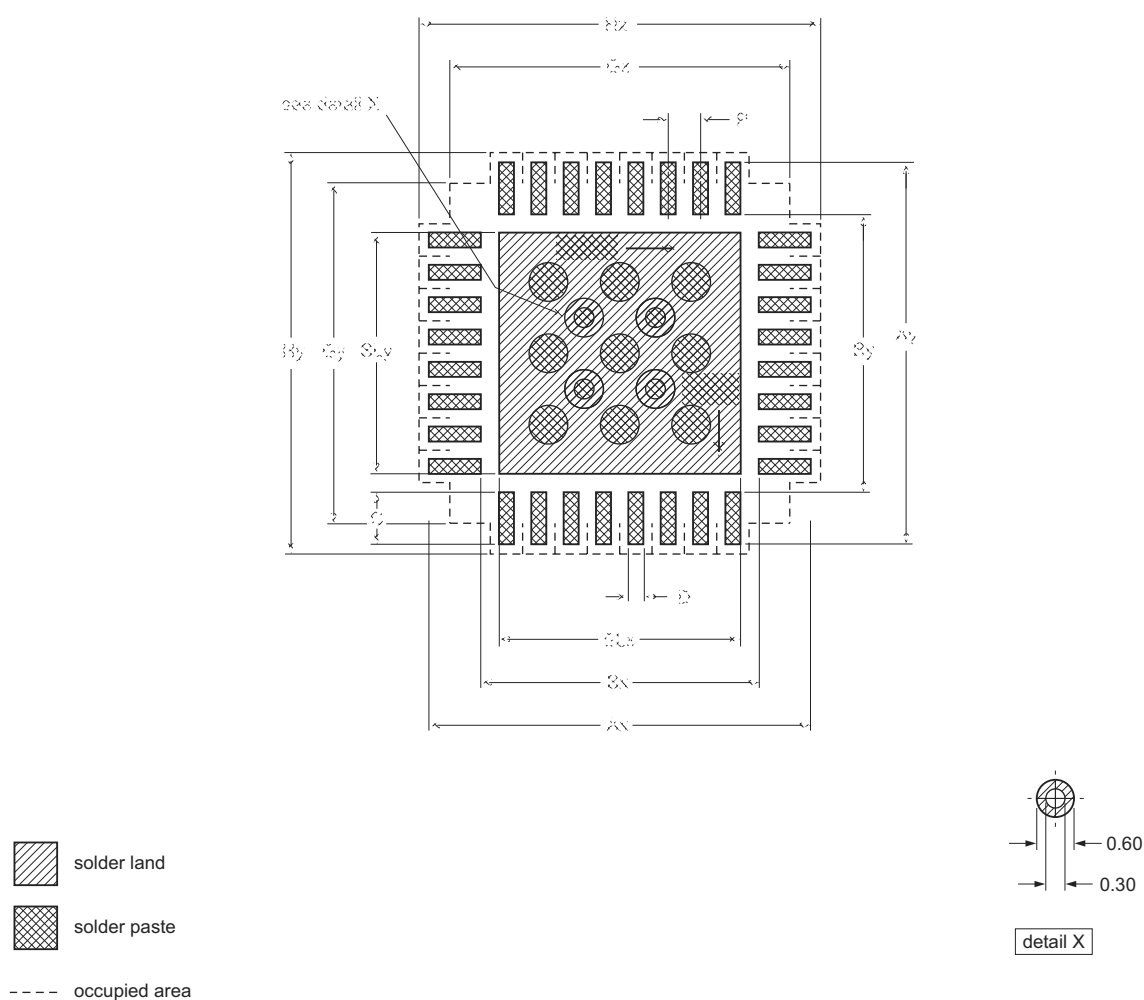


Fig 37. Package outline LQFP48 (SOT313-2)

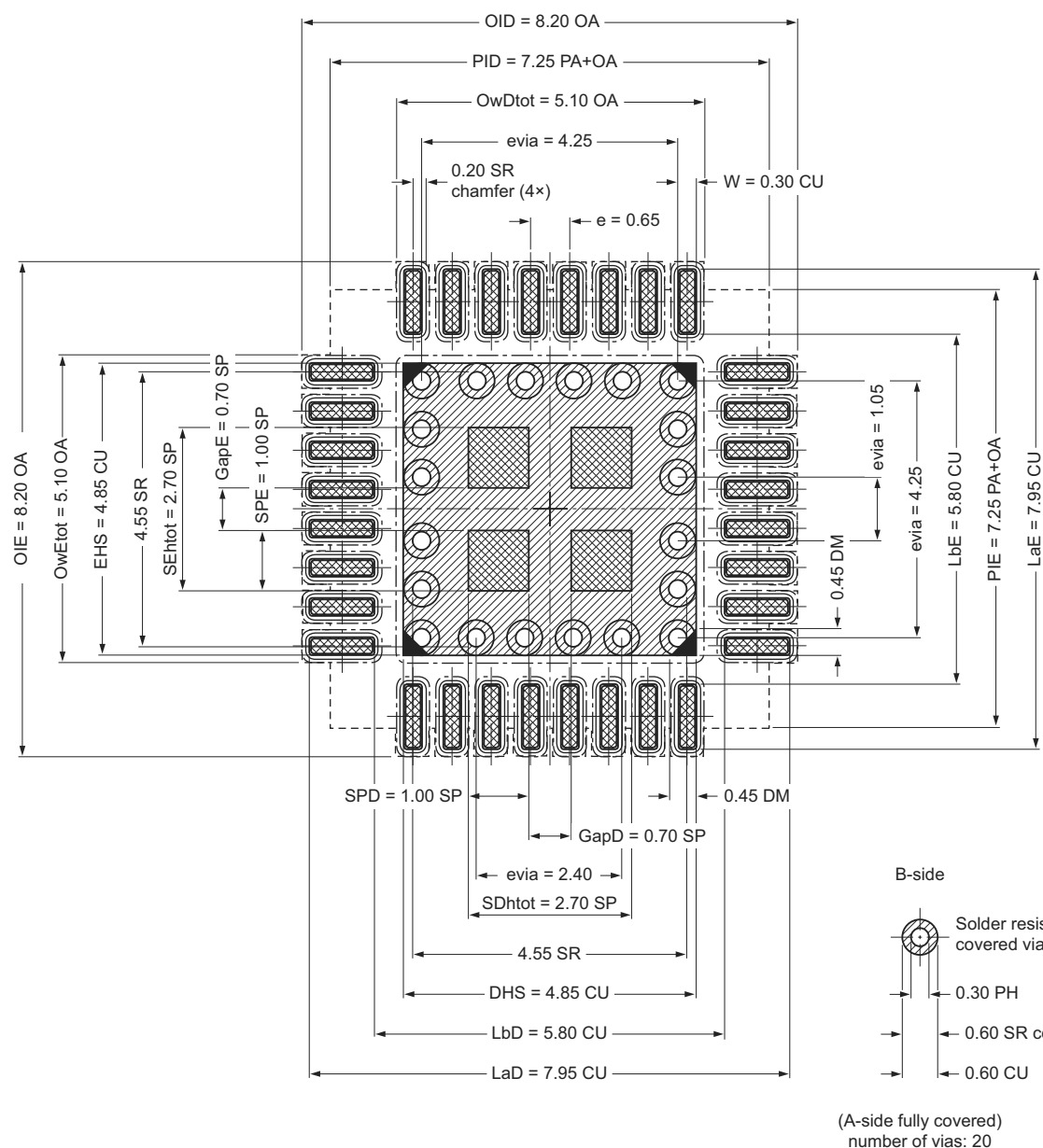
13. Soldering

Footprint information for reflow soldering of HVQFN33 package



Dimensions in mm														
P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	nSPx	nSPy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	5.25	5.25	6.2	6.2	3.75	3.75	3	3
Issue date	11-11-15 11-11-20													

Fig 39. Reflow soldering for the HVQFN33 (5x5) package



	solder land		solder land plus solder paste
	solder paste deposit		solder resist
----	occupied area		Dimensions in mm

Remark:
Stencil thickness: 0.125 mm

001aao134

Fig 40. Reflow soldering for the HVQFN33 (7x7) package

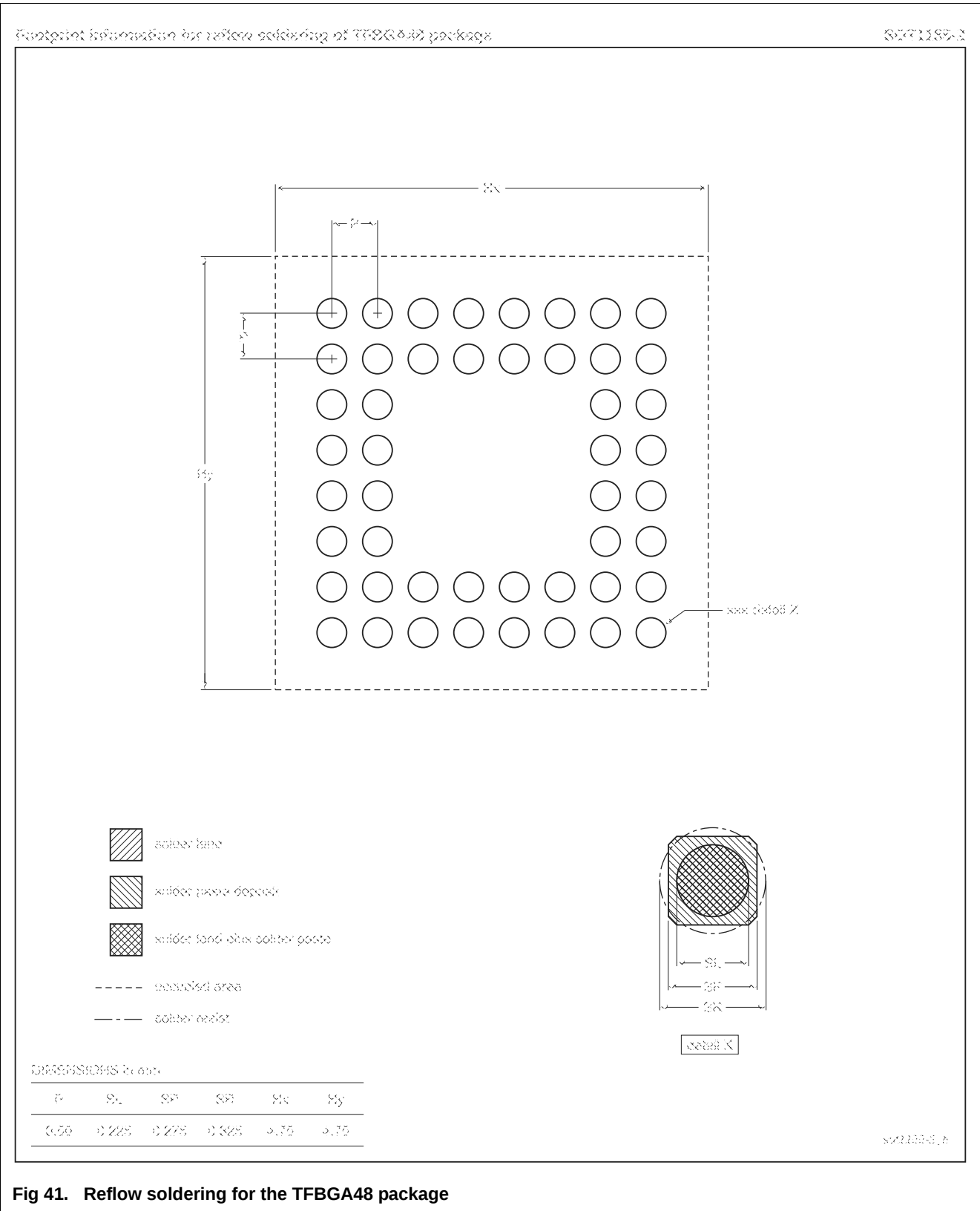


Fig 41. Reflow soldering for the TFBGA48 package

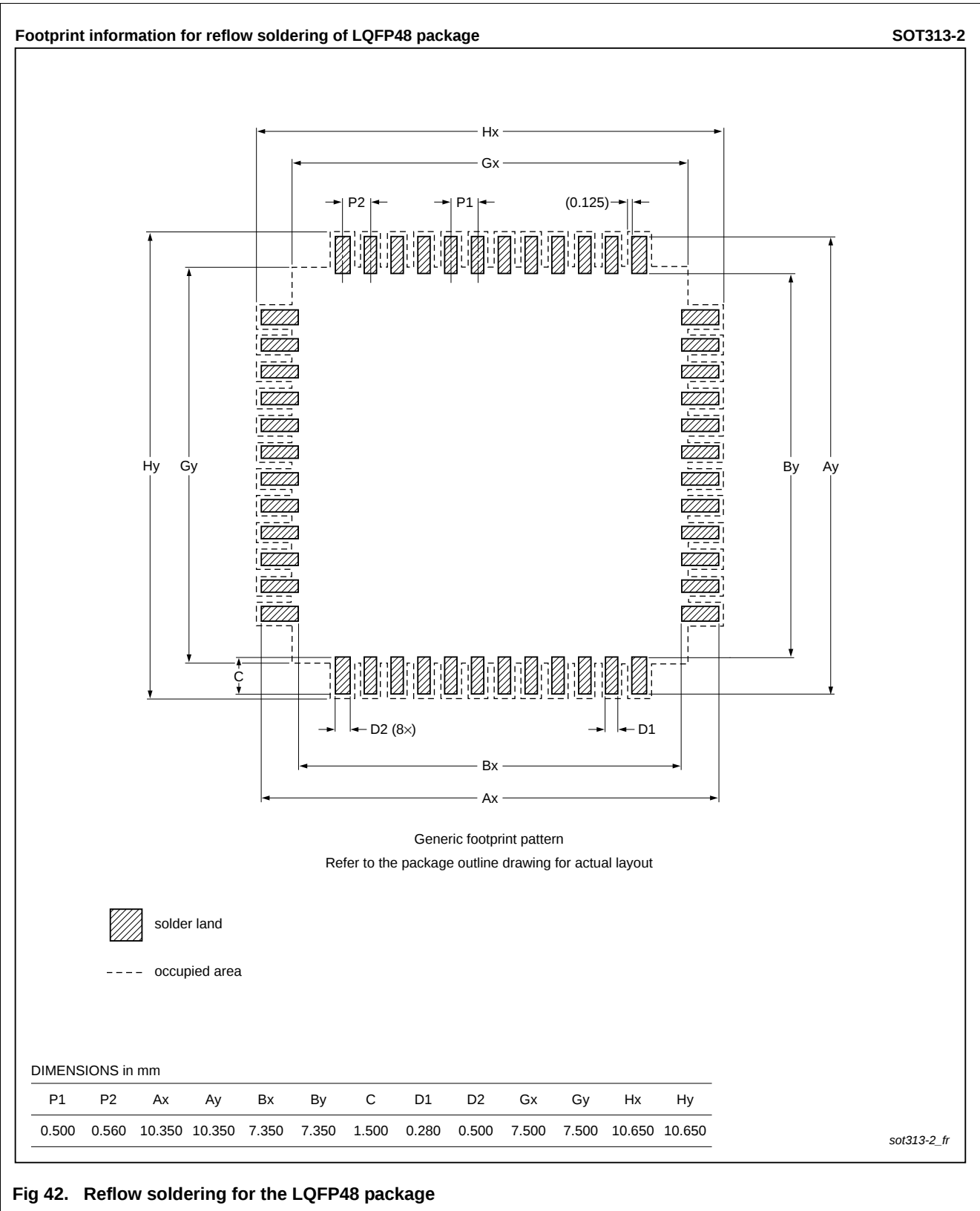


Fig 42. Reflow soldering for the LQFP48 package