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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit
Speed	50MHz
Connectivity	I²C, Microwire, SmartCard, SPI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b SAR
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TFBGA
Supplier Device Package	48-TFBGA (4.5x4.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11u35fet48-501

- 4 kB on-chip EEPROM data memory; byte erasable and byte programmable; on-chip API support.
- Up to 12 kB SRAM data memory.
- 16 kB boot ROM.
- In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
- ROM-based USB drivers. Flash updates via USB supported.
- ROM-based 32-bit integer division routines.

- Debug options:
  - Standard JTAG (Joint Test Action Group) test interface for BSDL (Boundary Scan Description Language).
  - Serial Wire Debug.
- Digital peripherals:
  - Up to 54 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, repeater mode, and open-drain mode.
  - Up to 8 GPIO pins can be selected as edge and level sensitive interrupt sources.
  - Two GPIO grouped interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
  - High-current source output driver (20 mA) on one pin.
  - High-current sink driver (20 mA) on true open-drain pins.
  - Four general purpose counter/timers with a total of up to 8 capture inputs and 13 match outputs.
  - Programmable Windowed WatchDog Timer (WWDT) with a dedicated, internal low-power WatchDog Oscillator (WDO).
- Analog peripherals:
  - 10-bit ADC with input multiplexing among eight pins.
- Serial interfaces:
  - USB 2.0 full-speed device controller.
  - USART with fractional baud rate generation, internal FIFO, a full modem control handshake interface, and support for RS-485/9-bit mode and synchronous mode. USART supports an asynchronous smart card interface (ISO 7816-3).
  - Two SSP controllers with FIFO and multi-protocol capabilities.
  - I^2C-bus interface supporting the full I^2C-bus specification and Fast-mode Plus with a data rate of up to 1 Mbit/s with multiple address recognition and monitor mode.
- I/O Handler for hardware emulation of serial interfaces and DMA; supported through software libraries. (LPC11U37HFBD64/401 only.)
- Clock generation:
  - Crystal Oscillator with an operating range of 1 MHz to 25 MHz (system oscillator).
  - 12 MHz high-frequency Internal RC oscillator (IRC) that can optionally be used as a system clock.
  - Internal low-power, low-frequency WatchDog Oscillator (WDO) with programmable frequency output.
  - PLL allows CPU operation up to the maximum CPU rate with the system oscillator or the IRC as clock sources.
  - A second, dedicated PLL is provided for USB.

6.2 Pin description

Table 3 shows all pins and their assigned digital or analog functions in order of the GPIO port number. The default function after reset is listed first. All port pins have internal pull-up resistors enabled after reset except for the true open-drain pins PIO0_4 and PIO0_5.

Every port pin has a corresponding IOCON register for programming the digital or analog function, the pull-up/pull-down configuration, the repeater, and the open-drain modes.

The USART, counter/timer, and SSP functions are available on more than one port pin.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
RESET/PIO0_0	2	C1	3	4 [2]	I; PU	I	**RESET —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode. In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed and Deep power-down mode is not used.
					-	I/O	**PIO0_0 —** General purpose digital input/output pin.
PIO0_1/CLKOUT/ CT32B0_MAT2/ USB_FTOGGLE	3	C2	4	5 [3]	I; PU	I/O	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler or the USB device enumeration.
					-	O	**CLKOUT —** Clockout pin.
					-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					-	O	**USB_FTOGGLE —** USB 1 ms Start-of-Frame signal.
PIO0_2/SSEL0/ CT16B0_CAP0/IOH_0	8	F1	10	13 [3]	I; PU	I/O	**PIO0_2 —** General purpose digital input/output pin.
					-	I/O	**SSEL0 —** Slave select for SSP0.
					-	I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
					-	I/O	**IOH_0 —** I/O Handler input/output 0. LPC11U37HFBD64/401 only.
PIO0_3/USB_VBUS/ IOH_1	9	H2	14	19 [3]	I; PU	I/O	**PIO0_3 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler. A HIGH level during reset starts the USB device enumeration.
					-	I	**USB_VBUS —** Monitors the presence of USB bus power.
					-	I/O	**IOH_1 —** I/O Handler input/output 1. LPC11U37HFBD64/401 only.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
PIO0_4/SCL/IOH_2	10	G3	15	20 [4]	I; IA	I/O	**PIO0_4 —** General purpose digital input/output pin (open-drain).
					-	I/O	**SCL —** I^2C-bus clock input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
					-	I/O	**IOH_2 —** I/O Handler input/output 2. LPC11U37HFBD64/401 only.
PIO0_5/SDA/IOH_3	11	H3	16	21 [4]	I; IA	I/O	**PIO0_5 —** General purpose digital input/output pin (open-drain).
					-	I/O	**SDA —** I^2C-bus data input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
					-	I/O	**IOH_3 —** I/O Handler input/output 3. LPC11U37HFBD64/401 only.
PIO0_6/$\overline{\text{USB\_CONNECT}}$/SCK0/IOH_4	15	H6	22	29 [3]	I; PU	I/O	**PIO0_6 —** General purpose digital input/output pin.
					-	O	**$\overline{\text{USB\_CONNECT}}$ —** Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
					-	I/O	**SCK0 —** Serial clock for SSP0.
					-	I/O	**IOH_4 —** I/O Handler input/output 4. LPC11U37HFBD64/401 only.
PIO0_7/$\overline{\text{CTS}}$/IOH_5	16	G7	23	30 [5]	I; PU	I/O	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
					-	I	**$\overline{\text{CTS}}$ —** Clear To Send input for USART.
					-	I/O	**IOH_5 —** I/O Handler input/output 5. (LPC11U37HFBD64/401 only.)
PIO0_8/MISO0/CT16B0_MAT0/R/IOH_6	17	F8	27	36 [3]	I; PU	I/O	**PIO0_8 —** General purpose digital input/output pin.
					-	I/O	**MISO0 —** Master In Slave Out for SSP0.
					-	O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
					-	-	Reserved.
					-	I/O	**IOH_6 —** I/O Handler input/output 6. (LPC11U37HFBD64/401 only.)
PIO0_9/MOSI0/CT16B0_MAT1/R/IOH_7	18	F7	28	37 [3]	I; PU	I/O	**PIO0_9 —** General purpose digital input/output pin.
					-	I/O	**MOSI0 —** Master Out Slave In for SSP0.
					-	O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					-	-	Reserved.
					-	I/O	**IOH_7 —** I/O Handler input/output 7. (LPC11U37HFBD64/401 only.)

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
SWCLK/PIO0_10/SCK0/ CT16B0_MAT2	19	E7	29	38 [3]	I; PU	I	**SWCLK —** Serial wire clock and test clock TCK for JTAG interface.
					-	I/O	**PIO0_10 —** General purpose digital input/output pin.
					-	O	**SCK0 —** Serial clock for SSP0.
					-	O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
TDI/PIO0_11/AD0/ CT32B0_MAT3	21	D8	32	42 [6]	I; PU	I	**TDI —** Test Data In for JTAG interface.
					-	I/O	**PIO0_11 —** General purpose digital input/output pin.
					-	I	**AD0 —** A/D converter, input 0.
					-	O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
TMS/PIO0_12/AD1/ CT32B1_CAP0	22	C7	33	44 [6]	I; PU	I	**TMS —** Test Mode Select for JTAG interface.
					-	I/O	**PIO_12 —** General purpose digital input/output pin.
					-	I	**AD1 —** A/D converter, input 1.
					-	I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
TDO/PIO0_13/AD2/ CT32B1_MAT0	23	C8	34	45 [6]	I; PU	O	**TDO —** Test Data Out for JTAG interface.
					-	I/O	**PIO0_13 —** General purpose digital input/output pin.
					-	I	**AD2 —** A/D converter, input 2.
					-	O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
$\overline{\text{TRST}}$/PIO0_14/AD3/ CT32B1_MAT1	24	B7	35	46 [6]	I; PU	I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
					-	I/O	**PIO0_14 —** General purpose digital input/output pin.
					-	I	**AD3 —** A/D converter, input 3.
					-	O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO0_15/AD4/ CT32B1_MAT2	25	B6	39	52 [6]	I; PU	I/O	**SWDIO —** Serial wire debug input/output.
					-	I/O	**PIO0_15 —** General purpose digital input/output pin.
					-	I	**AD4 —** A/D converter, input 4.
					-	O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO0_16/AD5/ CT32B1_MAT3/IOH_8/ WAKEUP	26	A6	40	53 [6]	I; PU	I/O	**PIO0_16 —** General purpose digital input/output pin.
					-	I	**AD5 —** A/D converter, input 5.
					-	O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
					-	I/O	**IOH_8 —** I/O Handler input/output 8. (LPC11U37HFBD64/401 only.)
					-	I	**WAKEUP —** Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode, then pull LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
PIO1_28/CT32B0_CAP0/ SCLK	-	H7	24	31 [3]	I; PU	I/O	**PIO1_28 —** General purpose digital input/output pin.
					-	I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
					-	I/O	**SCLK —** Serial clock input/output for USART in synchronous mode.
PIO1_29/SCK0/ CT32B0_CAP1	-	D7	31	41 [3]	I; PU	I/O	**PIO1_29 —** General purpose digital input/output pin.
					-	I/O	**SCK0 —** Serial clock for SSP0.
					-	I	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0.
PIO1_31	-	-	25	- [3]	I; PU	I/O	**PIO1_31 —** General purpose digital input/output pin.
USB_DM	13	G5	19	25 [7]	F	-	**USB_DM —** USB bidirectional D− line.
USB_DP	14	H5	20	26 [7]	F	-	**USB_DP —** USB bidirectional D+ line.
XTALIN	4	D1	6	8 [8]	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	5	E1	7	9 [8]	-	-	Output from the oscillator amplifier.
V_{DD}	6; 29	B4; E2	8; 44	10; 33; 48; 58	-	-	Supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
V_{SS}	33	B5; D2	5; 41	7; 54	-	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; If the pins are not used, tie floating pins to ground or power to minimize power consumption.

[2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See Figure 32 for the reset pad configuration.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 31).

[4] I^2C-bus pin compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 31); includes high-current output driver.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 31); includes digital input glitch filter.

[7] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[8] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). Leave XTALOUT floating.

7.18.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL. On the LPC11U3x, use the system oscillator to provide the clock source to USB.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

7.18.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over processing and temperature is ±40 % (see also Table 13).

7.18.2 System PLL and USB PLL

The LPC11U3x contain a system PLL and a dedicated PLL for generating the 48 MHz USB clock. The system and USB PLLs are identical.

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. To support this frequency range, an additional divider keeps the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. Software can enable the PLL later. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.18.3 Clock output

The LPC11U3x feature a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.18.4 Wake-up process

The LPC11U3x begin operation by using the 12 MHz IRC oscillator as the clock source at power-up and when awakened from Deep power-down mode . This mechanism allows chip operation to resume quickly. If the application uses the main oscillator or the PLL, software must enable these components and wait for them to stabilize. Only then can the system use the PLL and main oscillator as a clock source.

7.18.5 Power control

The LPC11U3x support various power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate can also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This power control mechanism allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals. This register allows fine-tuning of power

consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.18.5.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC11U3x for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

Remark: When using the USB, configure the LPC11U3x in Default mode.

7.18.5.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and can generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, by memory systems and related controllers, and by internal buses.

7.18.5.3 Deep-sleep mode

In Deep-sleep mode, the LPC11U3x is in Sleep-mode and all peripheral clocks and all clock sources are off except for the IRC. The IRC output is disabled unless the IRC is selected as input to the watchdog timer. In addition all analog blocks are shut down and the flash is in stand-by mode. In Deep-sleep mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

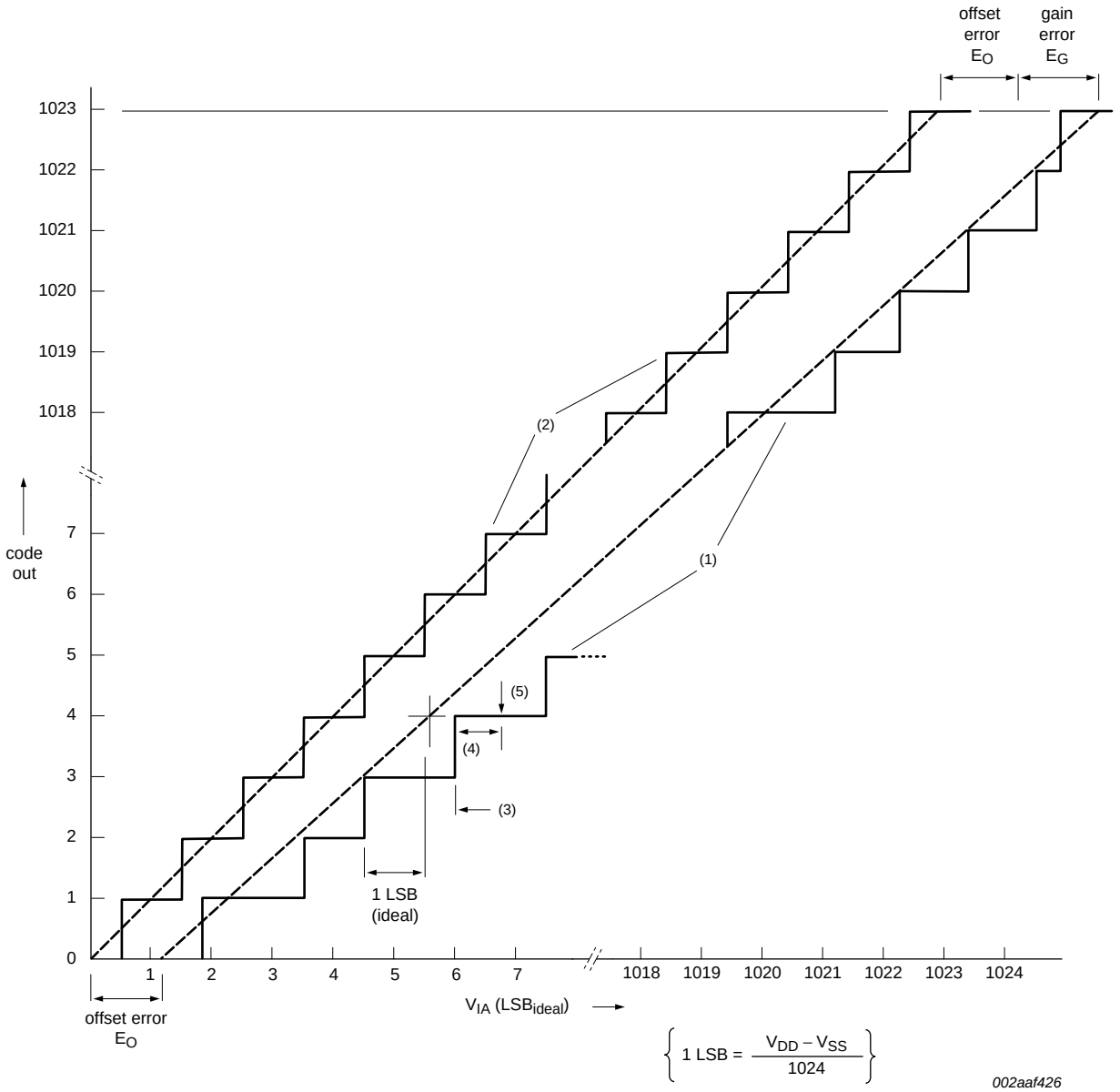
The LPC11U3x can wake up from Deep-sleep mode via reset, selected GPIO pins, a watchdog timer interrupt, or an interrupt generating USB port activity.

Deep-sleep mode saves power and allows for short wake-up times.

7.18.5.4 Power-down mode

In Power-down mode, the LPC11U3x is in Sleep-mode and all peripheral clocks and all clock sources are off except for watchdog oscillator if selected. In addition all analog blocks and the flash are shut down. In Power-down mode, the application can keep the BOD circuit running for BOD protection.

The LPC11U3x can wake up from Power-down mode via reset, selected GPIO pins, a watchdog timer interrupt, or an interrupt generating USB port activity.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 8. ADC characteristics

9.1 BOD static characteristics

Table 7. BOD static characteristics[1]
T_{amb} = 25 °C.

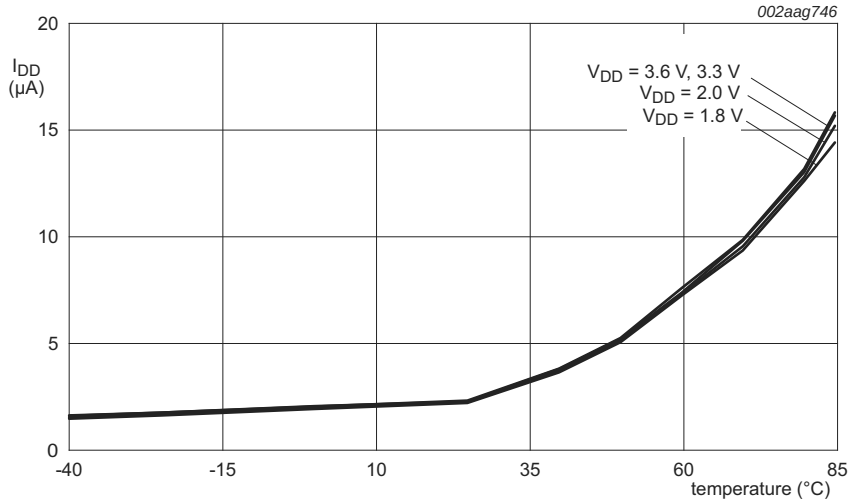
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1				
		assertion	-	2.22	-	V
		de-assertion	-	2.35	-	V
		interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V
		reset level 0				
		assertion	-	1.46	-	V
		de-assertion	-	1.63	-	V
		reset level 1				
		assertion	-	2.06	-	V
		de-assertion	-	2.15	-	V
		reset level 2				
		assertion	-	2.35	-	V
		de-assertion	-	2.43	-	V
		reset level 3				
		assertion	-	2.63	-	V
		de-assertion	-	2.71	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *the LPC11Uxx user manual*.

9.2 Power consumption

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see the *LPC11Uxx user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.



Conditions: BOD disabled; all oscillators and analog blocks turned off in the PDSLEEPCFG register; USB_DP and USB_DM pulled LOW externally.

Fig 13. Typical supply current versus temperature in Power-down mode

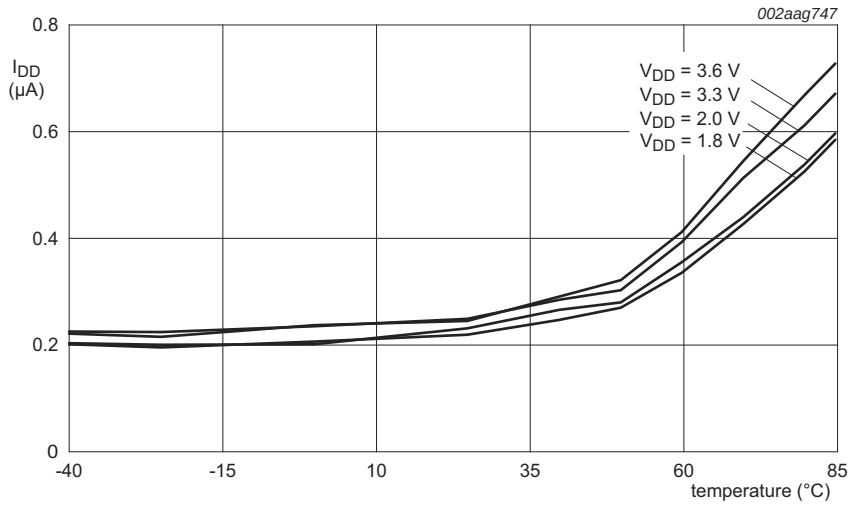


Fig 14. Typical supply current versus temperature in Deep power-down mode

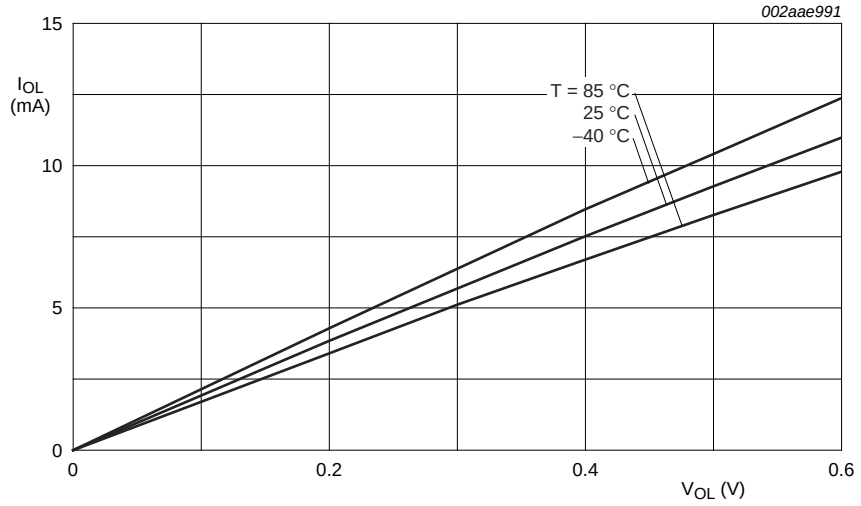
9.3 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

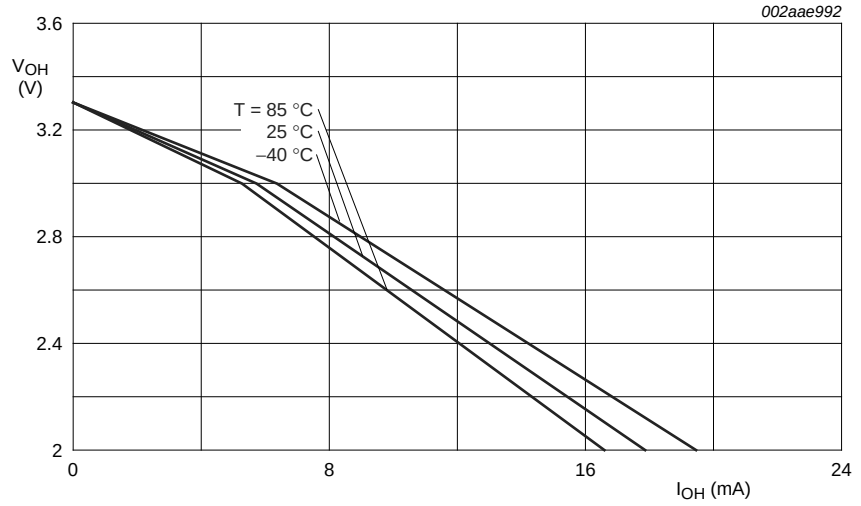
Table 8. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.27	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.22	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	0.004	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.051	-	-	Independent of main clock frequency.
Main PLL	-	0.21	-	-
ADC	-	0.08	0.29	-
CLKOUT	-	0.12	0.47	Main clock divided by 4 in the CLKOUTDIV register.
CT16B0	-	0.02	0.06	-
CT16B1	-	0.02	0.06	-
CT32B0	-	0.02	0.07	-
CT32B1	-	0.02	0.06	-
GPIO	-	0.23	0.88	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCONFIG	-	0.03	0.10	-
I^2C	-	0.04	0.13	-
ROM	-	0.04	0.15	-
SPI0	-	0.12	0.45	-
SPI1	-	0.12	0.45	-
UART	-	0.22	0.82	-
WWDT	-	0.02	0.06	Main clock selected as clock source for the WDT.
USB	-	-	1.2	-



Conditions: V_{DD} = 3.3 V; standard port pins and PIO0_7.

Fig 17. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 18. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +85 °C) is ±40 %.

[3] See the *LPC11Uxx user manual.*

10.4 I/O pins

Table 14. Dynamic characteristics: I/O pins[1]

T_{amb} = −40 °C to +85 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

10.5 I²C-bus

Table 15. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	Standard-mode	0	100	kHz
		Fast-mode	0	400	kHz
		Fast-mode Plus	0	1	MHz
t_f	fall time [4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
		Fast-mode	20 + 0.1 × C_b	300	ns
		Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock	Standard-mode	4.7	-	µs
		Fast-mode	1.3	-	µs
		Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock	Standard-mode	4.0	-	µs
		Fast-mode	0.6	-	µs
		Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time [3][4][8]	Standard-mode	0	-	µs
		Fast-mode	0	-	µs
		Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time [9][10]	Standard-mode	250	-	ns
		Fast-mode	100	-	ns
		Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

Table 18. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 19. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

11.3 XTAL Printed-Circuit Board (PCB) layout guidelines

Follow these guidelines for PCB layout:

- Connect the crystal on the PCB as close as possible to the oscillator input and output pins of the chip.
- Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal use have a common ground plane.
- Connect the external components to the ground plain.
- To keep parasitics and the noise coupled in via the PCB as small as possible, keep loops as small as possible.
- Choose smaller values of C_{x1} and C_{x2} if parasitics of the PCB layout increase.

Under nominal operating condition V_{DD} = 3.3 V and with the maximum sampling frequency fs = 400 kHz, the parameters assume the following values:

C_{ia} = 1 pF (max)

R_{mux} = 2 kΩ (max)

R_{sw} = 1.3 kΩ (max)

C_{io} = 7.1 pF (max)

The effective input impedance with these parameters is R_{in} = 308 kΩ.

11.7 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 6:

- The ADC input trace must be short and as close as possible to the LPC11U3x chip.
- Shield The ADC input traces from fast switching digital signals and noisy power supply lines.
- The ADC and the digital core share the same power supply. Therefore, filter the power supply line adequately.
- To improve the ADC performance in a noisy environment, put the device in Sleep mode during the ADC conversion.

11.8 I/O Handler software library applications

The following sections provide application examples for the I/O Handler software library. All library examples make use of the I/O Handler hardware to extend the functionality of the part through software library calls. The libraries are available on http://www.LPCware.com.

11.8.1 I/O Handler I^2S

The I/O Handler software library provides functions to emulate an I^2S master transmit interface using the I/O Handler hardware block.

The emulated I^2S interface loops over a 1 kB buffer, transmitting the datawords according to the I^2S protocol. Interrupts are generated every time when the first 512 bytes have been transmitted and when the last 512 bytes have been transmitted. This allows the ARM core to load the free portion of the buffer with new data, thereby enabling streaming audio.

Two channels with 16-bit per channel are supported. The code size of the software library is 1 kB and code must be executed from the SRAM1 memory area reserved for the I/O Handler code.

11.8.2 I/O Handler UART

The I/O Handler UART library emulates one additional full-duplex UART. The emulated UART can be configured for 7 or 8 data bits, no parity, and 1 or 2 stop bits. The baud rate is configurable up to 115200 baud. The RXD signal is available on three I/O Handler pins (IOH_6, IOH_16, IOH_20), while TXD and CTS are available on all 21 I/O Handler pins.

The code size of the software library is about 1.2 kB and code must be executed from the SRAM1 memory area reserved for the I/O Handler code.

11.8.3 I/O Handler I²C

The I/O Handler I²C library allows to have an additional I²C-bus master. I²C read, I²C write and combined I²C read/write are supported. Data is automatically read from and written to user-defined buffers.

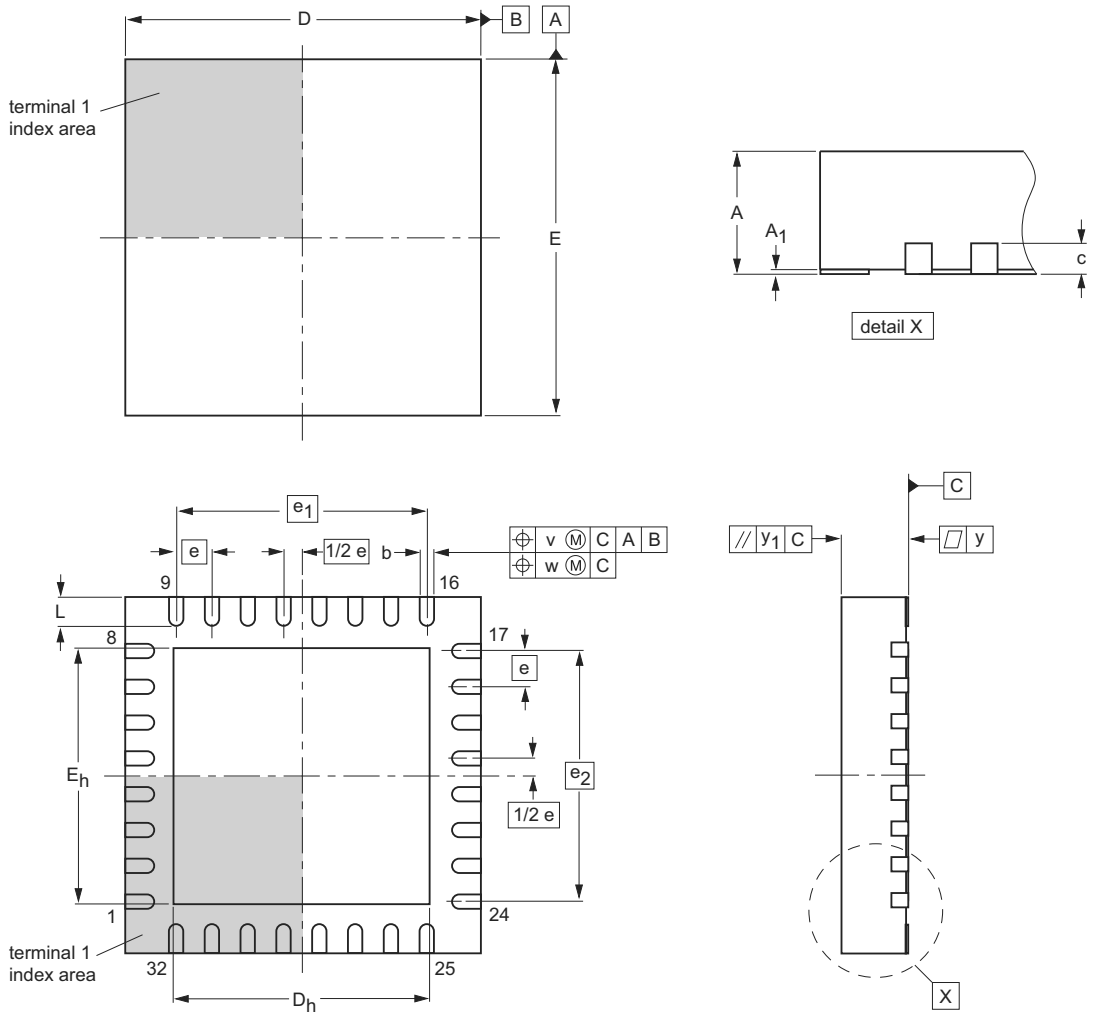
The I/O Handler I²C library combined with the on-chip I²C module allows to have two distinct I²C buses, allowing to separate low-speed from high-speed devices or bridging two I²C buses.

11.8.4 I/O Handler DMA

The I/O Handler DMA library offers DMA-like functionality. Four types of transfer are supported: memory to memory, memory to peripheral, peripheral to memory and peripheral to peripheral. Supported peripherals are USART, SSP0/1, ADC and GPIO. DMA transfers can be triggered by the source/target peripheral, software, counter/timer module CT16B1, or I/O Handler pin PIO1_6/IOH_16.

12. Package outline

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm



Dimensions (mm are the original dimensions)

Unit[1]		A[1]	A_1	b	c	D[1]	D_h	E[1]	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	0.85	0.05	0.30	0.2	5.1	3.75	5.1	3.75	0.5	3.5	3.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

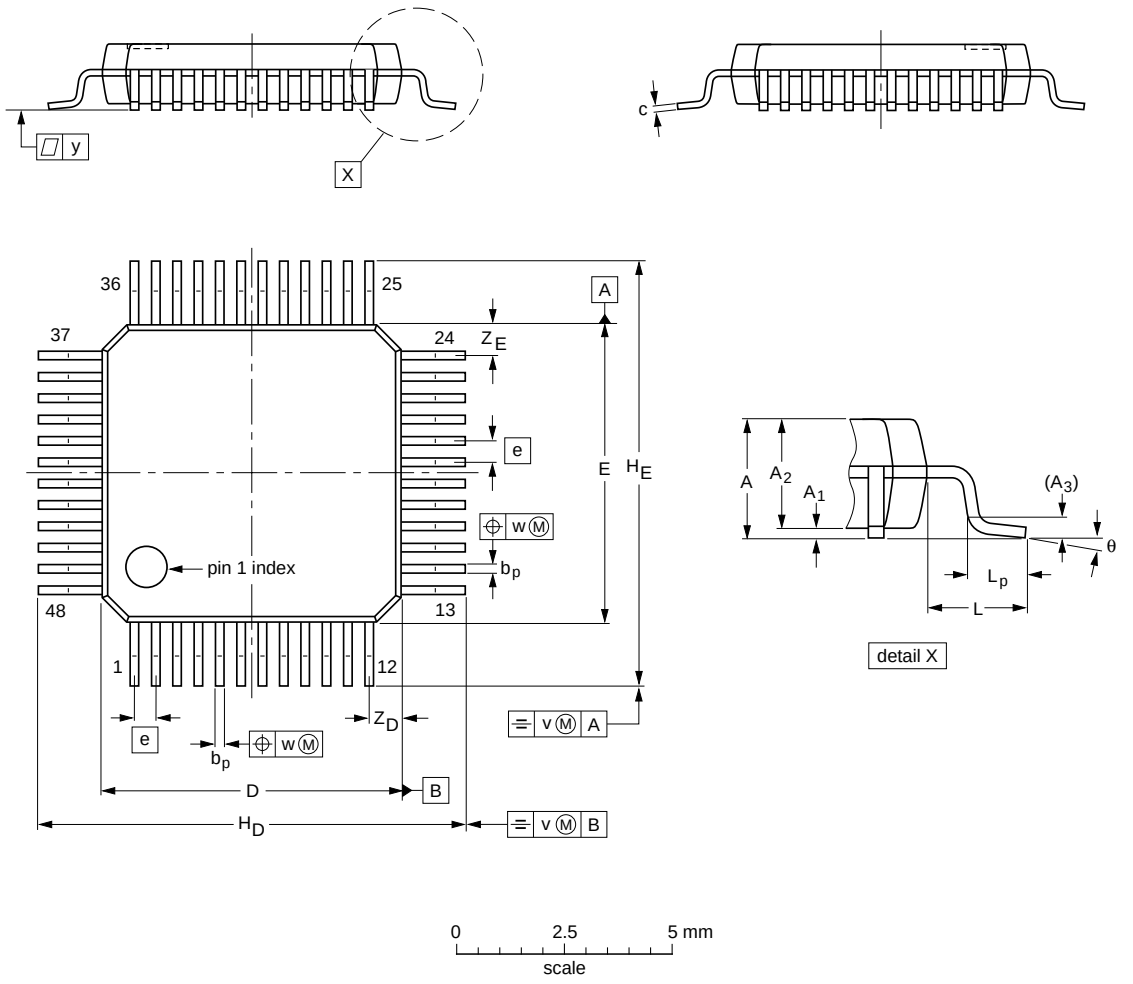
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33f_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		MO-220				~~11-10-11~~ 11-10-17

Fig 34. Package outline HVQFN33 (5 x 5 x 0.85 mm)

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

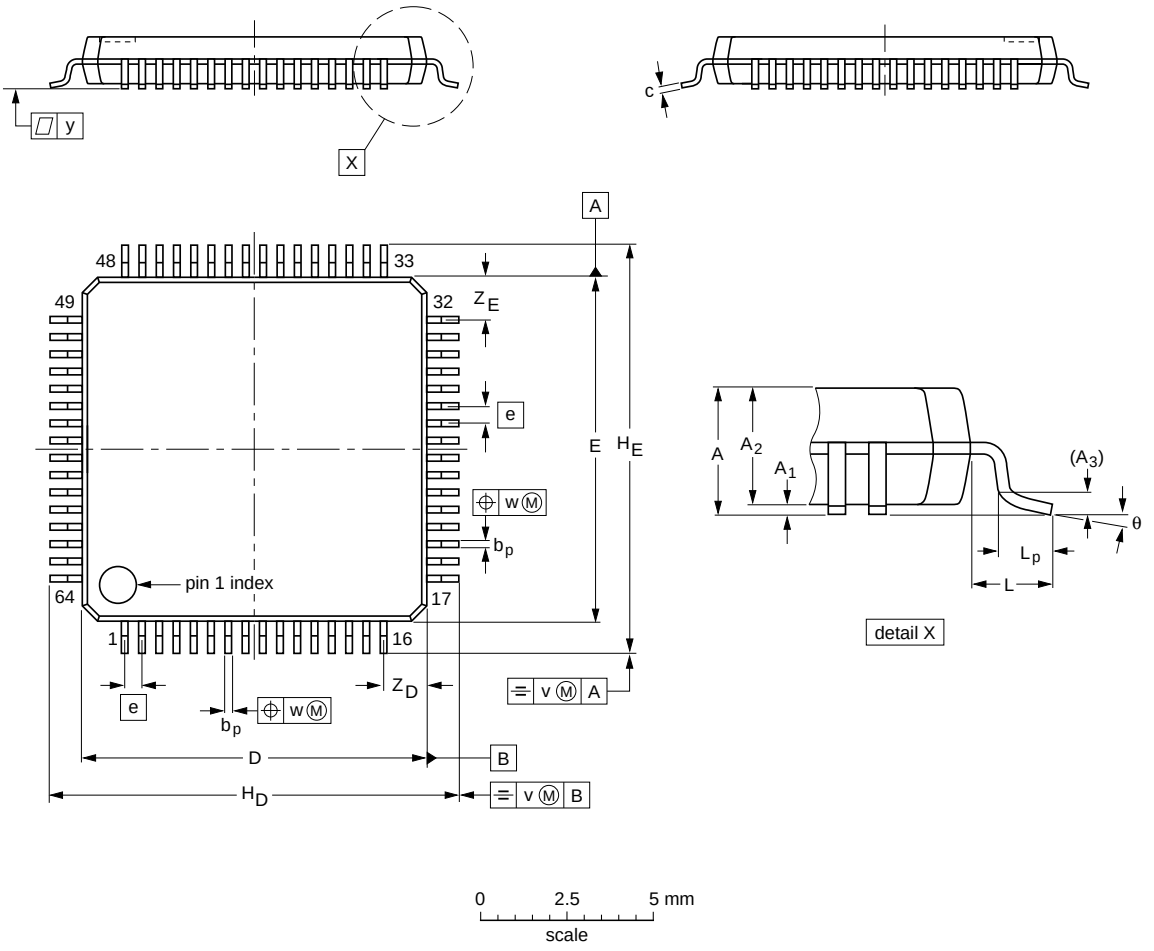
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 37. Package outline LQFP48 (SOT313-2)

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 38. Package outline LQFP64 (SOT314-2)

Footprint information for reflow soldering of HVQFN33 package

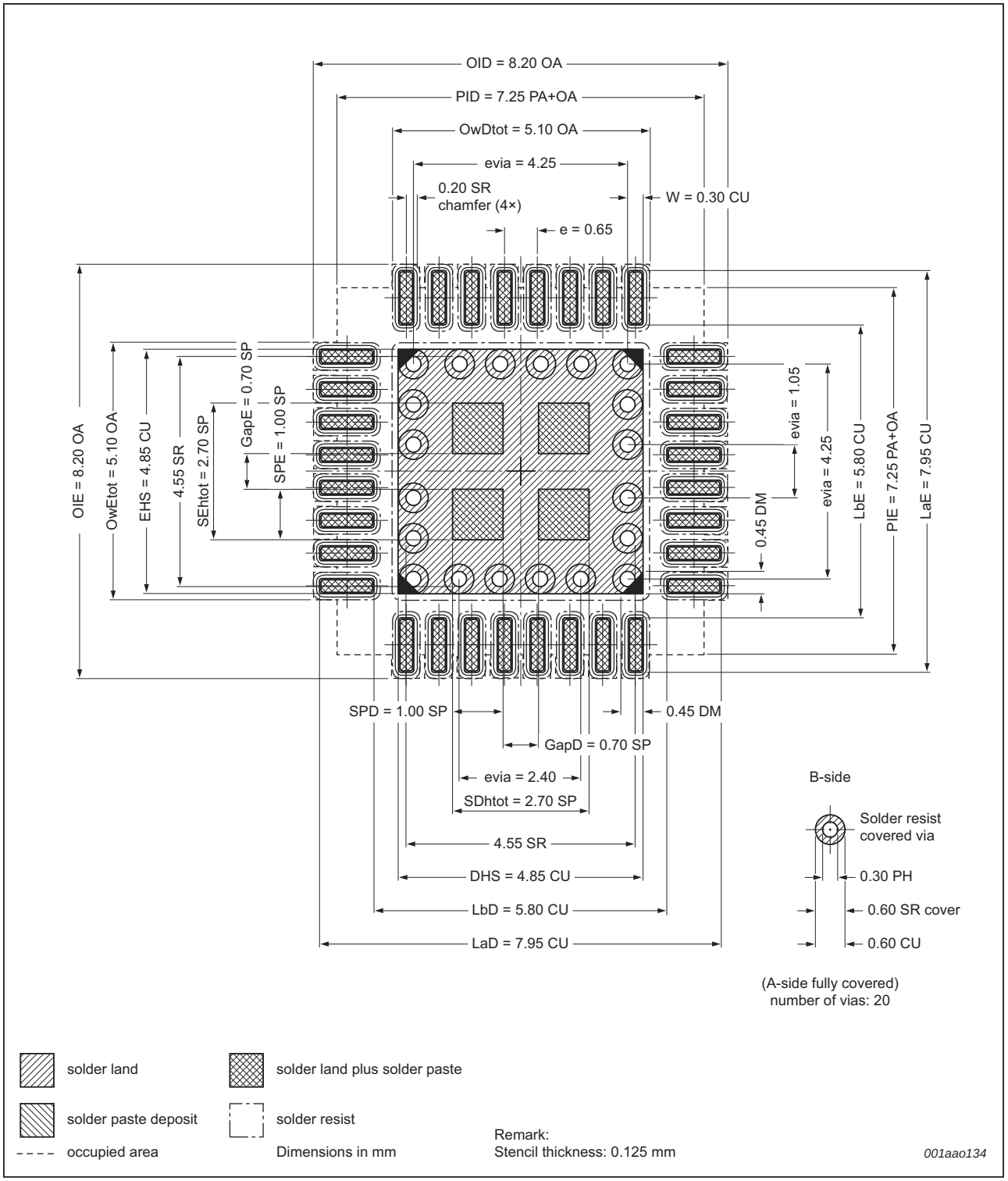


Fig 40. Reflow soldering for the HVQFN33 (7x7) package