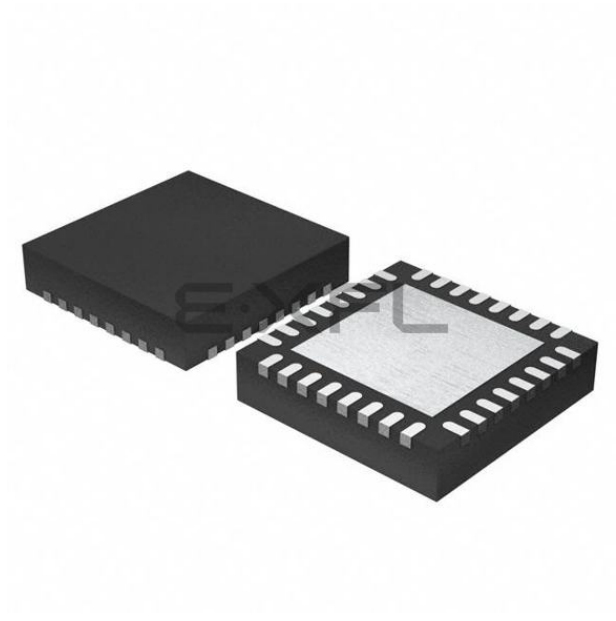

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SmartCard, SPI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11u35fhi33-501y

- Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.

- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.
  - Power profiles residing in boot ROM provide optimized performance and minimized power consumption for any given application through one simple function call.
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Processor wake-up from Deep-sleep and Power-down modes via reset, selectable GPIO pins, watchdog interrupt, or USB port activity.
  - Processor wake-up from Deep power-down mode using one special function pin.
  - Power-On Reset (POR).
  - Brownout detect with up to four separate thresholds for interrupt and forced reset.
- Unique device serial number for identification.
- Single 3.3 V power supply (1.8 V to 3.6 V).
- Temperature range −40 °C to +85 °C.
- Available as LQFP64, LQFP48, TFBGA48, and HVQFN33 packages.

3. Applications

- Consumer peripherals
- Medical
- Industrial control
- Handheld scanners
- USB audio devices

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC11U34FHN33/311	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11U34FBD48/311	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U34FHN33/421	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11U34FBD48/421	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U35FHN33/401	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11U35FBD48/401	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U35FBD64/401	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11U35FHI33/501	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC11U35FET48/501	TFBGA48	plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 × 4.5 × 0.7 mm	SOT1155-2
LPC11U36FBD48/401	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

Table 1. Ordering information *…continued*

Type number	Package		
	Name	Description	Version
LPC11U36FBD64/401	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11U37FBD48/401	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U37HFBD64/401	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11U37FBD64/501	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

4.1 Ordering options

Table 2. Ordering options

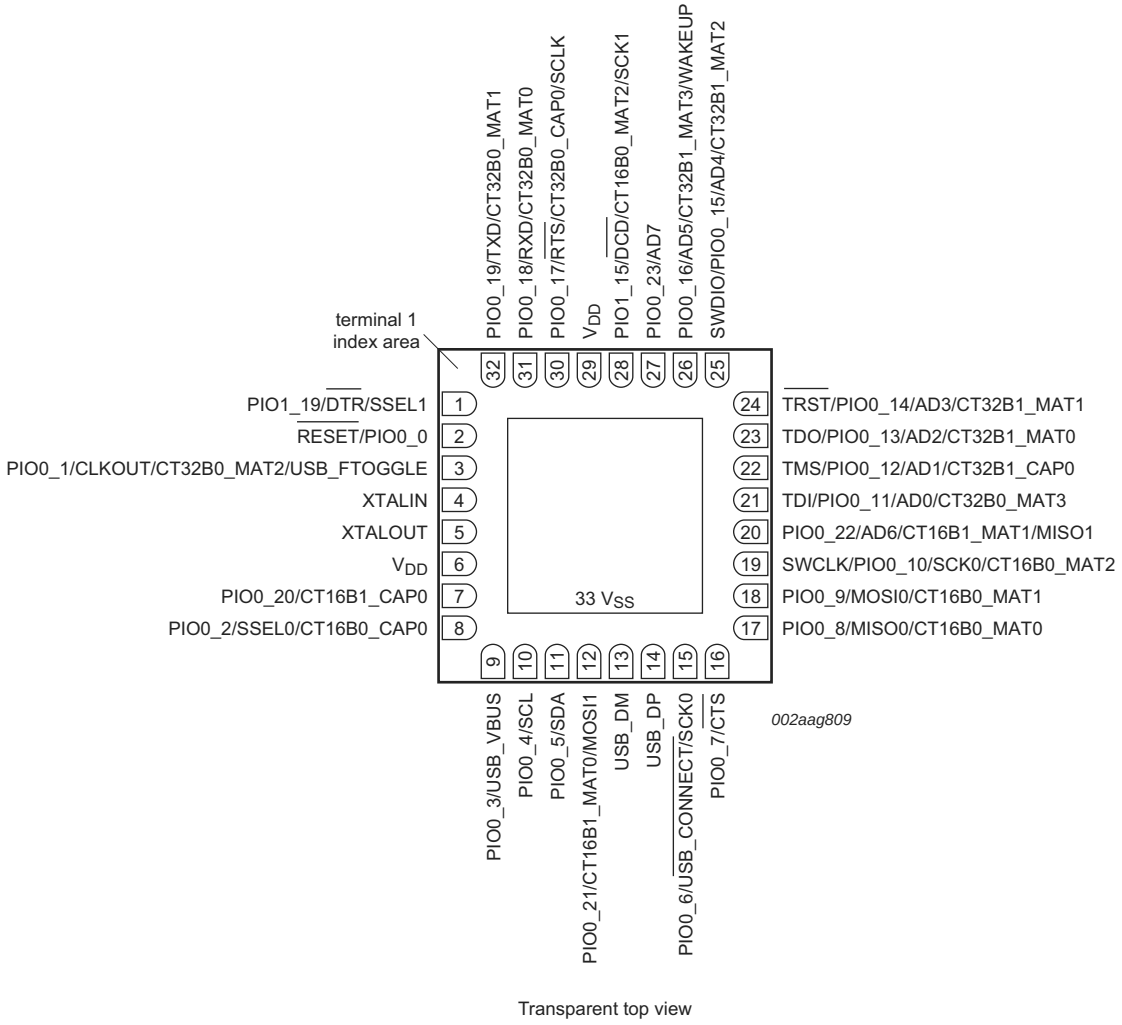
Type number	Flash in kB	EEPROM in kB	SRAM0 in kB	USB SRAM in kB	SRAM1 in kB	Total SRAM in kB[1]	I/O Handler	USART	I²C-bus FM+	SSP	USB device	ADC channels	GPIO pins
LPC11U34FHN33/311	40	4	8	-	-	8	no	1	1	2	1	8	26
LPC11U34FBD48/311	40	4	8	-	-	8	no	1	1	2	1	8	40
LPC11U34FHN33/421	48	4	8	2	-	10	no	1	1	2	1	8	26
LPC11U34FBD48/421	48	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U35FHN33/401	64	4	8	2	-	10	no	1	1	2	1	8	26
LPC11U35FBD48/401	64	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U35FBD64/401	64	4	8	2	-	10	no	1	1	2	1	8	54
LPC11U35FHI33/501	64	4	8	2	2[1]	12	no	1	1	2	1	8	26
LPC11U35FET48/501	64	4	8	2	2[1]	12	no	1	1	2	1	8	40
LPC11U36FBD48/401	96	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U36FBD64/401	96	4	8	2	-	10	no	1	1	2	1	8	54
LPC11U37FBD48/401	128	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U37HFBD64/401	128	4	8	2	2[2]	10	yes	1	1	2	1	8	54
LPC11U37FBD64/501	128	4	8	2	2[1]	12	no	1	1	2	1	8	54

[1] For general-purpose use.

[2] For I/O Handler use only.

6. Pinning information

6.1 Pinning



Transparent top view

For parts LPC11U34FHN33/311, LPC11U34FHN33/421, LPC11U35FHN33/401, LPC11U35FHI33/501

Fig 2. Pin configuration (HVQFN33)

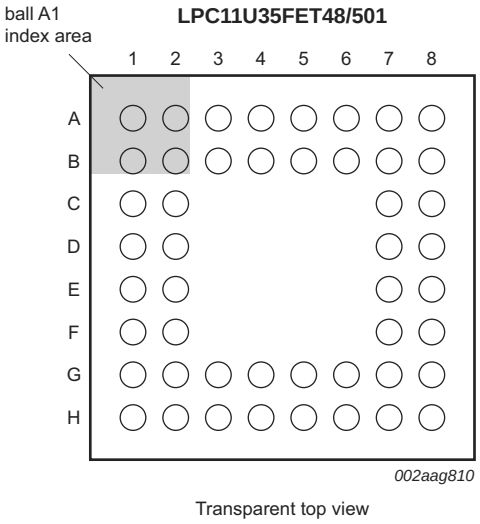


Fig 3. Pin configuration (TFBGA48)

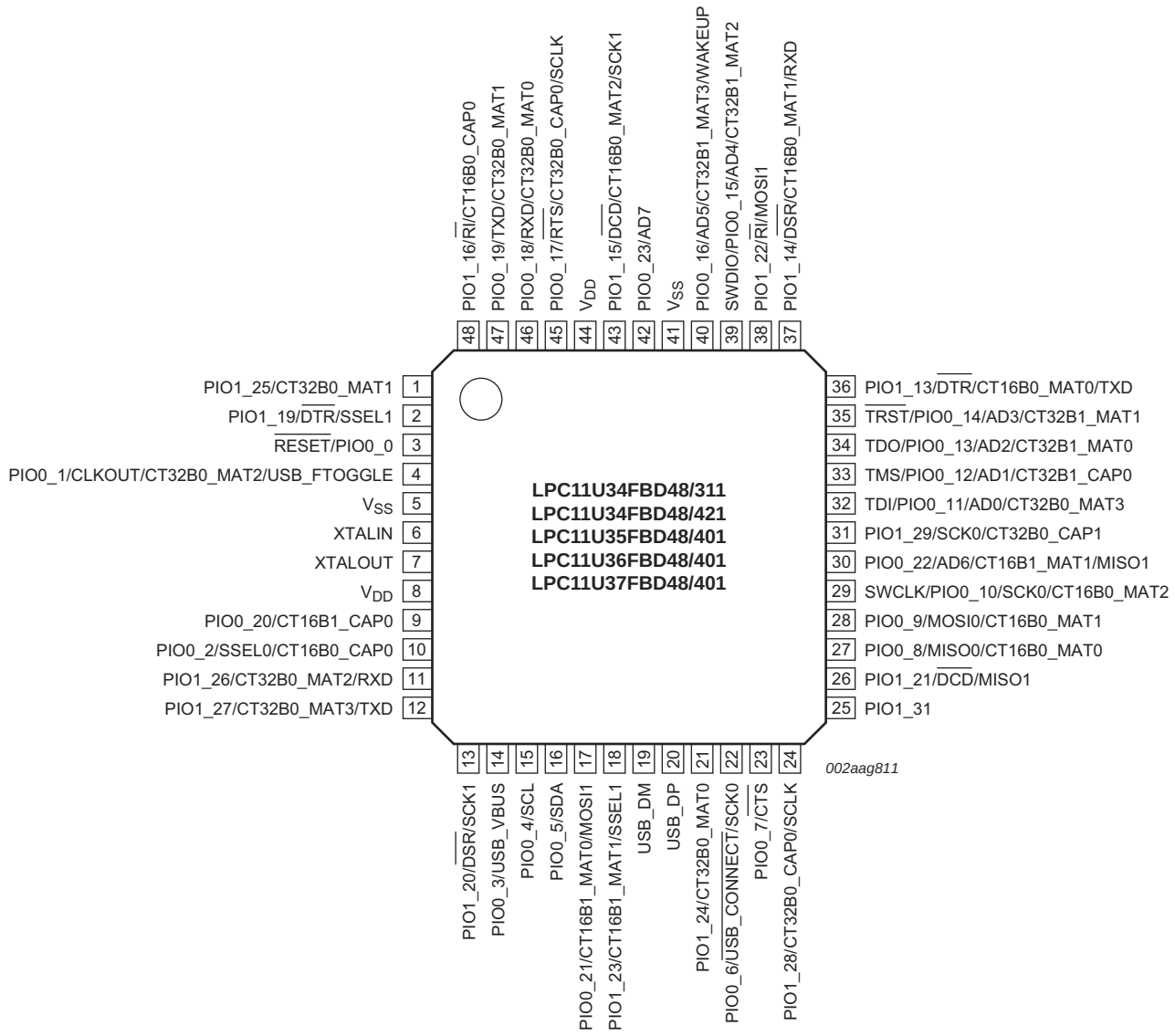


Fig 4. Pin configuration (LQFP48)

6.2 Pin description

Table 3 shows all pins and their assigned digital or analog functions in order of the GPIO port number. The default function after reset is listed first. All port pins have internal pull-up resistors enabled after reset except for the true open-drain pins PIO0_4 and PIO0_5.

Every port pin has a corresponding IOCON register for programming the digital or analog function, the pull-up/pull-down configuration, the repeater, and the open-drain modes.

The USART, counter/timer, and SSP functions are available on more than one port pin.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
RESET/PIO0_0	2	C1	3	4 [2]	I; PU	I	**RESET —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode. In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed and Deep power-down mode is not used.
					-	I/O	**PIO0_0 —** General purpose digital input/output pin.
PIO0_1/CLKOUT/ CT32B0_MAT2/ USB_FTOGGLE	3	C2	4	5 [3]	I; PU	I/O	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler or the USB device enumeration.
					-	O	**CLKOUT —** Clockout pin.
					-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					-	O	**USB_FTOGGLE —** USB 1 ms Start-of-Frame signal.
PIO0_2/SSEL0/ CT16B0_CAP0/IOH_0	8	F1	10	13 [3]	I; PU	I/O	**PIO0_2 —** General purpose digital input/output pin.
					-	I/O	**SSEL0 —** Slave select for SSP0.
					-	I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
					-	I/O	**IOH_0 —** I/O Handler input/output 0. LPC11U37HFBD64/401 only.
PIO0_3/USB_VBUS/ IOH_1	9	H2	14	19 [3]	I; PU	I/O	**PIO0_3 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler. A HIGH level during reset starts the USB device enumeration.
					-	I	**USB_VBUS —** Monitors the presence of USB bus power.
					-	I/O	**IOH_1 —** I/O Handler input/output 1. LPC11U37HFBD64/401 only.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
PIO1_28/CT32B0_CAP0/ SCLK	-	H7	24	31 [3]	I; PU	I/O	**PIO1_28 —** General purpose digital input/output pin.
					-	I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
					-	I/O	**SCLK —** Serial clock input/output for USART in synchronous mode.
PIO1_29/SCK0/ CT32B0_CAP1	-	D7	31	41 [3]	I; PU	I/O	**PIO1_29 —** General purpose digital input/output pin.
					-	I/O	**SCK0 —** Serial clock for SSP0.
					-	I	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0.
PIO1_31	-	-	25	- [3]	I; PU	I/O	**PIO1_31 —** General purpose digital input/output pin.
USB_DM	13	G5	19	25 [7]	F	-	**USB_DM —** USB bidirectional D− line.
USB_DP	14	H5	20	26 [7]	F	-	**USB_DP —** USB bidirectional D+ line.
XTALIN	4	D1	6	8 [8]	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	5	E1	7	9 [8]	-	-	Output from the oscillator amplifier.
V_{DD}	6; 29	B4; E2	8; 44	10; 33; 48; 58	-	-	Supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
V_{SS}	33	B5; D2	5; 41	7; 54	-	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; If the pins are not used, tie floating pins to ground or power to minimize power consumption.

[2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See Figure 32 for the reset pad configuration.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 31).

[4] I^2C-bus pin compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 31); includes high-current output driver.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 31); includes digital input glitch filter.

[7] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[8] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). Leave XTALOUT floating.

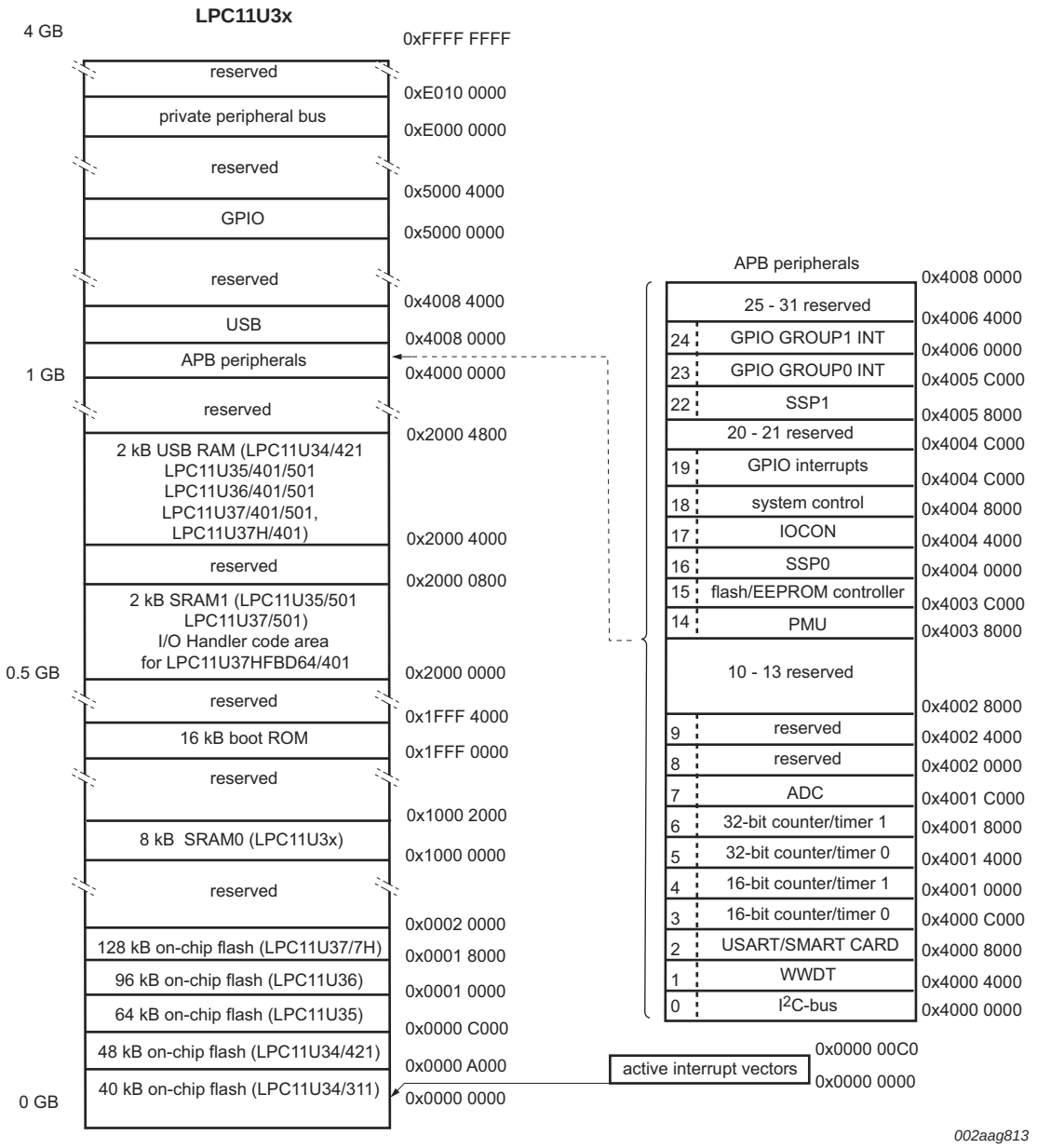


Fig 6. LPC11U3x memory map

7.6 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC11U3x, the NVIC supports 24 vectored interrupts.

application notes from NXP (see http://www.LPCware.com.) LPCXpresso, Keil, and IAR IDEs are supported. I/O Handler library code must be executed from the memory area 0x2000 0000 to 0x2000 07FF. This memory is not available for other use.

For application examples, see Section 11.8 “I/O Handler software library applications”. Each I/O Handler library uses a specific subset of I/O Handler pins and in some cases other pins and peripherals such as the counter/timers.

7.11 USART

The LPC11U3x contains one USART.

The USART includes full modem control, support for synchronous mode, and a smart card interface. The RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The USART uses a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.11.1 Features

- Maximum USART data bit rate of 3.125 Mbit/s.
- 16 byte receive and transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.
- Support for synchronous mode.
- Includes smart card interface.

7.12 SSP serial I/O controller

The SSP controllers operate on a SSP, 4-wire SSI, or Microwire bus. The controller can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bit to 16 bit of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.12.1 Features

- Maximum SSP speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode)
- Compatible with Motorola SPI (Serial Peripheral Interface), 4-wire Texas Instruments SSI (Serial Synchronous Interface), and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation

- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.13 I²C-bus serial I/O controller

The LPC11U3x contain one I²C-bus controller.

The I²C-bus is bidirectional for inter-IC control using only two wires: a Serial CLock line (SCL) and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C-bus is a multi-master bus, and more than one bus master connected to the interface can be controlled the bus.

7.13.1 Features

- The I²C-interface is an I²C-bus compliant interface with open-drain pins. The I²C-bus interface supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus can be used for test and diagnostic purposes.
- The I²C-bus controller supports multiple address recognition and a bus monitor mode.

7.14 10-bit ADC

The LPC11U3x contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

7.14.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to V_{DD}.
- 10-bit conversion time $\geq$ 2.44 μs (up to 400 kSamples/s).
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

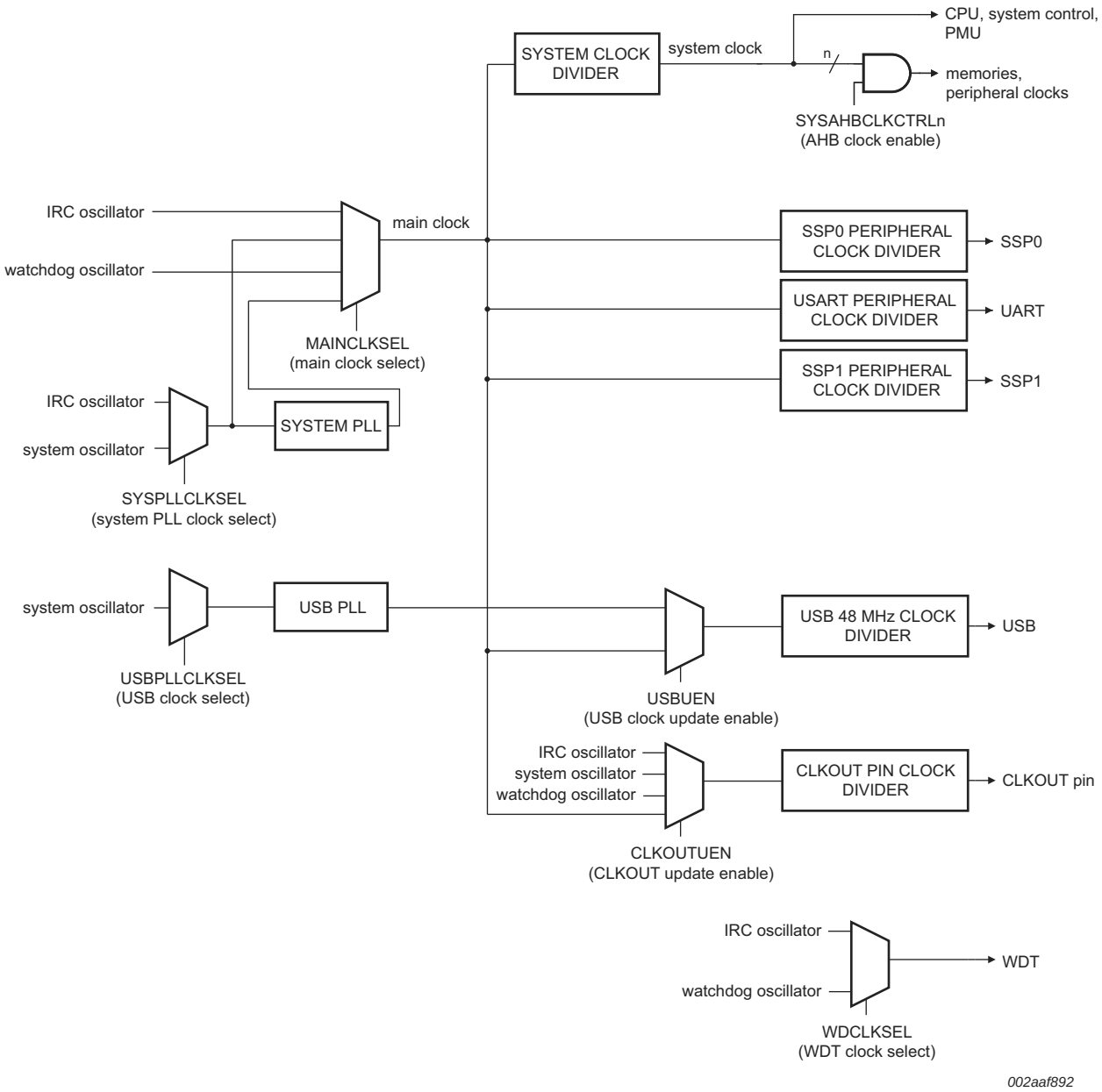


Fig 7. LPC11U3x clocking generation block diagram

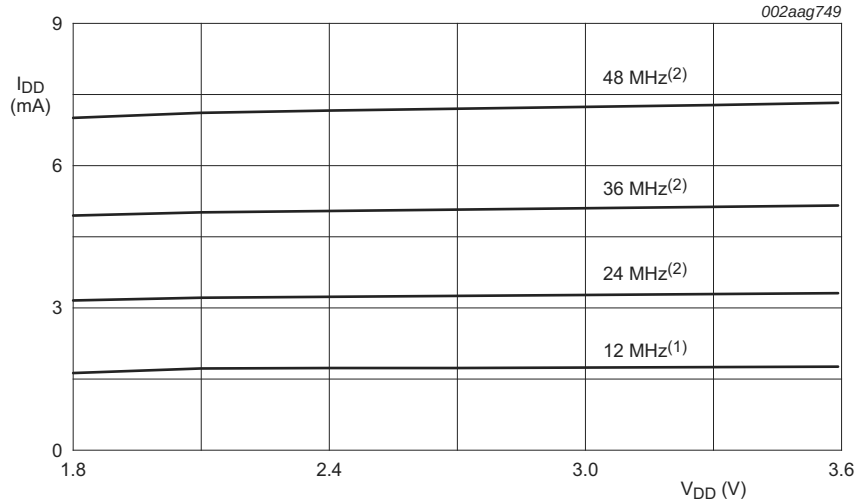
7.18.1.1 Internal RC oscillator

The IRC can be used as the clock source for the WDT, and/or as the clock that drives the system PLL and then the CPU. The nominal IRC frequency is 12 MHz.

Upon power-up, any chip reset, or wake-up from Deep power-down mode, the LPC11U3x use the IRC as the clock source. Software can later switch to one of the other available clock sources.

Table 5. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.0 V ≤ V_{DD} ≤ 3.6 V	4	-	-	mA
		1.8 V ≤ V_{DD} < 2.0 V	3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V [13]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD} [13]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V; 2.0 V ≤ V_{DD} ≤ 3.6 V	−15	−50	−85	μA
		1.8 V ≤ V_{DD} < 2.0 V	−10	−50	−85	μA
		V_{DD} < V_I < 5 V	0	0	0	μA
High-drive output pin (PIO0_7)						
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled	-	0.5	10	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled	-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function; V_{DD} ≥ 1.8 V [11] [12]	0	-	5.0	V
		V_{DD} = 0 V	0	-	3.6	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage		0.4	-	-	V
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = −20 mA	V_{DD} − 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OH} = −12 mA	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.0 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA	-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.0 V; I_{OL} = 3 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 2.5 V ≤ V_{DD} ≤ 3.6 V	20	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V	12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.0 V ≤ V_{DD} ≤ 3.6 V	4	-	-	mA
		1.8 V ≤ V_{DD} < 2.0 V	3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD} [13]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	10	50	150	μA

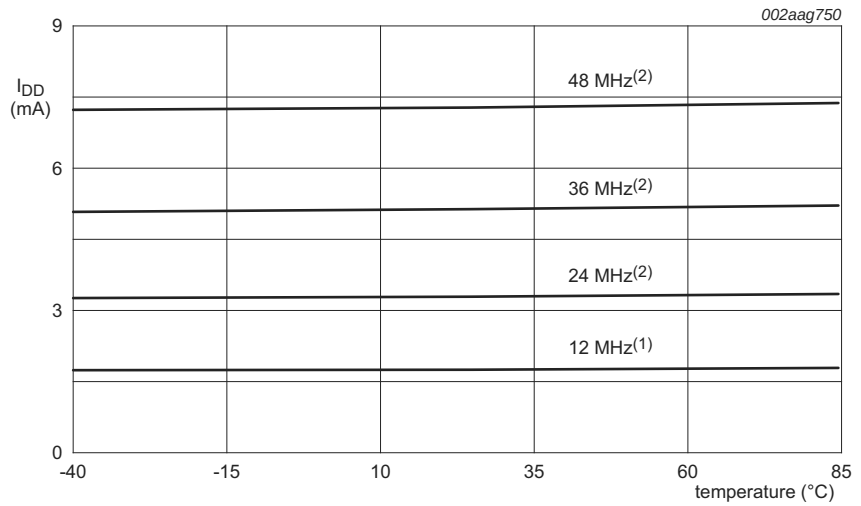


Conditions: T_{amb} = 25 °C; Active mode entered executing code `while(1){}` from flash; internal pull-up resistors disabled; BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; low-current mode; USB_DP and USB_DM pulled LOW externally.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 9. Typical supply current versus regulator supply voltage V_{DD} in active mode



Conditions: V_{DD} = 3.3 V; Active mode entered executing code `while(1){}` from flash; internal pull-up resistors disabled; BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; low-current mode; USB_DP and USB_DM pulled LOW externally.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 10. Typical supply current versus temperature in Active mode

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +85 °C) is ±40 %.

[3] See the *LPC11Uxx user manual.*

10.4 I/O pins

Table 14. Dynamic characteristics: I/O pins[1]

T_{amb} = −40 °C to +85 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

10.5 I²C-bus

Table 15. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	Standard-mode	0	100	kHz
		Fast-mode	0	400	kHz
		Fast-mode Plus	0	1	MHz
t_f	fall time [4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
		Fast-mode	20 + 0.1 × C_b	300	ns
		Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock	Standard-mode	4.7	-	µs
		Fast-mode	1.3	-	µs
		Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock	Standard-mode	4.0	-	µs
		Fast-mode	0.6	-	µs
		Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time [3][4][8]	Standard-mode	0	-	µs
		Fast-mode	0	-	µs
		Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time [9][10]	Standard-mode	250	-	ns
		Fast-mode	100	-	ns
		Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

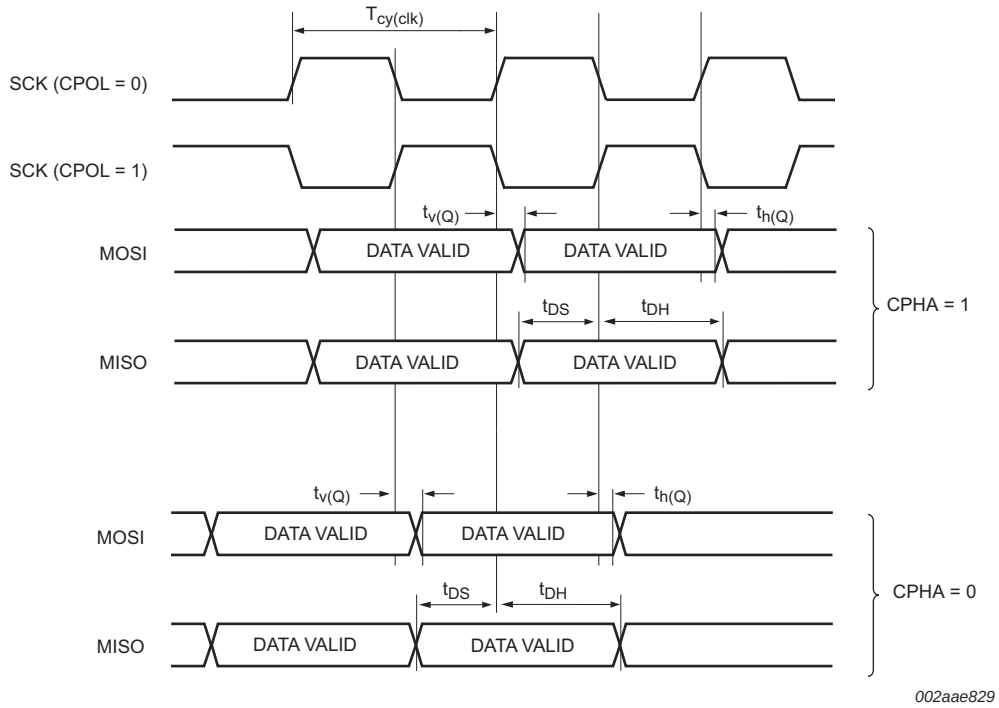


Fig 24. SSP master timing in SPI mode

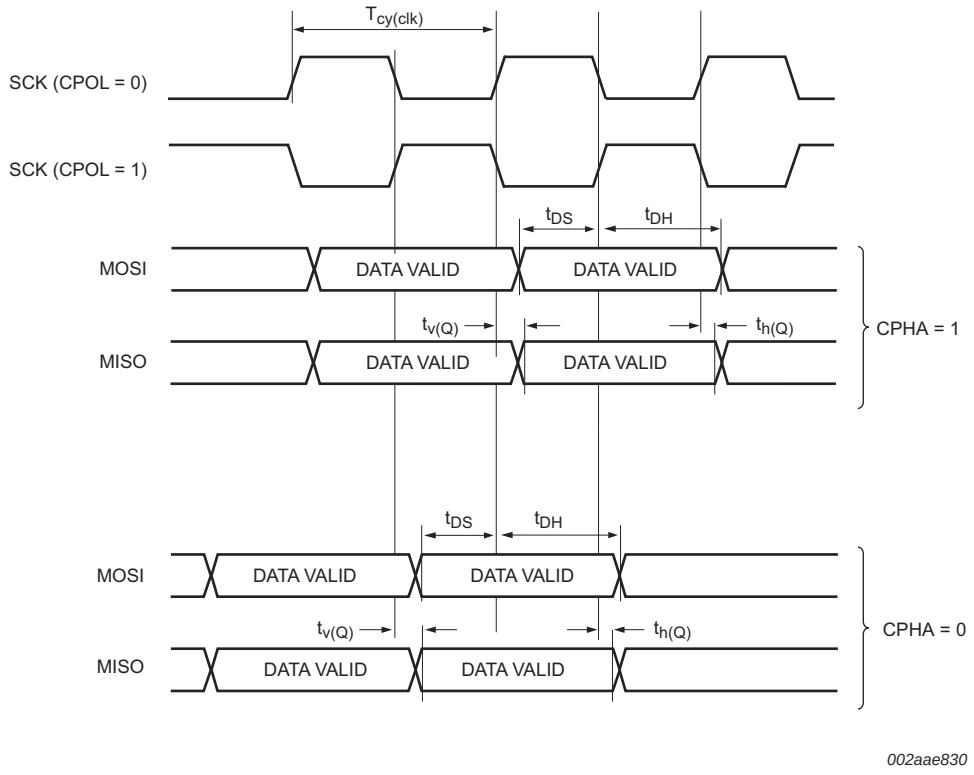


Fig 25. SSP slave timing in SPI mode

11.5 Reset pad configuration

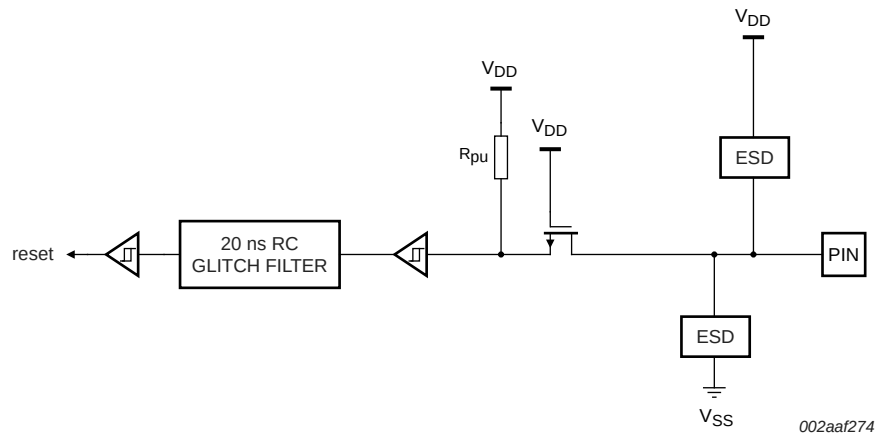


Fig 32. Reset pad configuration

11.6 ADC effective input impedance

A simplified diagram of the ADC input channels can be used to determine the effective input impedance seen from an external voltage source. See Figure 33.

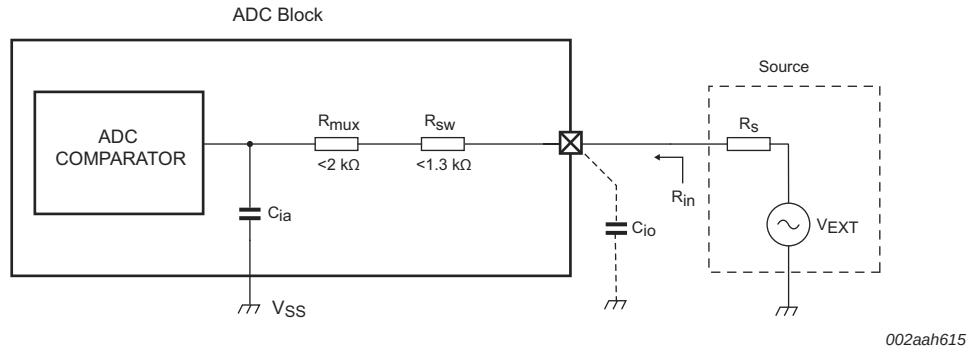


Fig 33. ADC input channel

The effective input impedance, R_{in}, seen by the external voltage source, V_{EXT}, is the parallel impedance of ($(1/f_s \times C_{ia}) + R_{mux} + R_{sw}$) and ($1/f_s \times C_{io}$), and can be calculated using Equation 1 with

f_s = sampling frequency

C_{ia} = ADC analog input capacitance

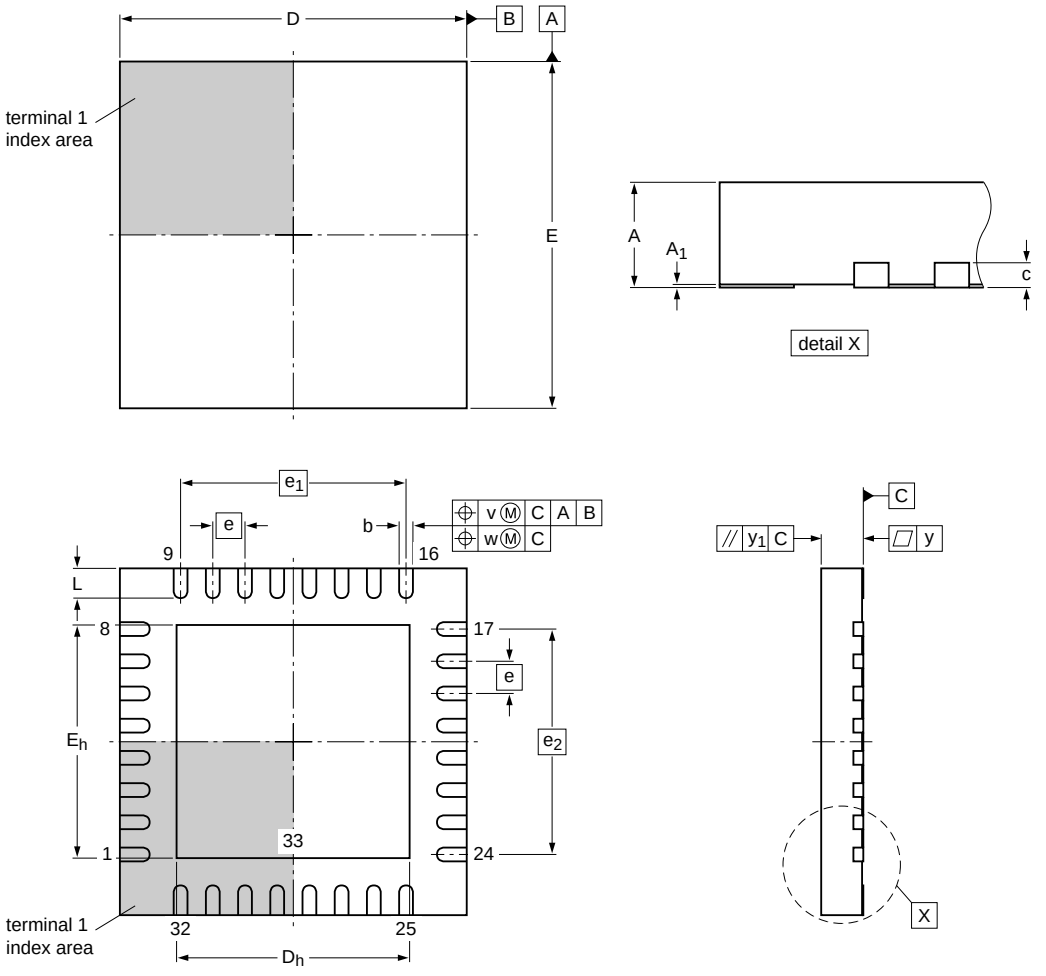
R_{mux} = analog mux resistance

R_{sw} = switch resistance

C_{io} = pin capacitance

$$R_{in} = \left(\frac{1}{f_s \times C_{ia}} + R_{mux} + R_{sw}\right) \parallel \left(\frac{1}{f_s \times C_{io}}\right) \quad (1)$$

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.35		7.1	4.85	7.1	4.85				0.75				
mm	nom	0.85	0.02	0.28	0.2	7.0	4.70	7.0	4.70	0.65	4.55	4.55	0.60	0.1	0.05	0.08	0.1
	min	0.80	0.00	0.23		6.9	4.55	6.9	4.55				0.45				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		- - -				~~09-03-17~~ 09-03-23

Fig 35. Package outline HVQFN33 (7 x 7 x 0.85 mm)

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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