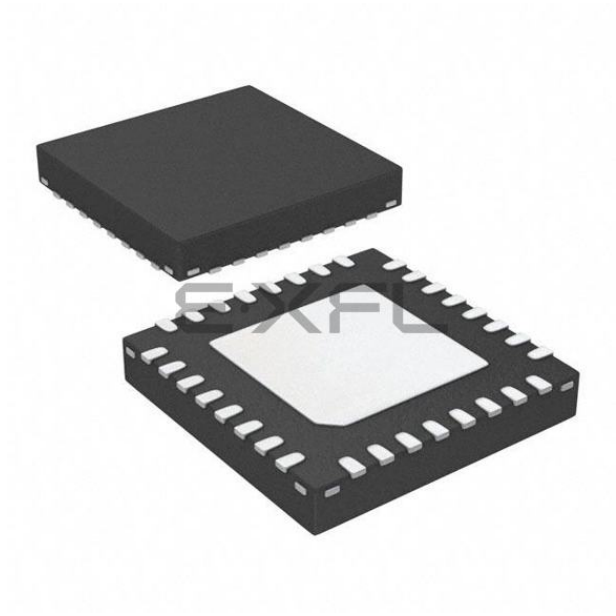

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SmartCard, SPI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11u35fhn33-401

- 4 kB on-chip EEPROM data memory; byte erasable and byte programmable; on-chip API support.
- Up to 12 kB SRAM data memory.
- 16 kB boot ROM.
- In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
- ROM-based USB drivers. Flash updates via USB supported.
- ROM-based 32-bit integer division routines.

- Debug options:
  - Standard JTAG (Joint Test Action Group) test interface for BSDL (Boundary Scan Description Language).
  - Serial Wire Debug.
- Digital peripherals:
  - Up to 54 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, repeater mode, and open-drain mode.
  - Up to 8 GPIO pins can be selected as edge and level sensitive interrupt sources.
  - Two GPIO grouped interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
  - High-current source output driver (20 mA) on one pin.
  - High-current sink driver (20 mA) on true open-drain pins.
  - Four general purpose counter/timers with a total of up to 8 capture inputs and 13 match outputs.
  - Programmable Windowed WatchDog Timer (WWDT) with a dedicated, internal low-power WatchDog Oscillator (WDO).
- Analog peripherals:
  - 10-bit ADC with input multiplexing among eight pins.
- Serial interfaces:
  - USB 2.0 full-speed device controller.
  - USART with fractional baud rate generation, internal FIFO, a full modem control handshake interface, and support for RS-485/9-bit mode and synchronous mode. USART supports an asynchronous smart card interface (ISO 7816-3).
  - Two SSP controllers with FIFO and multi-protocol capabilities.
  - I^2C-bus interface supporting the full I^2C-bus specification and Fast-mode Plus with a data rate of up to 1 Mbit/s with multiple address recognition and monitor mode.
- I/O Handler for hardware emulation of serial interfaces and DMA; supported through software libraries. (LPC11U37HFBD64/401 only.)
- Clock generation:
  - Crystal Oscillator with an operating range of 1 MHz to 25 MHz (system oscillator).
  - 12 MHz high-frequency Internal RC oscillator (IRC) that can optionally be used as a system clock.
  - Internal low-power, low-frequency WatchDog Oscillator (WDO) with programmable frequency output.
  - PLL allows CPU operation up to the maximum CPU rate with the system oscillator or the IRC as clock sources.
  - A second, dedicated PLL is provided for USB.

Table 1. Ordering information *…continued*

Type number	Package		
	Name	Description	Version
LPC11U36FBD64/401	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11U37FBD48/401	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U37HFBD64/401	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11U37FBD64/501	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

4.1 Ordering options

Table 2. Ordering options

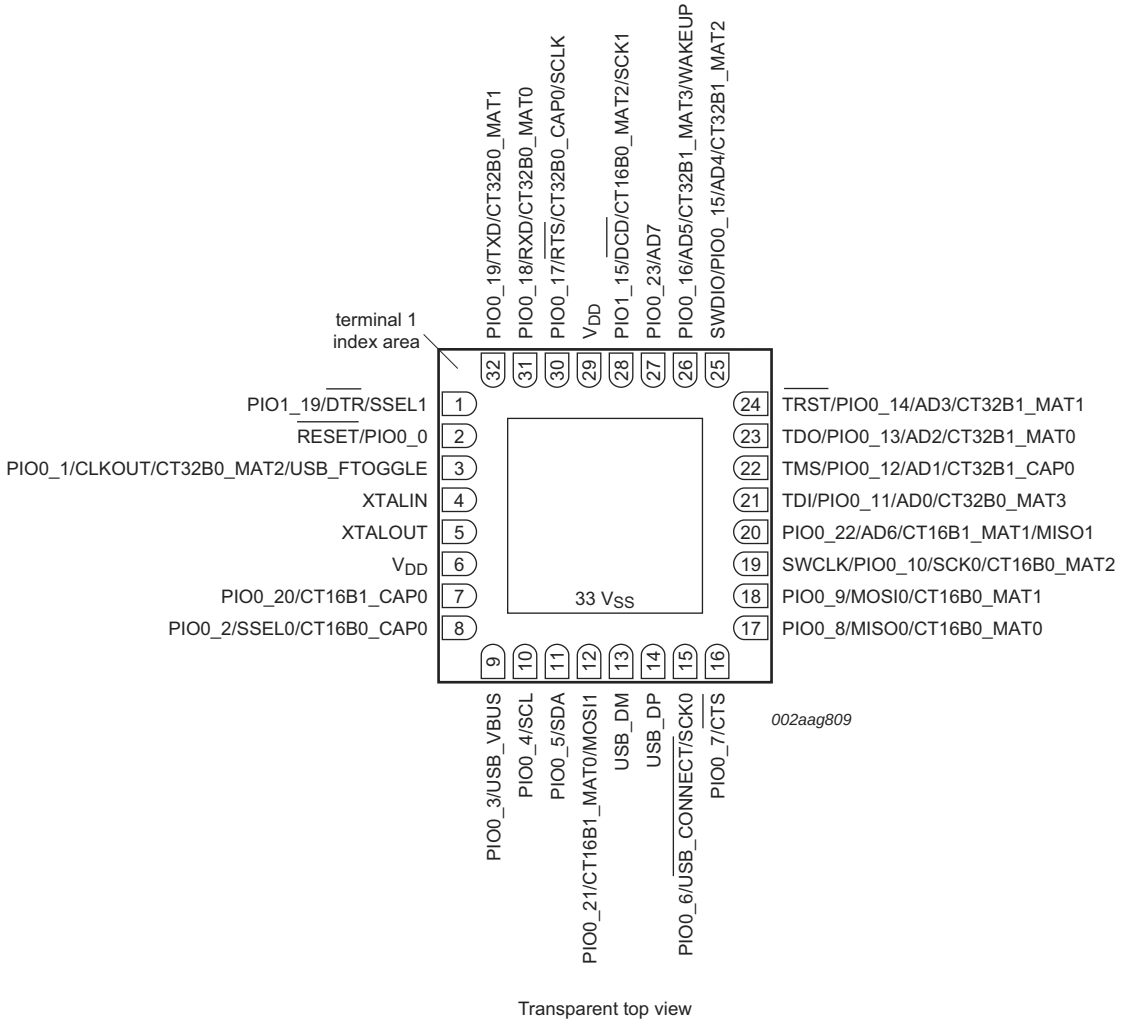
Type number	Flash in kB	EEPROM in kB	SRAM0 in kB	USB SRAM in kB	SRAM1 in kB	Total SRAM in kB[1]	I/O Handler	USART	I²C-bus FM+	SSP	USB device	ADC channels	GPIO pins
LPC11U34FHN33/311	40	4	8	-	-	8	no	1	1	2	1	8	26
LPC11U34FBD48/311	40	4	8	-	-	8	no	1	1	2	1	8	40
LPC11U34FHN33/421	48	4	8	2	-	10	no	1	1	2	1	8	26
LPC11U34FBD48/421	48	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U35FHN33/401	64	4	8	2	-	10	no	1	1	2	1	8	26
LPC11U35FBD48/401	64	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U35FBD64/401	64	4	8	2	-	10	no	1	1	2	1	8	54
LPC11U35FHI33/501	64	4	8	2	2[1]	12	no	1	1	2	1	8	26
LPC11U35FET48/501	64	4	8	2	2[1]	12	no	1	1	2	1	8	40
LPC11U36FBD48/401	96	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U36FBD64/401	96	4	8	2	-	10	no	1	1	2	1	8	54
LPC11U37FBD48/401	128	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U37HFBD64/401	128	4	8	2	2[2]	10	yes	1	1	2	1	8	54
LPC11U37FBD64/501	128	4	8	2	2[1]	12	no	1	1	2	1	8	54

[1] For general-purpose use.

[2] For I/O Handler use only.

6. Pinning information

6.1 Pinning



Transparent top view

For parts LPC11U34FHN33/311, LPC11U34FHN33/421, LPC11U35FHN33/401, LPC11U35FHI33/501

Fig 2. Pin configuration (HVQFN33)

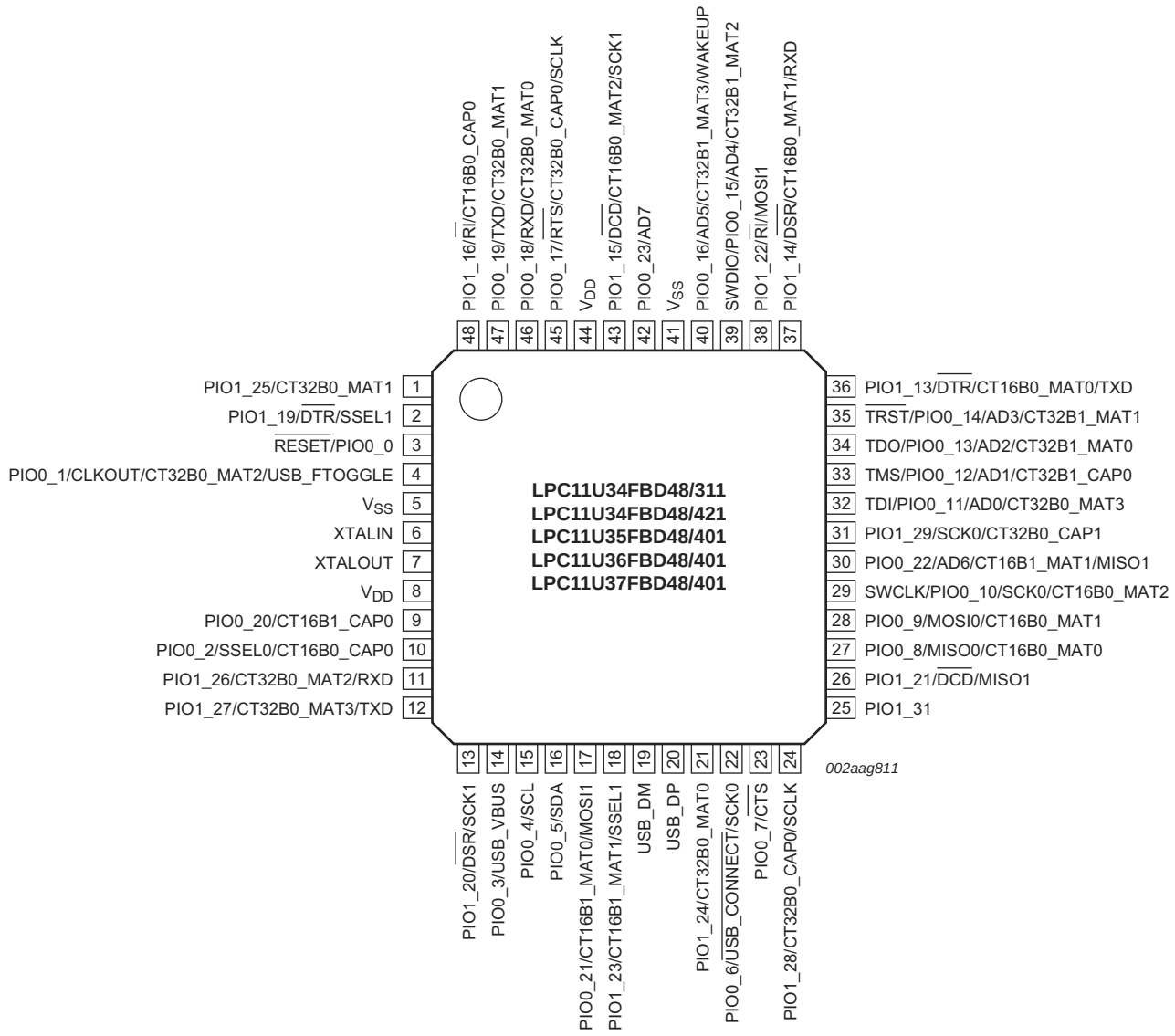


Fig 4. Pin configuration (LQFP48)

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
PIO0_17/$\overline{\text{RTS}}$/ CT32B0_CAP0/SCLK	30	A3	45	60 [3]	I; PU	I/O	**PIO0_17 —** General purpose digital input/output pin.
					-	O	**$\overline{\text{RTS}}$ —** Request To Send output for USART.
					-	I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
					-	I/O	**SCLK —** Serial clock input/output for USART in synchronous mode.
PIO0_18/RXD/ CT32B0_MAT0	31	B3	46	61 [3]	I; PU	I/O	**PIO0_18 —** General purpose digital input/output pin.
					-	I	**RXD —** Receiver input for USART. Used in UART ISP mode.
					-	O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO0_19/TXD/ CT32B0_MAT1	32	B2	47	62 [3]	I; PU	I/O	**PIO0_19 —** General purpose digital input/output pin.
					-	O	**TXD —** Transmitter output for USART. Used in UART ISP mode.
					-	O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO0_20/CT16B1_CAP0	7	F2	9	11 [3]	I; PU	I/O	**PIO0_20 —** General purpose digital input/output pin.
					-	I	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO0_21/CT16B1_MAT0/ MOSI1	12	G4	17	22 [3]	I; PU	I/O	**PIO0_21 —** General purpose digital input/output pin.
					-	O	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
					-	I/O	**MOSI1 —** Master Out Slave In for SSP1.
PIO0_22/AD6/ CT16B1_MAT1/MISO1	20	E8	30	40 [6]	I; PU	I/O	**PIO0_22 —** General purpose digital input/output pin.
					-	I	**AD6 —** A/D converter, input 6.
					-	O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
					-	I/O	**MISO1 —** Master In Slave Out for SSP1.
PIO0_23/AD7/IOH_9	27	A5	42	56 [6]	I; PU	I/O	**PIO0_23 —** General purpose digital input/output pin.
					-	I	**AD7 —** A/D converter, input 7.
					-	I/O	**IOH_9 —** I/O Handler input/output 9. (LPC11U37HFBD64/401 only.)
PIO1_0/CT32B1_MAT0/ IOH_10	-	-	-	1 [3]	I; PU	I/O	**PIO1_0 —** General purpose digital input/output pin.
					-	O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
					-	I/O	**IOH_10 —** I/O Handler input/output 10. (LPC11U37HFBD64/401 only.)
PIO1_1/CT32B1_MAT1/ IOH_11	-	-	-	17 [3]	I; PU	I/O	**PIO1_1 —** General purpose digital input/output pin.
					-	O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
					-	I/O	**IOH_11 —** I/O Handler input/output 11. (LPC11U37HFBD64/401 only.)
PIO1_2/CT32B1_MAT2/ IOH_12	-	-	-	34 [3]	I; PU	I/O	**PIO1_2 —** General purpose digital input/output pin.
					-	O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
					-	I/O	**IOH_12 —** I/O Handler input/output 12. (LPC11U37HFBD64/401 only.)

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
PIO1_3/CT32B1_MAT3/ IOH_13	-	-	-	50 [3]	I; PU	I/O	**PIO1_3 —** General purpose digital input/output pin.
					-	O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
					-	I/O	**IOH_13 —** I/O Handler input/output 13. (LPC11U37HFBD64/401 only.)
PIO1_4/CT32B1_CAP0/ IOH_14	-	-	-	16 [3]	I; PU	I/O	**PIO1_4 —** General purpose digital input/output pin.
					-	I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
					-	I/O	**IOH_14 —** I/O Handler input/output 14. (LPC11U37HFBD64/401 only.)
PIO1_5/CT32B1_CAP1 /IOH_15	-	H8	-	32 [3]	I; PU	I/O	**PIO1_5 —** General purpose digital input/output pin.
					-	I	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
					-	I/O	**IOH_15 —** I/O Handler input/output 15. (LPC11U37HFBD64/401 only.)
PIO1_6/IOH_16	-	-	-	64 [3]	I; PU	I/O	**PIO1_6 —** General purpose digital input/output pin.
					-	I/O	**IOH_16 —** I/O Handler input/output 16. (LPC11U37HFBD64/401 only.)
PIO1_7/IOH_17	-	-	-	6 [3]	I; PU	I/O	**PIO1_7 —** General purpose digital input/output pin.
					-	I/O	**IOH_17 —** I/O Handler input/output 17. (LPC11U37HFBD64/401 only.)
PIO1_8/IOH_18	-	-	-	39 [3]	I; PU	I/O	**PIO1_8 —** General purpose digital input/output pin.
					-	I/O	**IOH_18 —** I/O Handler input/output 18. (LPC11U37HFBD64/401 only.)
PIO1_9	-	-	-	55 [3]	I; PU	I/O	**PIO1_9 —** General purpose digital input/output pin.
PIO1_10	-	-	-	12 [3]	I; PU	I/O	**PIO1_10 —** General purpose digital input/output pin.
PIO1_11	-	-	-	43 [3]	I; PU	I/O	**PIO1_11 —** General purpose digital input/output pin.
PIO1_12	-	-	-	59 [3]	I; PU	I/O	**PIO1_12 —** General purpose digital input/output pin.
PIO1_13/$\overline{\text{DTR}}$/ CT16B0_MAT0/TXD	-	B8	36	47 [3]	I; PU	I/O	**PIO1_13 —** General purpose digital input/output pin.
					-	O	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for USART.
					-	O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
					-	O	**TXD —** Transmitter output for USART.
PIO1_14/$\overline{\text{DSR}}$/ CT16B0_MAT1/RXD	-	A8	37	49 [3]	I; PU	I/O	**PIO1_14 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{DSR}}$ —** Data Set Ready input for USART.
					-	O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					-	I	**RXD —** Receiver input for USART.
PIO1_15/$\overline{\text{DCD}}$/ CT16B0_MAT2/SCK1	28	A4	43	57 [3]	I; PU	I/O	**PIO1_15 —** General purpose digital input/output pin.
						I	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for USART.
					-	O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
					-	I/O	**SCK1 —** Serial clock for SSP1.

7.8.1 Features

- GPIO pins can be configured as input or output by software.
- All GPIO pins default to inputs with interrupt disabled at reset.
- Pin registers allow pins to be sensed and set individually.
- Up to eight GPIO pins can be selected from all GPIO pins to create an edge- or level-sensitive GPIO interrupt request.
- Any pin or pins in each port can trigger a port interrupt.

7.9 USB interface

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot-plugging and dynamic configuration of the devices. The host controller initiates all transactions.

The LPC11U3x USB interface consists of a full-speed device controller with on-chip PHY (PHYsical layer) for device functions.

Remark: Configure the LPC11U3x in default power mode with the power profiles before using the USB (see Section 7.18.5.1). Do not use the USB with the part in performance, efficiency, or low-power mode.

7.9.1 Full-speed USB device controller

The device controller enables 12 Mbit/s data exchange with a USB Host controller. It consists of a register interface, serial interface engine, and endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. If enabled, an interrupt is generated.

7.9.1.1 Features

- Dedicated USB PLL available.
- Fully compliant with *USB 2.0 specification (full speed)*.
- Supports 10 physical (5 logical) endpoints including one control endpoint.
- Single and double buffering supported.
- Each non-control endpoint supports bulk, interrupt, or isochronous endpoint types.
- Supports wake-up from Deep-sleep mode and Power-down mode on USB activity and remote wake-up.
- Supports SoftConnect.

7.10 I/O Handler (LPC11U37HFBD64/401 only)

The I/O Handler is a software library-supported hardware engine for emulating serial interfaces and off-loading the CPU for processing-intensive functions. The I/O Handler can emulate, among others, DMA and serial interfaces such as UART, I^2C, or I^2S with no or very low additional CPU load. The software libraries are available with supporting

application notes from NXP (see http://www.LPCware.com.) LPCXpresso, Keil, and IAR IDEs are supported. I/O Handler library code must be executed from the memory area 0x2000 0000 to 0x2000 07FF. This memory is not available for other use.

For application examples, see Section 11.8 “I/O Handler software library applications”. Each I/O Handler library uses a specific subset of I/O Handler pins and in some cases other pins and peripherals such as the counter/timers.

7.11 USART

The LPC11U3x contains one USART.

The USART includes full modem control, support for synchronous mode, and a smart card interface. The RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The USART uses a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.11.1 Features

- Maximum USART data bit rate of 3.125 Mbit/s.
- 16 byte receive and transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.
- Support for synchronous mode.
- Includes smart card interface.

7.12 SSP serial I/O controller

The SSP controllers operate on a SSP, 4-wire SSI, or Microwire bus. The controller can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bit to 16 bit of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.12.1 Features

- Maximum SSP speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode)
- Compatible with Motorola SPI (Serial Peripheral Interface), 4-wire Texas Instruments SSI (Serial Synchronous Interface), and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation

7.15 General purpose external event counter/timers

The LPC11U3x includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.15.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- Up to two capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event can also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler can be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.

7.16 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.17 Windowed WatchDog Timer (WWDT)

The purpose of the WWDT is to prevent an unresponsive system state. If software fails to update the watchdog within a programmable time window, the watchdog resets the microcontroller

7.17.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time before watchdog time-out.

Power-down mode reduces power consumption compared to Deep-sleep mode at the expense of longer wake-up times.

7.18.5.5 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip except for the WAKEUP pin. The LPC11U3x can wake up from Deep power-down mode via the WAKEUP pin.

The LPC11U3x can be prevented from entering Deep power-down mode by setting a lock bit in the PMU block. Locking out Deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. Pull the $\overline{\text{RESET}}$ pin HIGH to prevent it from floating while in Deep power-down mode.

7.18.6 System control

7.18.6.1 Reset

Reset has four sources on the LPC11U3x: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

In Deep power-down mode, an external pull-up resistor is required on the $\overline{\text{RESET}}$ pin.

7.18.6.2 Brownout detection

The LPC11U3x includes up to four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Four threshold levels can be selected to cause a forced reset of the chip.

7.18.6.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details, see the *LPC11Uxx user manual*.

There are three levels of Code Read Protection:

Table 5. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.0 V ≤ V_{DD} ≤ 3.6 V	4	-	-	mA
		1.8 V ≤ V_{DD} < 2.0 V	3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V [13]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD} [13]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V; 2.0 V ≤ V_{DD} ≤ 3.6 V	−15	−50	−85	μA
		1.8 V ≤ V_{DD} < 2.0 V	−10	−50	−85	μA
		V_{DD} < V_I < 5 V	0	0	0	μA
High-drive output pin (PIO0_7)						
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled	-	0.5	10	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled	-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function; V_{DD} ≥ 1.8 V [11] [12]	0	-	5.0	V
		V_{DD} = 0 V	0	-	3.6	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage		0.4	-	-	V
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = −20 mA	V_{DD} − 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OH} = −12 mA	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.0 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA	-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.0 V; I_{OL} = 3 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 2.5 V ≤ V_{DD} ≤ 3.6 V	20	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V	12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.0 V ≤ V_{DD} ≤ 3.6 V	4	-	-	mA
		1.8 V ≤ V_{DD} < 2.0 V	3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD} [13]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	10	50	150	μA

Table 5. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Pin capacitance						
C_{io}	input/output capacitance	pins configured for analog function	-	-	7.1	pF
		I^2C-bus pins (PIO0_4 and PIO0_5)	-	-	2.5	pF
		pins configured as GPIO	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] For USB operation 3.0 V ≤ V_{DD} ≤ 3.6 V. Guaranteed by design.

[3] IRC enabled; system oscillator disabled; system PLL disabled.

[4] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[5] BOD disabled.

[6] All peripherals disabled in the AHBCLKCTRL register. Peripheral clocks to USART, SSP0/1 disabled in the SYSCON block.

[7] USB_DP and USB_DM pulled LOW externally.

[8] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[9] IRC disabled; system oscillator enabled; system PLL enabled.

[10] WAKEUP pin pulled HIGH externally. An external pull-up resistor is required on the $\overline{\text{RESET}}$ pin for the Deep power-down mode.

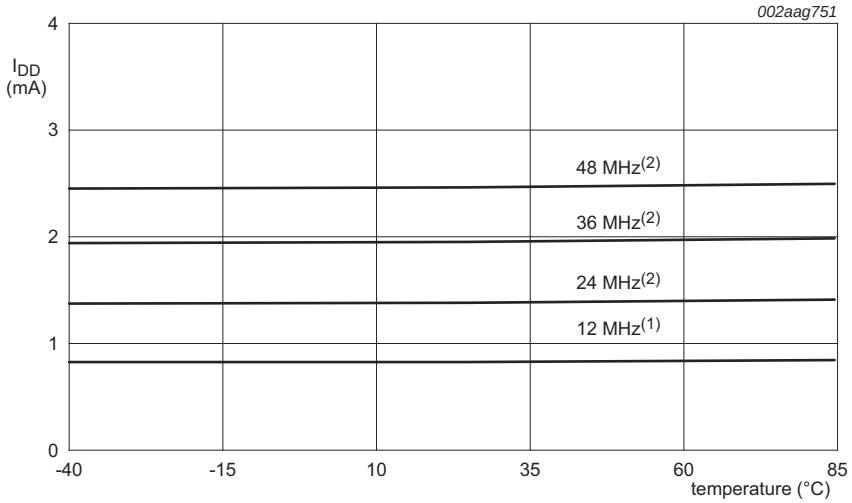
[11] Including voltage on outputs in 3-state mode.

[12] 3-state outputs go into 3-state mode in Deep power-down mode.

[13] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[14] To V_{SS}.

[15] Includes external resistors of 33 Ω ± 1 % on USB_DP and USB_DM.

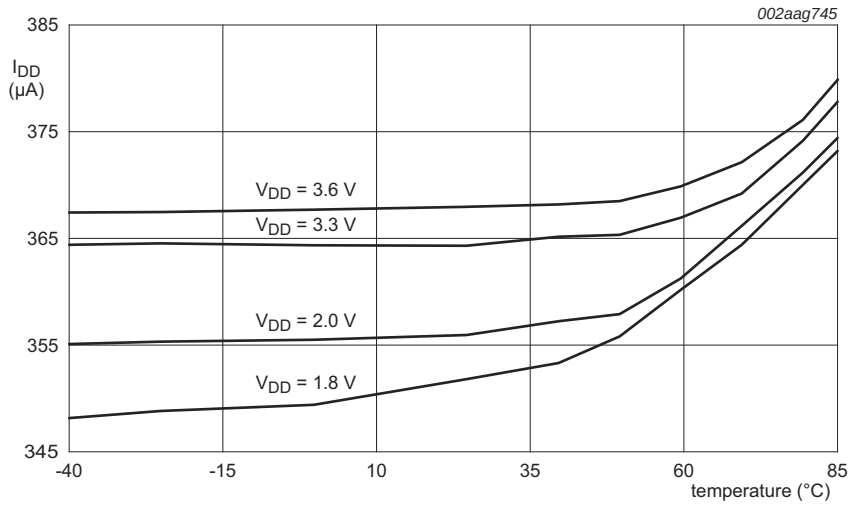


Conditions: V_{DD} = 3.3 V; Sleep mode entered from flash; internal pull-up resistors disabled; BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; low-current mode; USB_DP and USB_DM pulled LOW externally.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

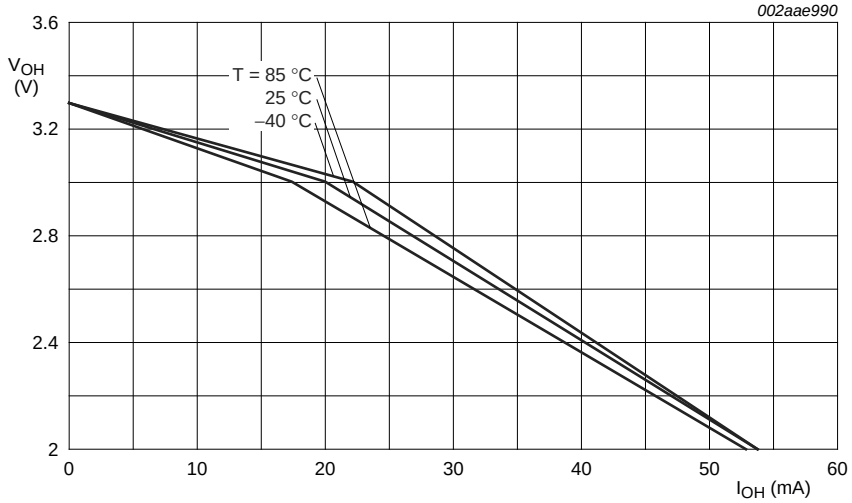
Fig 11. Typical supply current versus temperature in Sleep mode



Conditions: BOD disabled; all oscillators and analog blocks turned off in the PDSLEEPCFG register; USB_DP and USB_DM pulled LOW externally.

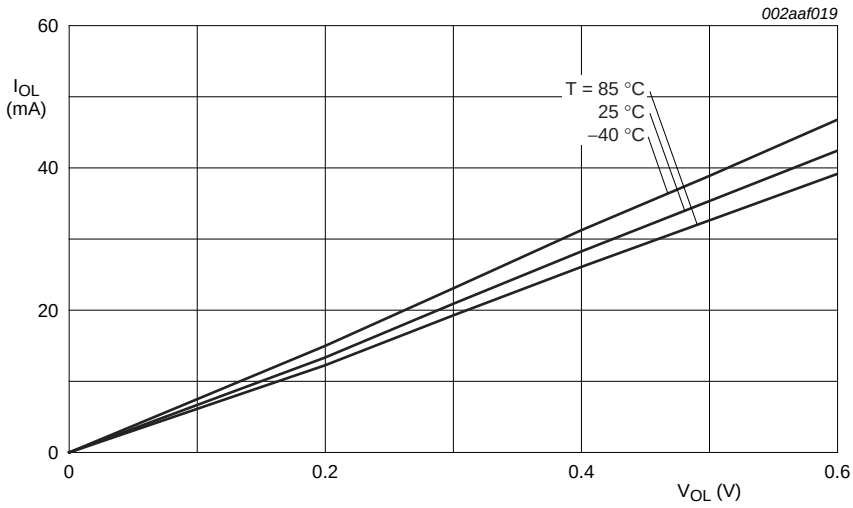
Fig 12. Typical supply current versus temperature in Deep-sleep mode

9.4 Electrical pin characteristics



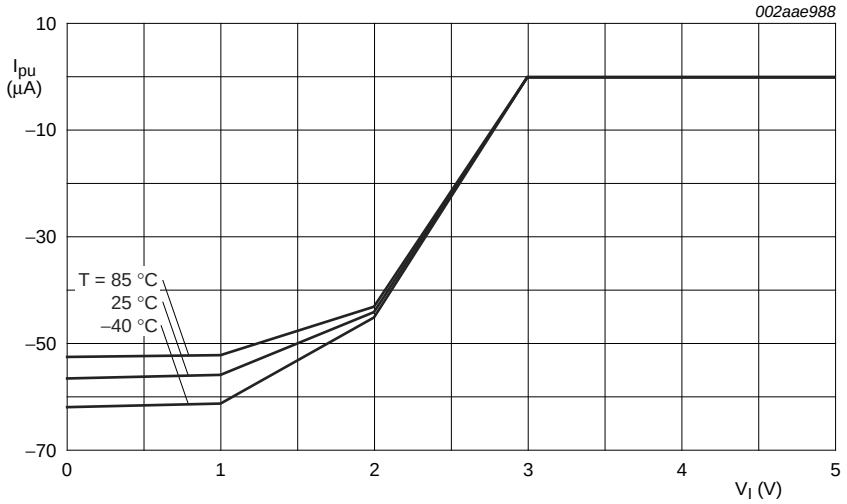
Conditions: V_{DD} = 3.3 V; on pin PIO0_7.

Fig 15. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}.



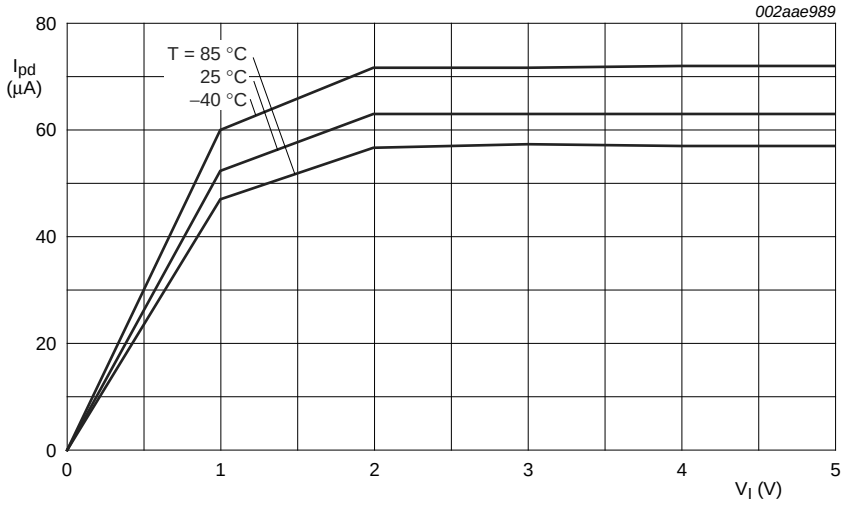
Conditions: V_{DD} = 3.3 V; on pins PIO0_4 and PIO0_5.

Fig 16. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 19. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 20. Typical pull-down current I_{pd} versus input voltage V_I

Under nominal operating condition V_{DD} = 3.3 V and with the maximum sampling frequency fs = 400 kHz, the parameters assume the following values:

C_{ia} = 1 pF (max)

R_{mux} = 2 kΩ (max)

R_{sw} = 1.3 kΩ (max)

C_{io} = 7.1 pF (max)

The effective input impedance with these parameters is R_{in} = 308 kΩ.

11.7 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 6:

- The ADC input trace must be short and as close as possible to the LPC11U3x chip.
- Shield The ADC input traces from fast switching digital signals and noisy power supply lines.
- The ADC and the digital core share the same power supply. Therefore, filter the power supply line adequately.
- To improve the ADC performance in a noisy environment, put the device in Sleep mode during the ADC conversion.

11.8 I/O Handler software library applications

The following sections provide application examples for the I/O Handler software library. All library examples make use of the I/O Handler hardware to extend the functionality of the part through software library calls. The libraries are available on http://www.LPCware.com.

11.8.1 I/O Handler I^2S

The I/O Handler software library provides functions to emulate an I^2S master transmit interface using the I/O Handler hardware block.

The emulated I^2S interface loops over a 1 kB buffer, transmitting the datawords according to the I^2S protocol. Interrupts are generated every time when the first 512 bytes have been transmitted and when the last 512 bytes have been transmitted. This allows the ARM core to load the free portion of the buffer with new data, thereby enabling streaming audio.

Two channels with 16-bit per channel are supported. The code size of the software library is 1 kB and code must be executed from the SRAM1 memory area reserved for the I/O Handler code.

11.8.2 I/O Handler UART

The I/O Handler UART library emulates one additional full-duplex UART. The emulated UART can be configured for 7 or 8 data bits, no parity, and 1 or 2 stop bits. The baud rate is configurable up to 115200 baud. The RXD signal is available on three I/O Handler pins (IOH_6, IOH_16, IOH_20), while TXD and CTS are available on all 21 I/O Handler pins.

The code size of the software library is about 1.2 kB and code must be executed from the SRAM1 memory area reserved for the I/O Handler code.

11.8.3 I/O Handler I²C

The I/O Handler I²C library allows to have an additional I²C-bus master. I²C read, I²C write and combined I²C read/write are supported. Data is automatically read from and written to user-defined buffers.

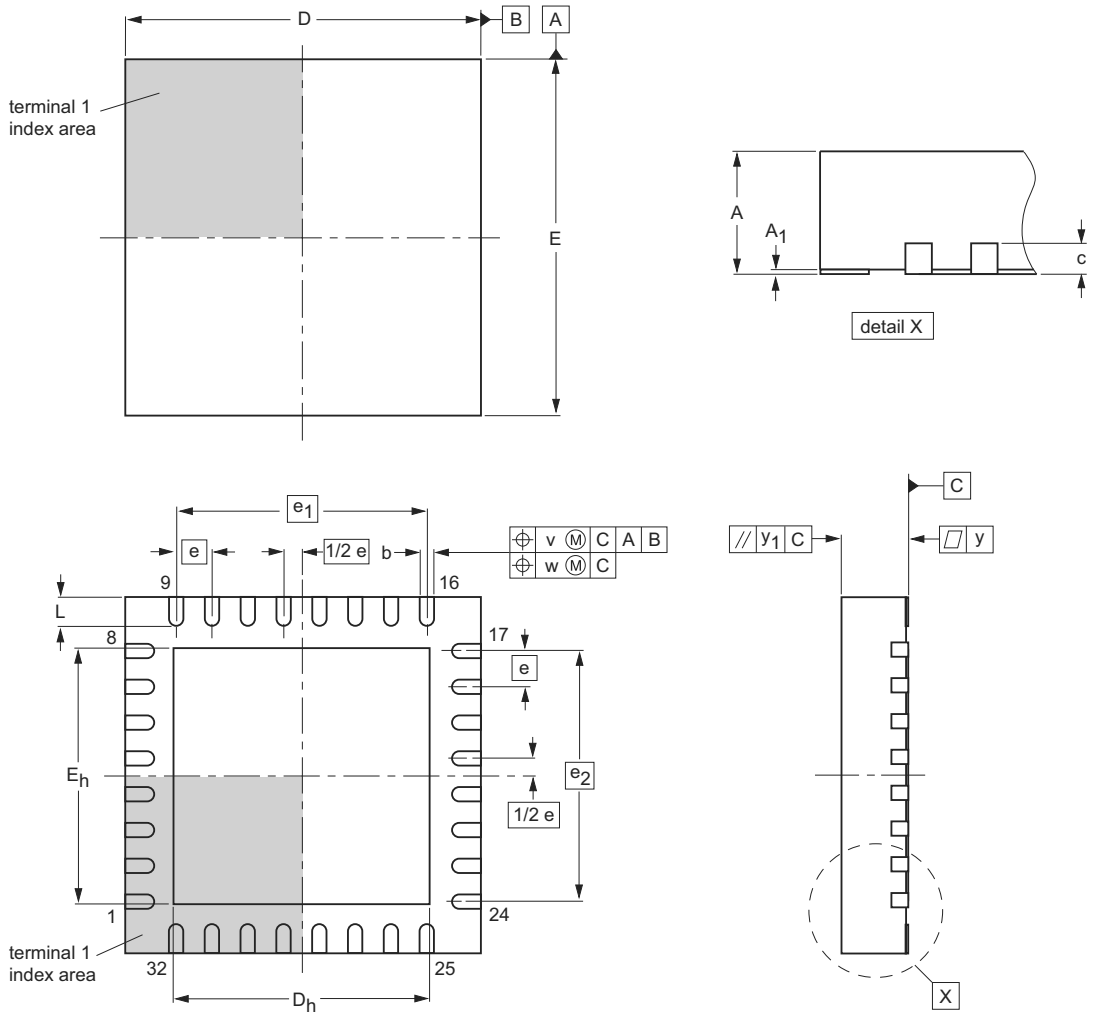
The I/O Handler I²C library combined with the on-chip I²C module allows to have two distinct I²C buses, allowing to separate low-speed from high-speed devices or bridging two I²C buses.

11.8.4 I/O Handler DMA

The I/O Handler DMA library offers DMA-like functionality. Four types of transfer are supported: memory to memory, memory to peripheral, peripheral to memory and peripheral to peripheral. Supported peripherals are USART, SSP0/1, ADC and GPIO. DMA transfers can be triggered by the source/target peripheral, software, counter/timer module CT16B1, or I/O Handler pin PIO1_6/IOH_16.

12. Package outline

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm



Dimensions (mm are the original dimensions)

Unit[1]		A[1]	A_1	b	c	D[1]	D_h	E[1]	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	0.85	0.05	0.30	0.2	5.1	3.75	5.1	3.75	0.5	3.5	3.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

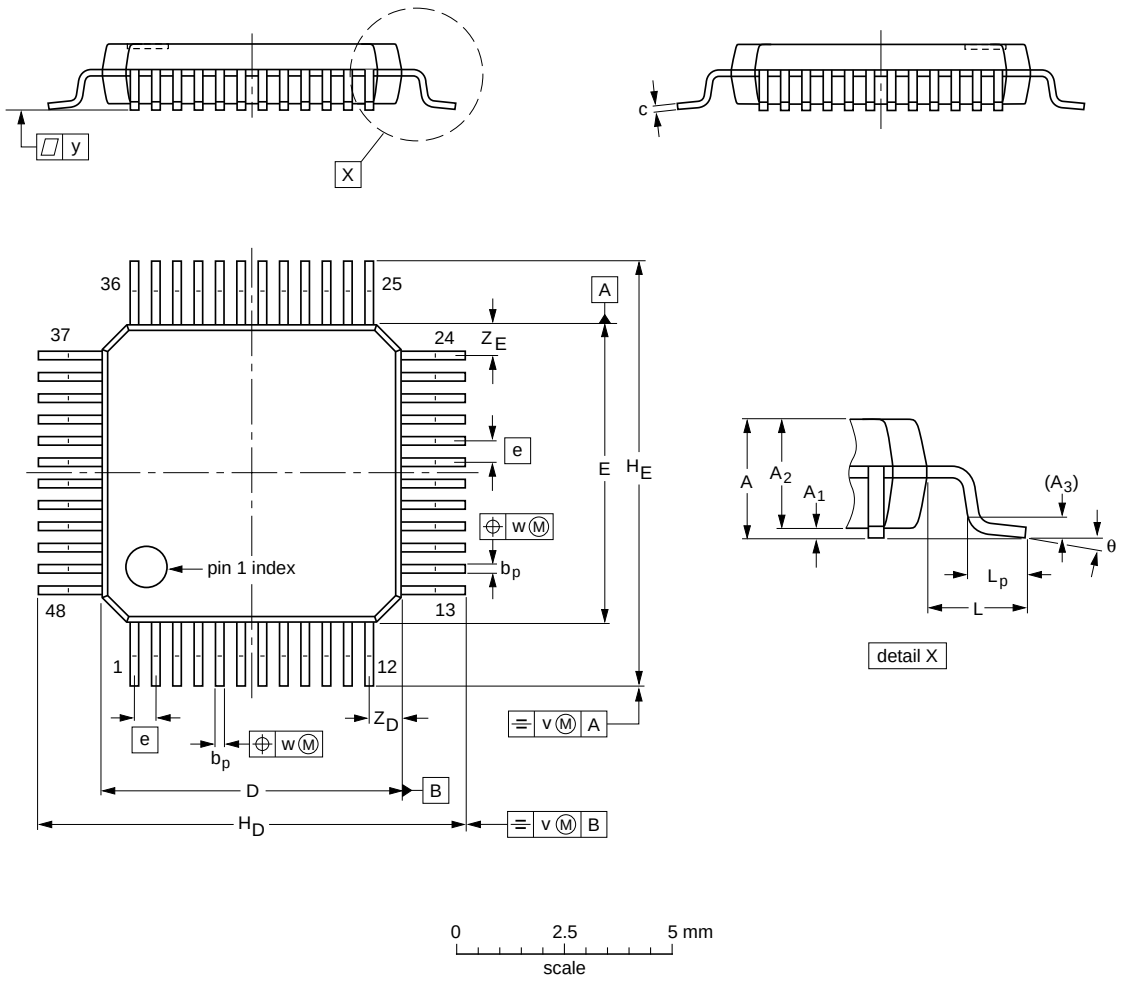
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33f_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		MO-220				~~11-10-11~~ 11-10-17

Fig 34. Package outline HVQFN33 (5 x 5 x 0.85 mm)

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 37. Package outline LQFP48 (SOT313-2)

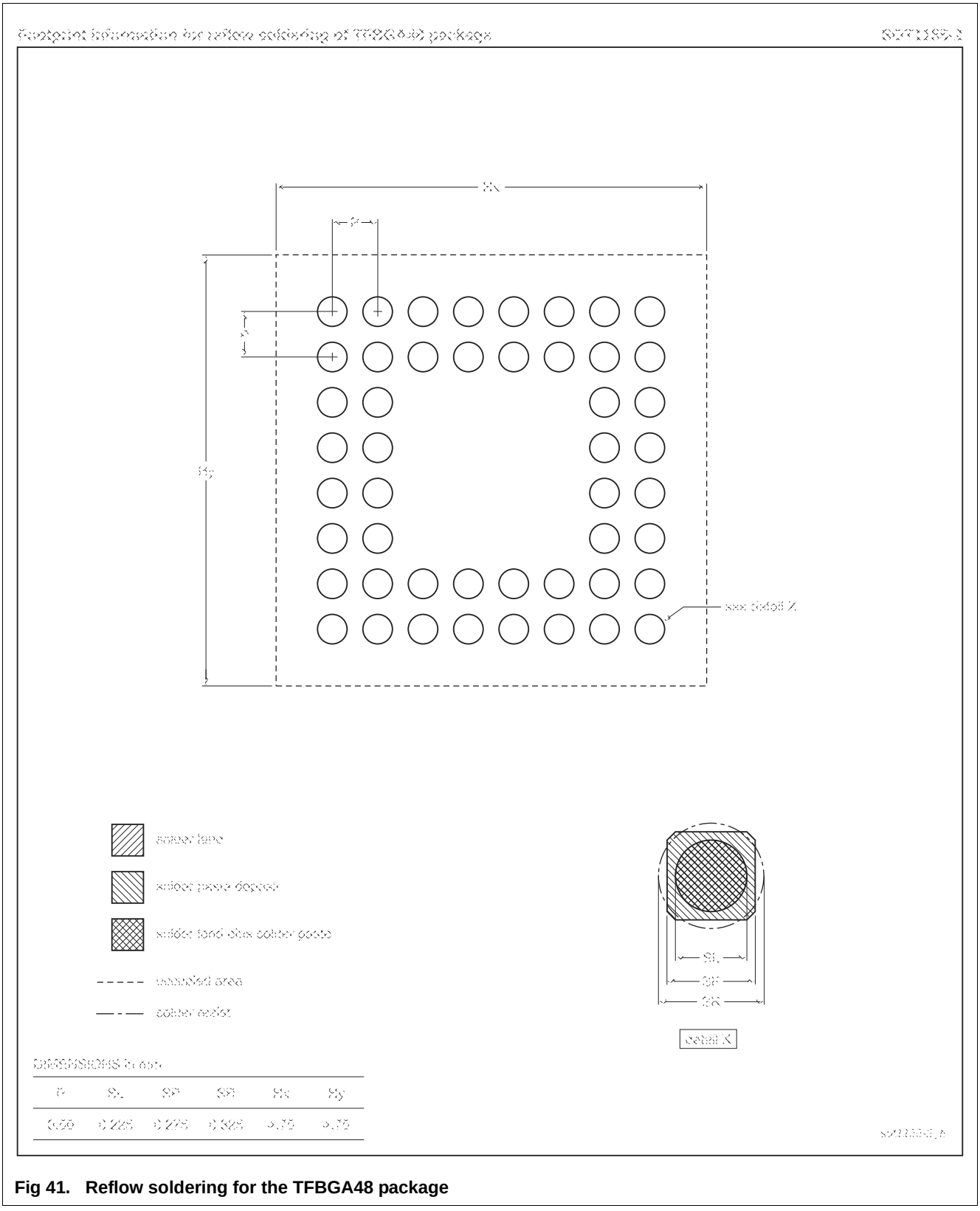


Fig 41. Reflow soldering for the TFBGA48 package