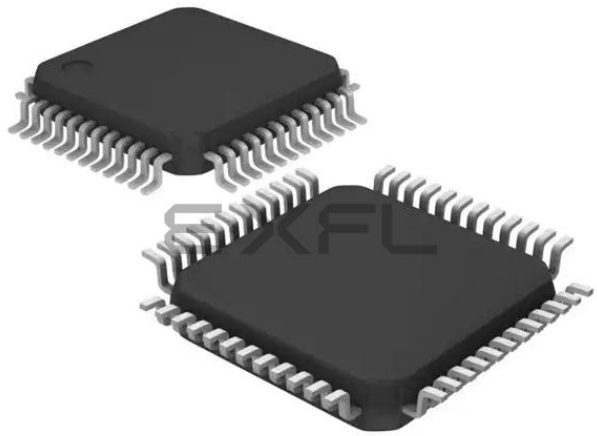

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SmartCard, SPI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	40
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11u37fbd48-401

- Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.

- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.
  - Power profiles residing in boot ROM provide optimized performance and minimized power consumption for any given application through one simple function call.
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Processor wake-up from Deep-sleep and Power-down modes via reset, selectable GPIO pins, watchdog interrupt, or USB port activity.
  - Processor wake-up from Deep power-down mode using one special function pin.
  - Power-On Reset (POR).
  - Brownout detect with up to four separate thresholds for interrupt and forced reset.
- Unique device serial number for identification.
- Single 3.3 V power supply (1.8 V to 3.6 V).
- Temperature range −40 °C to +85 °C.
- Available as LQFP64, LQFP48, TFBGA48, and HVQFN33 packages.

3. Applications

- Consumer peripherals
- Medical
- Industrial control
- Handheld scanners
- USB audio devices

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC11U34FHN33/311	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11U34FBD48/311	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U34FHN33/421	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11U34FBD48/421	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U35FHN33/401	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11U35FBD48/401	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U35FBD64/401	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11U35FHI33/501	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC11U35FET48/501	TFBGA48	plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 × 4.5 × 0.7 mm	SOT1155-2
LPC11U36FBD48/401	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

Table 1. Ordering information *…continued*

Type number	Package		
	Name	Description	Version
LPC11U36FBD64/401	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11U37FBD48/401	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U37HFBD64/401	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11U37FBD64/501	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

4.1 Ordering options

Table 2. Ordering options

Type number	Flash in kB	EEPROM in kB	SRAM0 in kB	USB SRAM in kB	SRAM1 in kB	Total SRAM in kB[1]	I/O Handler	USART	I²C-bus FM+	SSP	USB device	ADC channels	GPIO pins
LPC11U34FHN33/311	40	4	8	-	-	8	no	1	1	2	1	8	26
LPC11U34FBD48/311	40	4	8	-	-	8	no	1	1	2	1	8	40
LPC11U34FHN33/421	48	4	8	2	-	10	no	1	1	2	1	8	26
LPC11U34FBD48/421	48	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U35FHN33/401	64	4	8	2	-	10	no	1	1	2	1	8	26
LPC11U35FBD48/401	64	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U35FBD64/401	64	4	8	2	-	10	no	1	1	2	1	8	54
LPC11U35FHI33/501	64	4	8	2	2[1]	12	no	1	1	2	1	8	26
LPC11U35FET48/501	64	4	8	2	2[1]	12	no	1	1	2	1	8	40
LPC11U36FBD48/401	96	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U36FBD64/401	96	4	8	2	-	10	no	1	1	2	1	8	54
LPC11U37FBD48/401	128	4	8	2	-	10	no	1	1	2	1	8	40
LPC11U37HFBD64/401	128	4	8	2	2[2]	10	yes	1	1	2	1	8	54
LPC11U37FBD64/501	128	4	8	2	2[1]	12	no	1	1	2	1	8	54

[1] For general-purpose use.

[2] For I/O Handler use only.

6.2 Pin description

Table 3 shows all pins and their assigned digital or analog functions in order of the GPIO port number. The default function after reset is listed first. All port pins have internal pull-up resistors enabled after reset except for the true open-drain pins PIO0_4 and PIO0_5.

Every port pin has a corresponding IOCON register for programming the digital or analog function, the pull-up/pull-down configuration, the repeater, and the open-drain modes.

The USART, counter/timer, and SSP functions are available on more than one port pin.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
RESET/PIO0_0	2	C1	3	4 [2]	I; PU	I	**RESET —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode. In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed and Deep power-down mode is not used.
					-	I/O	**PIO0_0 —** General purpose digital input/output pin.
PIO0_1/CLKOUT/ CT32B0_MAT2/ USB_FTOGGLE	3	C2	4	5 [3]	I; PU	I/O	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler or the USB device enumeration.
					-	O	**CLKOUT —** Clockout pin.
					-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					-	O	**USB_FTOGGLE —** USB 1 ms Start-of-Frame signal.
PIO0_2/SSEL0/ CT16B0_CAP0/IOH_0	8	F1	10	13 [3]	I; PU	I/O	**PIO0_2 —** General purpose digital input/output pin.
					-	I/O	**SSEL0 —** Slave select for SSP0.
					-	I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
					-	I/O	**IOH_0 —** I/O Handler input/output 0. LPC11U37HFBD64/401 only.
PIO0_3/USB_VBUS/ IOH_1	9	H2	14	19 [3]	I; PU	I/O	**PIO0_3 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler. A HIGH level during reset starts the USB device enumeration.
					-	I	**USB_VBUS —** Monitors the presence of USB bus power.
					-	I/O	**IOH_1 —** I/O Handler input/output 1. LPC11U37HFBD64/401 only.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
PIO0_4/SCL/IOH_2	10	G3	15	20 [4]	I; IA	I/O	**PIO0_4 —** General purpose digital input/output pin (open-drain).
					-	I/O	**SCL —** I^2C-bus clock input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
					-	I/O	**IOH_2 —** I/O Handler input/output 2. LPC11U37HFBD64/401 only.
PIO0_5/SDA/IOH_3	11	H3	16	21 [4]	I; IA	I/O	**PIO0_5 —** General purpose digital input/output pin (open-drain).
					-	I/O	**SDA —** I^2C-bus data input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
					-	I/O	**IOH_3 —** I/O Handler input/output 3. LPC11U37HFBD64/401 only.
PIO0_6/$\overline{\text{USB\_CONNECT}}$/SCK0/IOH_4	15	H6	22	29 [3]	I; PU	I/O	**PIO0_6 —** General purpose digital input/output pin.
					-	O	**$\overline{\text{USB\_CONNECT}}$ —** Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
					-	I/O	**SCK0 —** Serial clock for SSP0.
					-	I/O	**IOH_4 —** I/O Handler input/output 4. LPC11U37HFBD64/401 only.
PIO0_7/$\overline{\text{CTS}}$/IOH_5	16	G7	23	30 [5]	I; PU	I/O	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
					-	I	**$\overline{\text{CTS}}$ —** Clear To Send input for USART.
					-	I/O	**IOH_5 —** I/O Handler input/output 5. (LPC11U37HFBD64/401 only.)
PIO0_8/MISO0/CT16B0_MAT0/R/IOH_6	17	F8	27	36 [3]	I; PU	I/O	**PIO0_8 —** General purpose digital input/output pin.
					-	I/O	**MISO0 —** Master In Slave Out for SSP0.
					-	O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
					-	-	Reserved.
					-	I/O	**IOH_6 —** I/O Handler input/output 6. (LPC11U37HFBD64/401 only.)
PIO0_9/MOSI0/CT16B0_MAT1/R/IOH_7	18	F7	28	37 [3]	I; PU	I/O	**PIO0_9 —** General purpose digital input/output pin.
					-	I/O	**MOSI0 —** Master Out Slave In for SSP0.
					-	O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					-	-	Reserved.
					-	I/O	**IOH_7 —** I/O Handler input/output 7. (LPC11U37HFBD64/401 only.)

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
PIO0_17/$\overline{\text{RTS}}$/ CT32B0_CAP0/SCLK	30	A3	45	60 [3]	I; PU	I/O	**PIO0_17 —** General purpose digital input/output pin.
					-	O	**$\overline{\text{RTS}}$ —** Request To Send output for USART.
					-	I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
					-	I/O	**SCLK —** Serial clock input/output for USART in synchronous mode.
PIO0_18/RXD/ CT32B0_MAT0	31	B3	46	61 [3]	I; PU	I/O	**PIO0_18 —** General purpose digital input/output pin.
					-	I	**RXD —** Receiver input for USART. Used in UART ISP mode.
					-	O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO0_19/TXD/ CT32B0_MAT1	32	B2	47	62 [3]	I; PU	I/O	**PIO0_19 —** General purpose digital input/output pin.
					-	O	**TXD —** Transmitter output for USART. Used in UART ISP mode.
					-	O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO0_20/CT16B1_CAP0	7	F2	9	11 [3]	I; PU	I/O	**PIO0_20 —** General purpose digital input/output pin.
					-	I	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO0_21/CT16B1_MAT0/ MOSI1	12	G4	17	22 [3]	I; PU	I/O	**PIO0_21 —** General purpose digital input/output pin.
					-	O	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
					-	I/O	**MOSI1 —** Master Out Slave In for SSP1.
PIO0_22/AD6/ CT16B1_MAT1/MISO1	20	E8	30	40 [6]	I; PU	I/O	**PIO0_22 —** General purpose digital input/output pin.
					-	I	**AD6 —** A/D converter, input 6.
					-	O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
					-	I/O	**MISO1 —** Master In Slave Out for SSP1.
PIO0_23/AD7/IOH_9	27	A5	42	56 [6]	I; PU	I/O	**PIO0_23 —** General purpose digital input/output pin.
					-	I	**AD7 —** A/D converter, input 7.
					-	I/O	**IOH_9 —** I/O Handler input/output 9. (LPC11U37HFBD64/401 only.)
PIO1_0/CT32B1_MAT0/ IOH_10	-	-	-	1 [3]	I; PU	I/O	**PIO1_0 —** General purpose digital input/output pin.
					-	O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
					-	I/O	**IOH_10 —** I/O Handler input/output 10. (LPC11U37HFBD64/401 only.)
PIO1_1/CT32B1_MAT1/ IOH_11	-	-	-	17 [3]	I; PU	I/O	**PIO1_1 —** General purpose digital input/output pin.
					-	O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
					-	I/O	**IOH_11 —** I/O Handler input/output 11. (LPC11U37HFBD64/401 only.)
PIO1_2/CT32B1_MAT2/ IOH_12	-	-	-	34 [3]	I; PU	I/O	**PIO1_2 —** General purpose digital input/output pin.
					-	O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
					-	I/O	**IOH_12 —** I/O Handler input/output 12. (LPC11U37HFBD64/401 only.)

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
PIO1_3/CT32B1_MAT3/ IOH_13	-	-	-	50 [3]	I; PU	I/O	**PIO1_3 —** General purpose digital input/output pin.
					-	O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
					-	I/O	**IOH_13 —** I/O Handler input/output 13. (LPC11U37HFBD64/401 only.)
PIO1_4/CT32B1_CAP0/ IOH_14	-	-	-	16 [3]	I; PU	I/O	**PIO1_4 —** General purpose digital input/output pin.
					-	I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
					-	I/O	**IOH_14 —** I/O Handler input/output 14. (LPC11U37HFBD64/401 only.)
PIO1_5/CT32B1_CAP1 /IOH_15	-	H8	-	32 [3]	I; PU	I/O	**PIO1_5 —** General purpose digital input/output pin.
					-	I	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
					-	I/O	**IOH_15 —** I/O Handler input/output 15. (LPC11U37HFBD64/401 only.)
PIO1_6/IOH_16	-	-	-	64 [3]	I; PU	I/O	**PIO1_6 —** General purpose digital input/output pin.
					-	I/O	**IOH_16 —** I/O Handler input/output 16. (LPC11U37HFBD64/401 only.)
PIO1_7/IOH_17	-	-	-	6 [3]	I; PU	I/O	**PIO1_7 —** General purpose digital input/output pin.
					-	I/O	**IOH_17 —** I/O Handler input/output 17. (LPC11U37HFBD64/401 only.)
PIO1_8/IOH_18	-	-	-	39 [3]	I; PU	I/O	**PIO1_8 —** General purpose digital input/output pin.
					-	I/O	**IOH_18 —** I/O Handler input/output 18. (LPC11U37HFBD64/401 only.)
PIO1_9	-	-	-	55 [3]	I; PU	I/O	**PIO1_9 —** General purpose digital input/output pin.
PIO1_10	-	-	-	12 [3]	I; PU	I/O	**PIO1_10 —** General purpose digital input/output pin.
PIO1_11	-	-	-	43 [3]	I; PU	I/O	**PIO1_11 —** General purpose digital input/output pin.
PIO1_12	-	-	-	59 [3]	I; PU	I/O	**PIO1_12 —** General purpose digital input/output pin.
PIO1_13/$\overline{\text{DTR}}$/ CT16B0_MAT0/TXD	-	B8	36	47 [3]	I; PU	I/O	**PIO1_13 —** General purpose digital input/output pin.
					-	O	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for USART.
					-	O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
					-	O	**TXD —** Transmitter output for USART.
PIO1_14/$\overline{\text{DSR}}$/ CT16B0_MAT1/RXD	-	A8	37	49 [3]	I; PU	I/O	**PIO1_14 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{DSR}}$ —** Data Set Ready input for USART.
					-	O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					-	I	**RXD —** Receiver input for USART.
PIO1_15/$\overline{\text{DCD}}$/ CT16B0_MAT2/SCK1	28	A4	43	57 [3]	I; PU	I/O	**PIO1_15 —** General purpose digital input/output pin.
						I	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for USART.
					-	O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
					-	I/O	**SCK1 —** Serial clock for SSP1.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
PIO1_16/$\overline{\text{RI}}$/ CT16B0_CAP0	-	A2	48	63 [3]	I; PU	I/O	**PIO1_16 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{RI}}$ —** Ring Indicator input for USART.
					-	I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO1_17/CT16B0_CAP1/ RXD	-	-	-	23 [3]	I; PU	I/O	**PIO1_17 —** General purpose digital input/output pin.
					-	I	**CT16B0_CAP1 —** Capture input 1 for 16-bit timer 0.
					-	I	**RXD —** Receiver input for USART.
PIO1_18/CT16B1_CAP1/ TXD	-	-	-	28 [3]	I; PU	I/O	**PIO1_18 —** General purpose digital input/output pin.
					-	I	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
					-	O	**TXD —** Transmitter output for USART.
PIO1_19/$\overline{\text{DTR}}$/SSEL1	1	B1	2	3 [3]	I; PU	I/O	**PIO1_19 —** General purpose digital input/output pin.
					-	O	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for USART.
					-	I/O	**SSEL1 —** Slave select for SSP1.
PIO1_20/$\overline{\text{DSR}}$/SCK1	-	H1	13	18 [3]	I; PU	I/O	**PIO1_20 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{DSR}}$ —** Data Set Ready input for USART.
					-	I/O	**SCK1 —** Serial clock for SSP1.
PIO1_21/$\overline{\text{DCD}}$/MISO1	-	G8	26	35 [3]	I; PU	I/O	**PIO1_21 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for USART.
					-	I/O	**MISO1 —** Master In Slave Out for SSP1.
PIO1_22/$\overline{\text{RI}}$/MOSI1	-	A7	38	51 [3]	I; PU	I/O	**PIO1_22 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{RI}}$ —** Ring Indicator input for USART.
					-	I/O	**MOSI1 —** Master Out Slave In for SSP1.
PIO1_23/CT16B1_MAT1/ SSEL1	-	H4	18	24 [3]	I; PU	I/O	**PIO1_23 —** General purpose digital input/output pin.
					-	O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
					-	I/O	**SSEL1 —** Slave select for SSP1.
PIO1_24/CT32B0_MAT0	-	G6	21	27 [3]	I; PU	I/O	**PIO1_24 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO1_25/CT32B0_MAT1	-	A1	1	2 [3]	I; PU	I/O	**PIO1_25 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_26/CT32B0_MAT2/ RXD/IOH_19	-	G2	11	14 [3]	I; PU	I/O	**PIO1_26 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					-	I	**RXD —** Receiver input for USART.
					-	I/O	**IOH_19 —** I/O Handler input/output 19. (LPC11U37HFBD64/401 only.)
PIO1_27/CT32B0_MAT3/ TXD/IOH_20	-	G1	12	15 [3]	I; PU	I/O	**PIO1_27 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
					-	O	**TXD —** Transmitter output for USART.
					-	I/O	**IOH_20 —** I/O Handler input/output 20. (LPC11U37HFBD64/401 only.)

Table 3. Pin description

Symbol	Pin HVQFN33	Pin TFBGA48	Pin LQFP48	Pin LQFP64	Reset state [1]	Type	Description
PIO1_28/CT32B0_CAP0/ SCLK	-	H7	24	31 [3]	I; PU	I/O	**PIO1_28 —** General purpose digital input/output pin.
					-	I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
					-	I/O	**SCLK —** Serial clock input/output for USART in synchronous mode.
PIO1_29/SCK0/ CT32B0_CAP1	-	D7	31	41 [3]	I; PU	I/O	**PIO1_29 —** General purpose digital input/output pin.
					-	I/O	**SCK0 —** Serial clock for SSP0.
					-	I	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0.
PIO1_31	-	-	25	- [3]	I; PU	I/O	**PIO1_31 —** General purpose digital input/output pin.
USB_DM	13	G5	19	25 [7]	F	-	**USB_DM —** USB bidirectional D− line.
USB_DP	14	H5	20	26 [7]	F	-	**USB_DP —** USB bidirectional D+ line.
XTALIN	4	D1	6	8 [8]	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	5	E1	7	9 [8]	-	-	Output from the oscillator amplifier.
V_{DD}	6; 29	B4; E2	8; 44	10; 33; 48; 58	-	-	Supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
V_{SS}	33	B5; D2	5; 41	7; 54	-	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; If the pins are not used, tie floating pins to ground or power to minimize power consumption.

[2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See Figure 32 for the reset pad configuration.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 31).

[4] I^2C-bus pin compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 31); includes high-current output driver.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 31); includes digital input glitch filter.

[7] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[8] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). Leave XTALOUT floating.

- Four programmable interrupt priority levels, with hardware priority level masking.
- Software interrupt generation.

7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

7.7 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Connect peripherals to the appropriate pins before activating the peripheral and before enabling any related interrupt. Activity of any enabled peripheral function that is not mapped to a related pin is treated as undefined.

7.7.1 Features

- Programmable pull-up, pull-down, or repeater mode.
- All GPIO pins (except PIO0_4 and PIO0_5) are pulled up to 3.3 V (V_{DD} = 3.3 V) if their pull-up resistor is enabled.
- Programmable pseudo open-drain mode.
- Programmable 10 ns glitch filter on pins PIO0_22, PIO0_23, and PIO0_11 to PIO0_16. The glitch filter is turned on by default.
- Programmable hysteresis.
- Programmable input inverter.

7.8 General-Purpose Input/Output GPIO

The GPIO registers control device pin functions that are not connected to a specific peripheral function. Pins can be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC11U3x use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Any GPIO pin providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

The GPIO block consists of three parts:

1. The GPIO ports.
2. The GPIO pin interrupt block to control eight GPIO pins selected as pin interrupts.
3. Two GPIO group interrupt blocks to control two combined interrupts from all GPIO pins.

7.8.1 Features

- GPIO pins can be configured as input or output by software.
- All GPIO pins default to inputs with interrupt disabled at reset.
- Pin registers allow pins to be sensed and set individually.
- Up to eight GPIO pins can be selected from all GPIO pins to create an edge- or level-sensitive GPIO interrupt request.
- Any pin or pins in each port can trigger a port interrupt.

7.9 USB interface

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot-plugging and dynamic configuration of the devices. The host controller initiates all transactions.

The LPC11U3x USB interface consists of a full-speed device controller with on-chip PHY (PHYsical layer) for device functions.

Remark: Configure the LPC11U3x in default power mode with the power profiles before using the USB (see Section 7.18.5.1). Do not use the USB with the part in performance, efficiency, or low-power mode.

7.9.1 Full-speed USB device controller

The device controller enables 12 Mbit/s data exchange with a USB Host controller. It consists of a register interface, serial interface engine, and endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. If enabled, an interrupt is generated.

7.9.1.1 Features

- Dedicated USB PLL available.
- Fully compliant with *USB 2.0 specification (full speed)*.
- Supports 10 physical (5 logical) endpoints including one control endpoint.
- Single and double buffering supported.
- Each non-control endpoint supports bulk, interrupt, or isochronous endpoint types.
- Supports wake-up from Deep-sleep mode and Power-down mode on USB activity and remote wake-up.
- Supports SoftConnect.

7.10 I/O Handler (LPC11U37HFBD64/401 only)

The I/O Handler is a software library-supported hardware engine for emulating serial interfaces and off-loading the CPU for processing-intensive functions. The I/O Handler can emulate, among others, DMA and serial interfaces such as UART, I^2C, or I^2S with no or very low additional CPU load. The software libraries are available with supporting

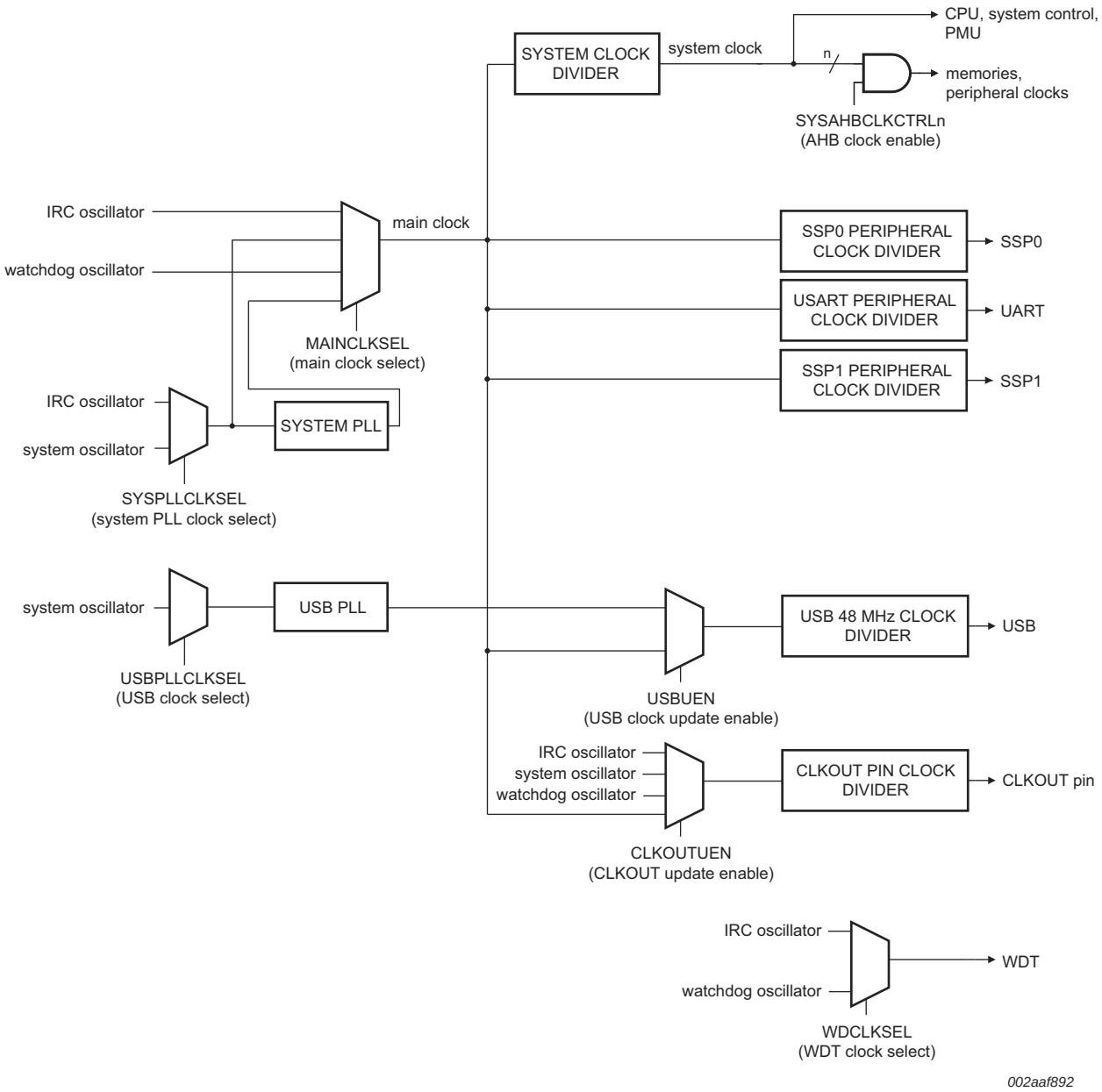


Fig 7. LPC11U3x clocking generation block diagram

7.18.1.1 Internal RC oscillator

The IRC can be used as the clock source for the WDT, and/or as the clock that drives the system PLL and then the CPU. The nominal IRC frequency is 12 MHz.

Upon power-up, any chip reset, or wake-up from Deep power-down mode, the LPC11U3x use the IRC as the clock source. Software can later switch to one of the other available clock sources.

consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.18.5.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC11U3x for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

Remark: When using the USB, configure the LPC11U3x in Default mode.

7.18.5.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and can generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, by memory systems and related controllers, and by internal buses.

7.18.5.3 Deep-sleep mode

In Deep-sleep mode, the LPC11U3x is in Sleep-mode and all peripheral clocks and all clock sources are off except for the IRC. The IRC output is disabled unless the IRC is selected as input to the watchdog timer. In addition all analog blocks are shut down and the flash is in stand-by mode. In Deep-sleep mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC11U3x can wake up from Deep-sleep mode via reset, selected GPIO pins, a watchdog timer interrupt, or an interrupt generating USB port activity.

Deep-sleep mode saves power and allows for short wake-up times.

7.18.5.4 Power-down mode

In Power-down mode, the LPC11U3x is in Sleep-mode and all peripheral clocks and all clock sources are off except for watchdog oscillator if selected. In addition all analog blocks and the flash are shut down. In Power-down mode, the application can keep the BOD circuit running for BOD protection.

The LPC11U3x can wake up from Power-down mode via reset, selected GPIO pins, a watchdog timer interrupt, or an interrupt generating USB port activity.

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details, see the *LPC11Uxx user manual*.

7.18.6.4 APB interface

The APB peripherals are located on one APB bus.

7.18.6.5 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the ROM.

7.18.6.6 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs.

7.19 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0 is configured to support up to four breakpoints and two watch points.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC11U3x is in reset.

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

Table 5. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.0 V ≤ V_{DD} ≤ 3.6 V	4	-	-	mA
		1.8 V ≤ V_{DD} < 2.0 V	3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V [13]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD} [13]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V; 2.0 V ≤ V_{DD} ≤ 3.6 V	−15	−50	−85	μA
		1.8 V ≤ V_{DD} < 2.0 V	−10	−50	−85	μA
		V_{DD} < V_I < 5 V	0	0	0	μA
High-drive output pin (PIO0_7)						
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled	-	0.5	10	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled	-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function; V_{DD} ≥ 1.8 V [11] [12]	0	-	5.0	V
		V_{DD} = 0 V	0	-	3.6	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage		0.4	-	-	V
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = −20 mA	V_{DD} − 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OH} = −12 mA	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.0 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA	-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.0 V; I_{OL} = 3 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 2.5 V ≤ V_{DD} ≤ 3.6 V	20	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V	12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.0 V ≤ V_{DD} ≤ 3.6 V	4	-	-	mA
		1.8 V ≤ V_{DD} < 2.0 V	3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD} [13]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	10	50	150	μA

Table 6. ADC static characteristics

T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz, V_{DD} = 2.5 V to 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DD}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity	[3]	-	-	±1.5	LSB
E_O	offset error	[4]	-	-	±3.5	LSB
E_G	gain error	[5]	-	-	0.6	%
E_T	absolute error	[6]	-	-	±4	LSB
R_{vsi}	voltage source interface resistance		-	-	40	kΩ
R_i	input resistance	[7][8]	-	-	2.5	MΩ

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 8.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 8.

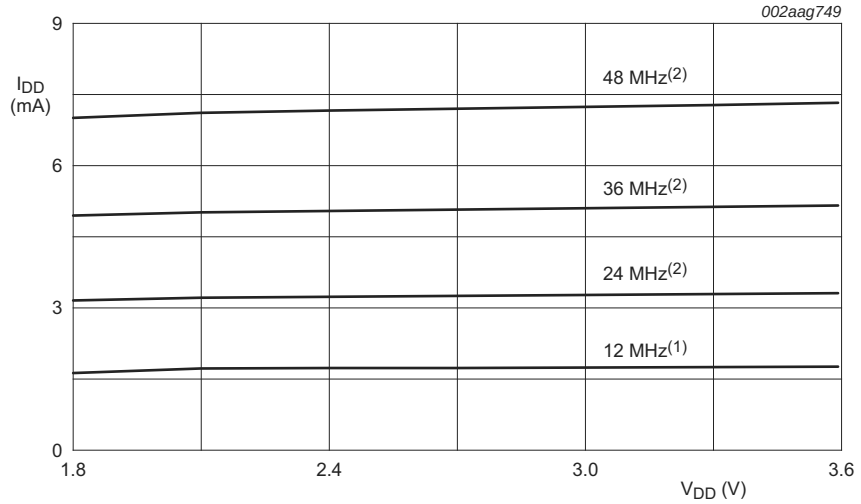
[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 8.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 8.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 8.

[7] T_{amb} = 25 °C; maximum sampling frequency f_s = 400 kSamples/s and analog input capacitance C_{ia} = 1 pF.

[8] Input resistance R_i depends on the sampling frequency fs: $R_i = 1 / (f_s \times C_{ia})$.

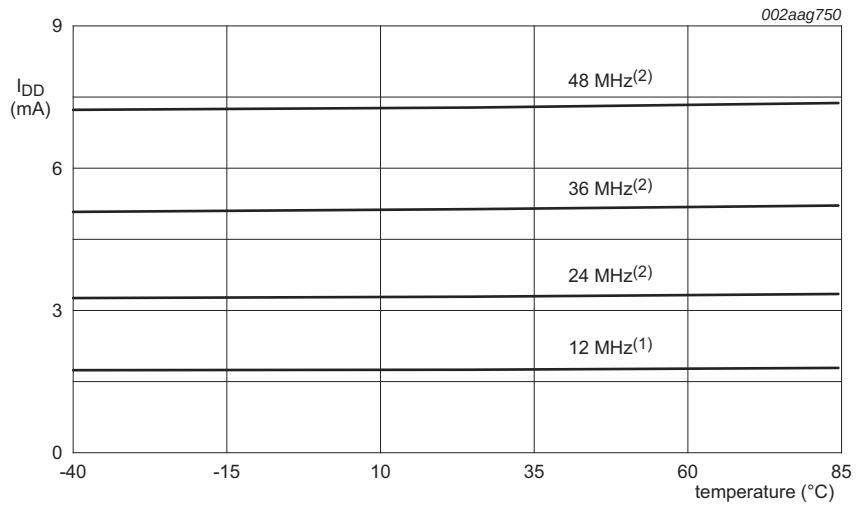


Conditions: T_{amb} = 25 °C; Active mode entered executing code `while(1){}` from flash; internal pull-up resistors disabled; BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; low-current mode; USB_DP and USB_DM pulled LOW externally.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 9. Typical supply current versus regulator supply voltage V_{DD} in active mode



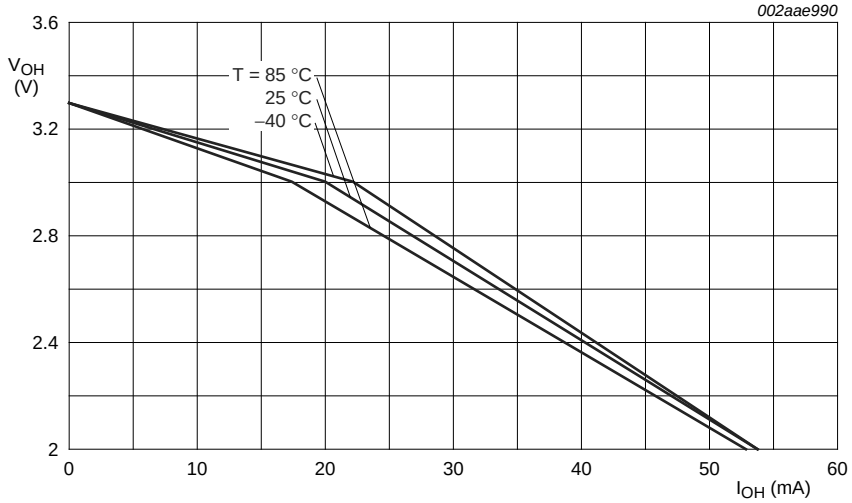
Conditions: V_{DD} = 3.3 V; Active mode entered executing code `while(1){}` from flash; internal pull-up resistors disabled; BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; low-current mode; USB_DP and USB_DM pulled LOW externally.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

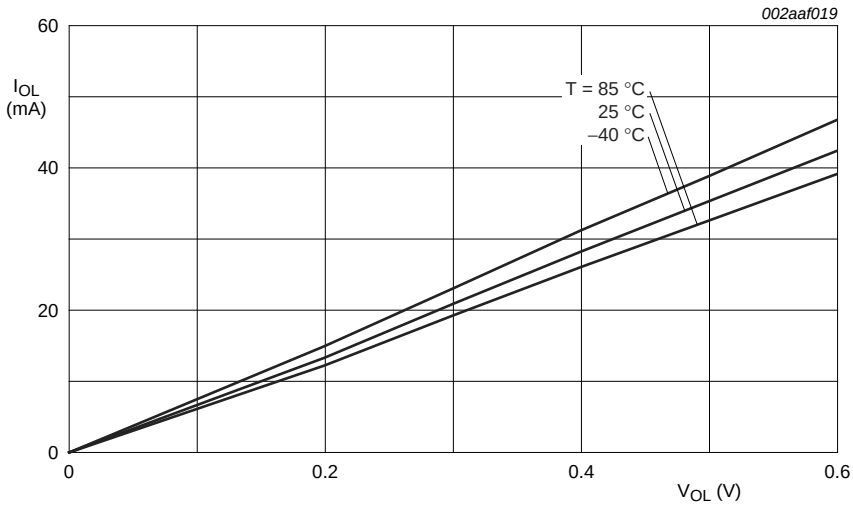
Fig 10. Typical supply current versus temperature in Active mode

9.4 Electrical pin characteristics



Conditions: V_{DD} = 3.3 V; on pin PIO0_7.

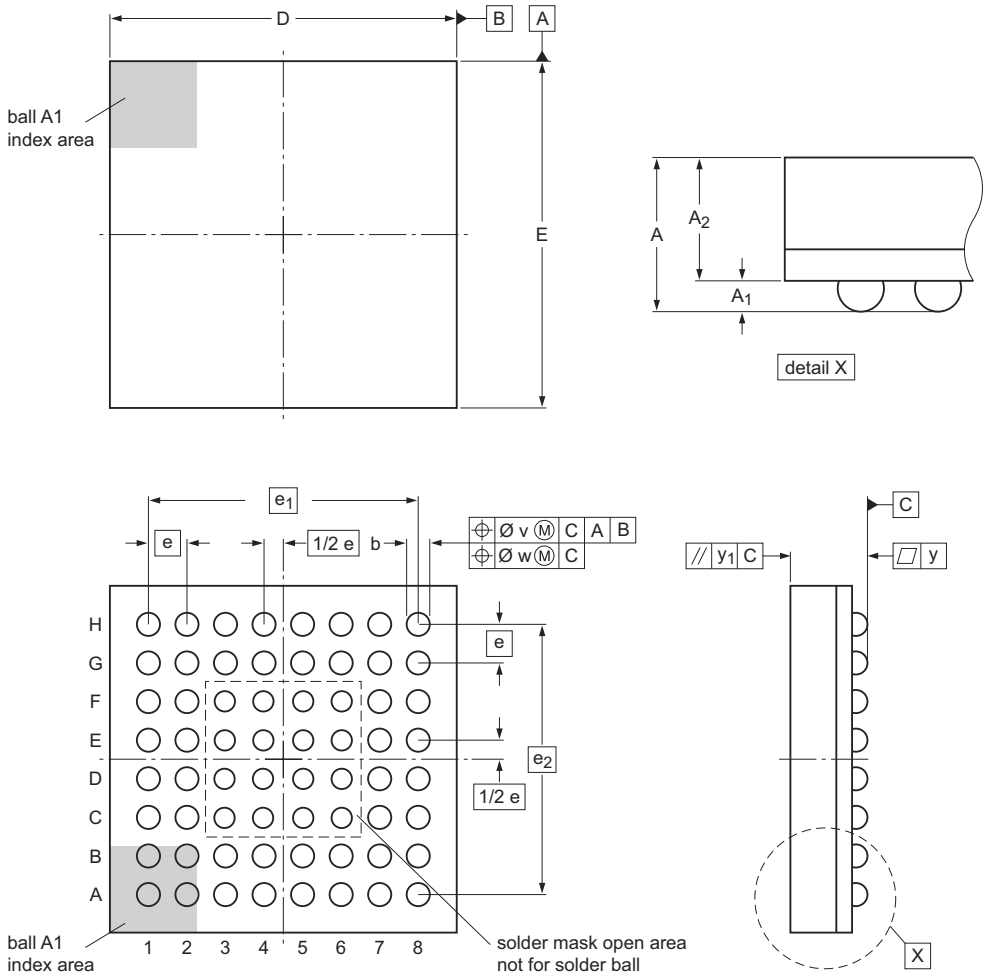
Fig 15. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}.



Conditions: V_{DD} = 3.3 V; on pins PIO0_4 and PIO0_5.

Fig 16. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

TFBGA48: plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 x 4.5 x 0.7 mm **SOT1155-2**



Dimensions

Unit	A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
max	1.10	0.30	0.80	0.35	4.6	4.6							
mm nom	0.95	0.25	0.70	0.30	4.5	4.5	0.5	3.5	3.5	0.15	0.05	0.08	0.1
min	0.85	0.20	0.65	0.25	4.4	4.4							

sot1155-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1155-2		- - -				~~13-06-17~~ 13-06-19

Fig 36. Package outline TFBGA48 (SOT1155-2)

16. Revision history

Table 21. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC11U3X v.2.3	20170208	Product data sheet	-	LPC11U3X v.2.2
Modifications:	• Updated Section 1 “General description”: Software libraries for multiple I/O Handler applications are available on nxp.com.			
LPC11U3X v.2.2	20140311	Product data sheet	-	LPC11U3X v.2.1
Modifications:	• Use of USB_CONNECT signal explained in Section 11.1 “Suggested USB interface solutions”. • Open-drain I^2C-bus and $\overline{\text{RESET}}$ pin descriptions clarified. See Table 3.			
LPC11U3X v.2.1	20131230	Product data sheet	-	LPC11U3X v.2
Modifications:		Add reserved function to pins PIO0_8/MISO0/CT16B0_MAT0/R/IOH_6 and PIO0_9/MOSI0/CT16B0_MAT1/R/IOH_7.		
LPC11U3X v.2	20131125	Product data sheet	-	LPC11U3X v.1.1
Modifications:		• Part LPC11U37HFBD64/401 with I/O handler added. • Additional I/O Handler pin functions added in Table 3. • Typical range of watchdog oscillator frequency changed to 9.4 kHz to 2.3 MHz.See Table 13. • Section 11.8 “I/O Handler software library applications” added. • Updated Section 11.1 “Suggested USB interface solutions” for clarity. • Condition V_{DD} = 0 V added to Parameter V_I in Table 5 for clarity.		
LPC11U3X v.1.1	20130924	Product data sheet	-	LPC11U3X v.1
Modifications:		• Removed the footnote “The peak current is limited to 25 times the corresponding maximum current.” in Table 4. • Table 3: Added “5 V tolerant pad” to $\overline{\text{RESET}}$/PIO0_0 table note. • Table 7: Removed BOD interrupt level 0. • Programmable glitch filter is enabled by default. See Section 7.7.1. • Added Section 11.6 “ADC effective input impedance”. • Table 5 “Static characteristics” added Pin capacitance section. • Updated Section 11.1 “Suggested USB interface solutions”. • Table 4 “Limiting values”: – Updated V_{DD} min and max. – Updated V_I conditions. • Table 10 “EEPROM characteristics”: – Removed f_{clk} and t_{er}; the user does not have control over these parameters. – Changed the t_{prog} from 1.1 ms to 2.9 ms; the EEPROM IAP always does an erase and program, thus the total program time is $t_{er} + t_{prog}$. • Changed title of Figure 29 from “USB interface on a self-powered device” to “USB interface with soft-connect”. • Section 10.7 “USB interface” added. Parameter t_{EOPR1} and t_{EOPR2} renamed to t_{EOPR}.		
LPC11U3X v.1	20120420	Product data sheet	-	-