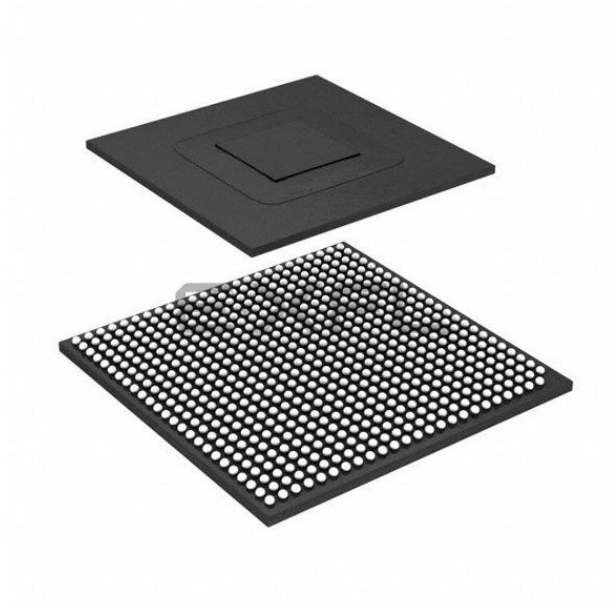

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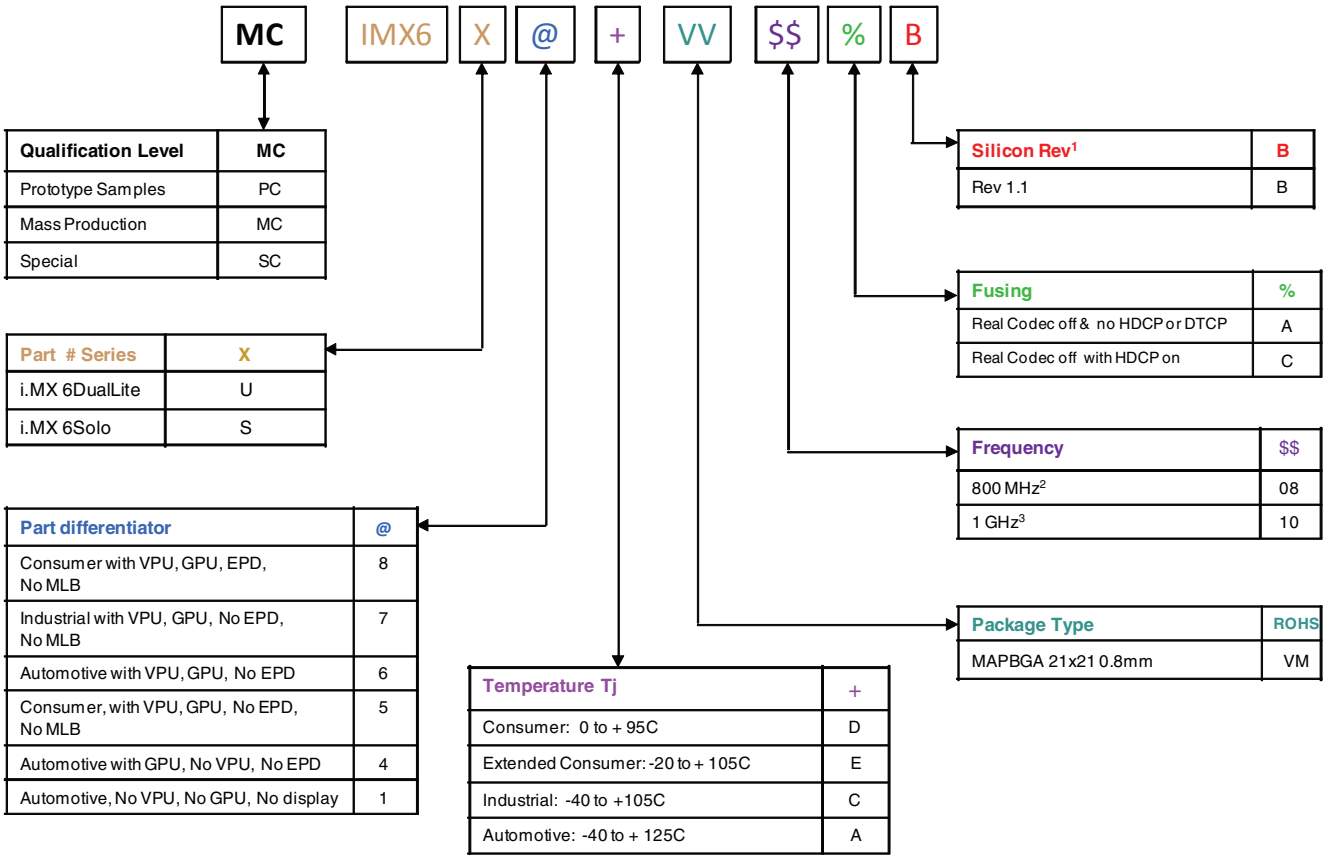
Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6s1avm08ac



1. See the freescale.com\imx6series Web page for latest information on the available silicon revision.
2. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 792 MHz.
3. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz.

Figure 1. Part Number Nomenclature—i.MX 6DualLite and 6Solo

1.2 Features

The i.MX 6Solo/6DualLite processors are based on ARM Cortex-A9 MPCore™ Platform, which has the following features:

- The i.MX 6Solo supports single ARM Cortex-A9 MPCore (with TrustZone)
- The i.MX 6DualLite supports dual ARM Cortex-A9 MPCore (with TrustZone)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer

  - MIPI/DSI, two lanes at 1 Gbps
- Camera sensors:
  - Two parallel Camera ports (up to 20 bit and up to 240 MHz peak)
  - MIPI CSI-2 Serial port, supporting from 80 Mbps to 1 Gbps speed per data lane. The CSI-2 Receiver core can manage one clock lane and up to two data lanes. Each i.MX 6Solo/6DualLite processor has two lanes.
- Expansion cards:
  - Four MMC/SD/SDIO card ports all supporting:
    - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
    - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- USB:
  - One high speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB Phy
  - Three USB 2.0 (480 Mbps) hosts:
    - One HS host with integrated High Speed Phy
    - Two HS hosts with integrated HS-IC USB (High Speed Inter-Chip USB) Phy
- Expansion PCI Express port (PCIe) v2.0 one lane
  - PCI Express (Gen 2.0) dual mode complex, supporting Root complex operations and Endpoint operations. Uses x1 PHY configuration.
- Miscellaneous IPs and interfaces:
  - Three I2S/SSI/AC97, up to 1.4 Mbps each
  - Enhanced Serial Audio Interface (ESAI), up to 1.4 Mbps per channel
  - Five UARTs, up to 4.0 Mbps each:
    - Providing RS232 interface
    - Supporting 9-bit RS485 multidrop mode
    - One of the five UARTs (UART1) supports 8-wire while others four supports 4-wire. This is due to the SoC IOMUX limitation, since all UART IPs are identical.
  - Four eCSPI (Enhanced CSPI)
  - Four I^2C, supporting 400 kbps
  - Gigabit Ethernet Controller (IEEE1588 compliant), 10/100/1000[1] Mbps
  - Four Pulse Width Modulators (PWM)
  - System JTAG Controller (SJC)
  - GPIO with interrupt capabilities
  - 8x8 Key Pad Port (KPP)
  - Sony Philips Digital Interconnect Format (SPDIF), Rx and Tx

1. The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Solo/6DualLite errata document (IMX6SDLCE).

3.1 Special Signal Considerations

Table 3 lists special signal considerations for the i.MX 6Solo/6DualLite processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, "Package Information and Contact Assignments." Signal descriptions are provided in the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

Table 3. Special Signal Considerations

Signal Name	Remarks
CLK1_P/CLK1_N CLK2_P/CLK2_N	Two general purpose differential high speed clock Input/outputs are provided. Any or both of them could be used: • To feed external reference clock to the PLLs and further to the modules inside SoC, for example as alternate reference clock for PCIe, Video/Audio interfaces, etc. • To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals, for example it could be used as an output of the PCIe master clock (root complex use) See the i.MX 6Solo/6DualLite reference manual for details on the respective clock trees. The clock inputs/outputs are LVDS differential pairs compatible with TIA/EIA-644 standard, the maximal frequency range supported is 0...600 MHz. Alternatively one may use single ended signal to drive CLKx_P input. In this case corresponding CLKx_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. See LVDS pad electrical specification for further details. After initialization, the CLKx inputs/outputs could be disabled (if not used). If unused any or both of the CLKx_N/P pairs may be left floating.
RTC_XTALI/RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal, (≤100 kΩ ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI the RTC_XTALO pin should be left floating or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be <100 kHz under typical conditions. In case when high accuracy real time clock are not required system may use internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and keep RTC_XTALO floating.
XTALI/XTALO	A 24.0 MHz crystal should be connected between XTALI and XTALO. level and the frequency should be <32 MHz under typical conditions. The crystal must be rated for a maximum drive level of 250 μW. An ESR (equivalent series resistance) of typical 80 Ω is recommended. Freescale BSP (board support package) software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALI must be directly driven by the external oscillator and XTALO is floated. The XTALI signal level must swing from ~0.8 x NVCC_PLL_OUT to ~0.2 V. If this clock is used as a reference for USB and PCIe, then there are strict frequency tolerance and jitter requirements. See OSC24M chapter and relevant interface specifications chapters for details.

Table 23. OSC32K Main Characteristics

	Min	Typ	Max	Comments
Bias resistor		14 MΩ		This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Crystal Properties				
Cload		10 pF		Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR		50 kΩ	100 kΩ	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes
- LVDS I/O
- MLB I/O

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

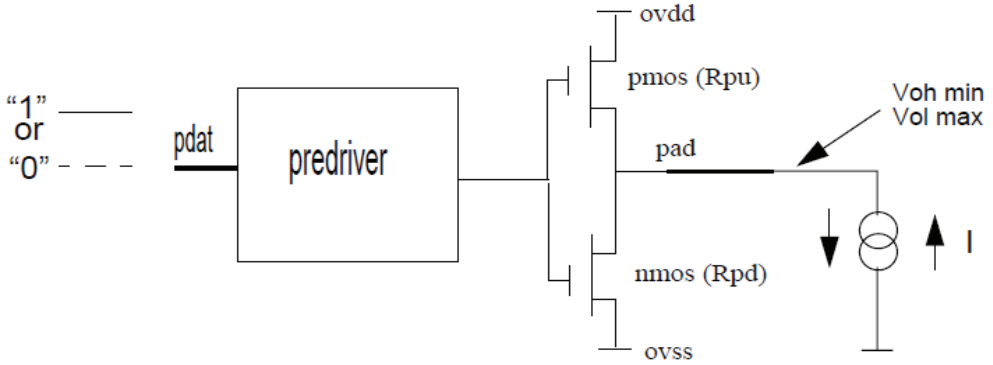


Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

2 Vid(ac) specifies the input differential voltage | Vtr - Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 32 shows the AC parameters for DDR I/O operating in DDR3/DDR3L mode.

Table 32. DDR I/O DDR3/DDR3L Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref - 0.175	V
AC differential input voltage[2]	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	Vref - 0.15	—	Vref + 0.15	V
Over/undershoot peak	Vpeak	—	—	—	0.4	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.5	V-ns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	Driver impedance = 34 Ω	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC JESD79_3C specification supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage | Vtr-Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.7.3 LVDS I/O AC Parameters

The differential output transition time waveform is shown in Figure 6.

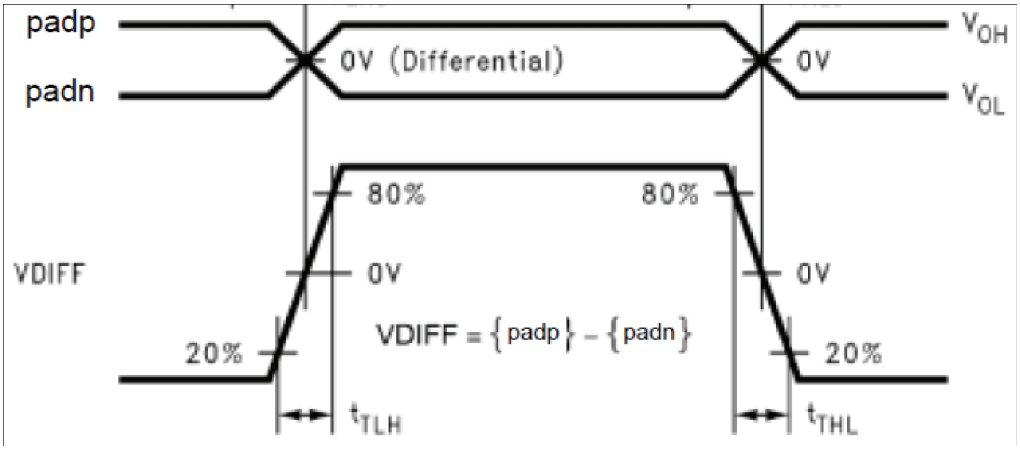
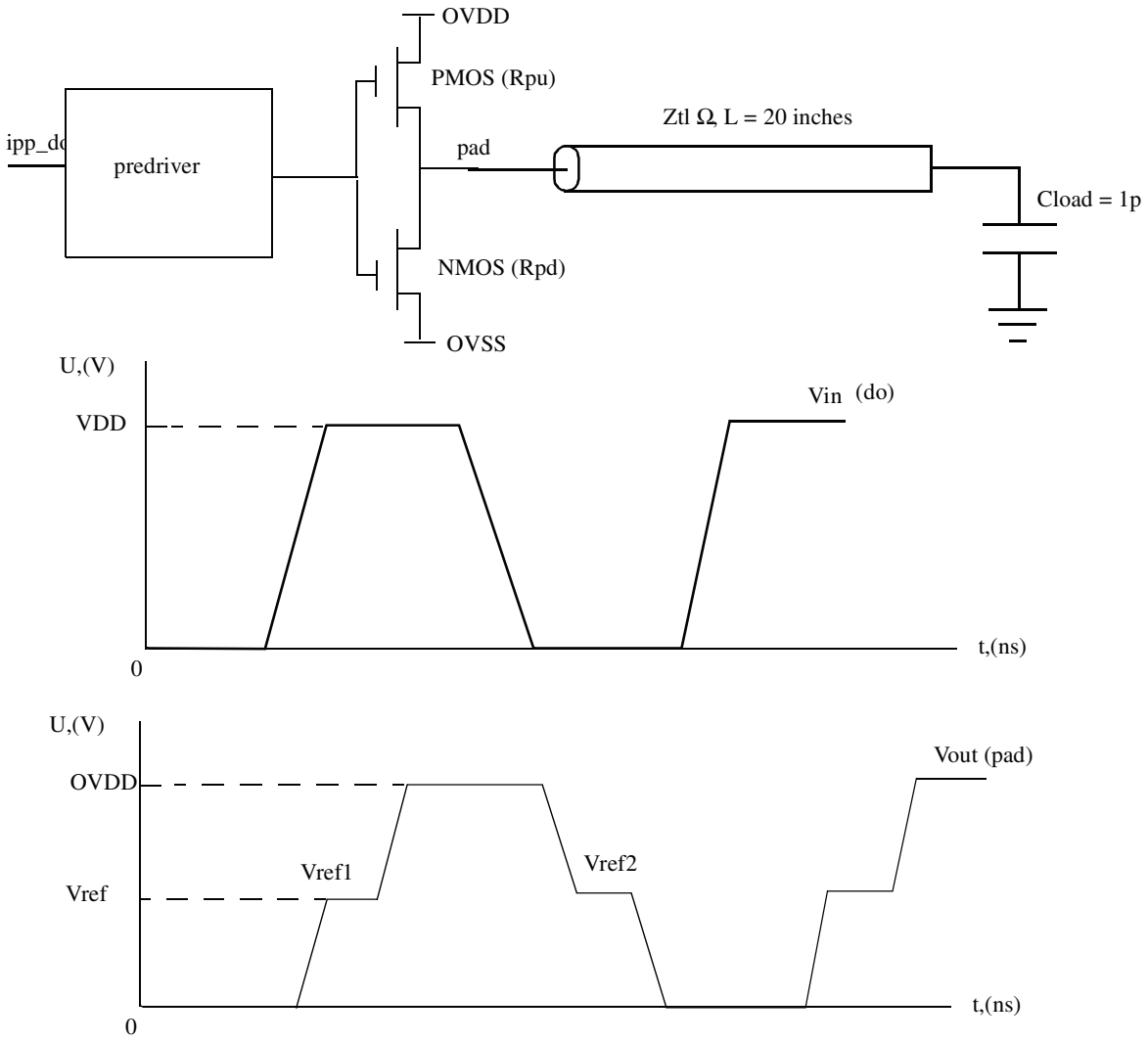


Figure 6. Differential LVDS Driver Transition Time Waveform



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 9. Impedance Matching Load for Measurement

4.9.3.4 Examples of EIM Synchronous Accesses

Table 43. EIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	BCLK Cycle time[2]	t	—	2 x t		3 x t	—	4 x t	—
WE2	BCLK Low Level Width	0.4 x t	—	0.8 x t		1.2 x t	—	1.6 x t	—
WE3	BCLK High Level Width	0.4 x t	—	0.8 x t		1.2 x t	—	1.6 x t	—
WE4	Clock rise to address valid[3]	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE5	Clock rise to address invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE6	Clock rise to CSx_B valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE7	Clock rise to CSx_B invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE8	Clock rise to WE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE9	Clock rise to WE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE10	Clock rise to OE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE11	Clock rise to OE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE12	Clock rise to BEy_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE13	Clock rise to BEy_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE14	Clock rise to ADV_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE15	Clock rise to ADV_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE16	Clock rise to Output Data Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE17	Clock rise to Output Data Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE18	Input Data setup time to Clock rise	2	—	4	—	—	—	—	—

1 All measurements are in reference to Vref level.

2 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 25shows the DDR3/DDR3L write timing parameters. The timing parameters for this diagram appear in Table 46.

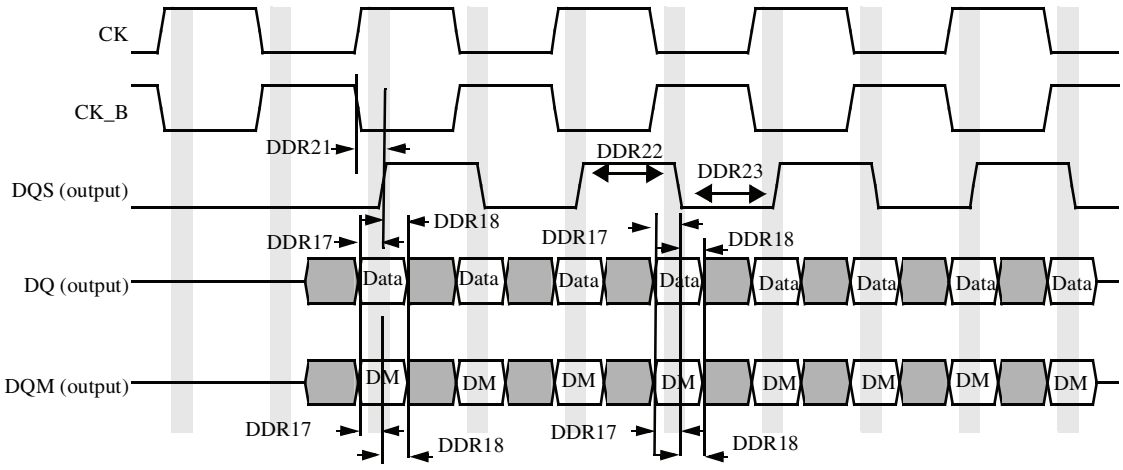


Figure 25. DDR3/DDR3L Write Cycle

Table 46. DDR3/DDR3L Write Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (differential strobe)	t_{DS}	420	—	ps
DDR18	DQ and DQM hold time to DQS (differential strobe)	t_{DH}	345	—	ps
DDR21	DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.25	+0.25	tCK
DDR22	DQS high level width	t_{DQSH}	0.45	0.55	tCK
DDR23	DQS low level width	t_{DQSL}	0.45	0.55	tCK

1 To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

2 All measurements are in reference to Vref level.

3 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

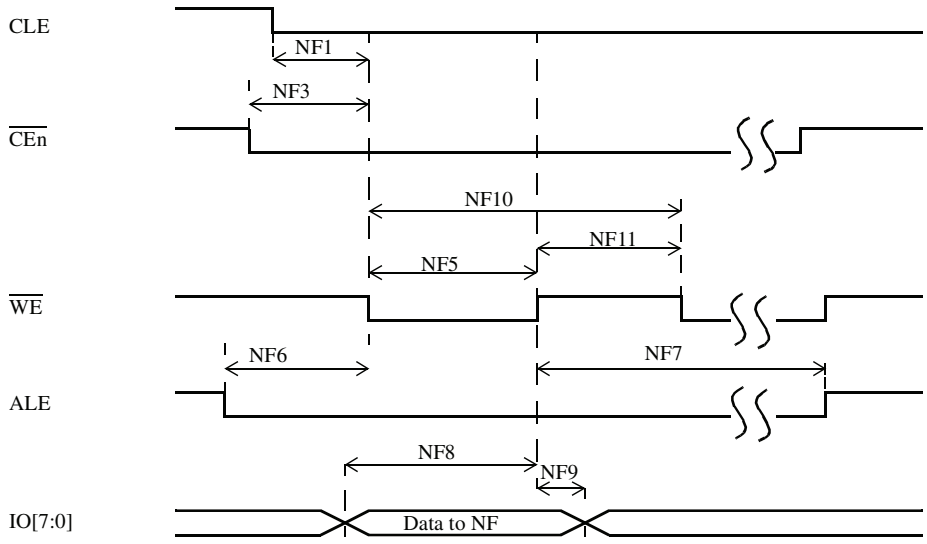


Figure 32. Write Data Latch Cycle Timing Diagram

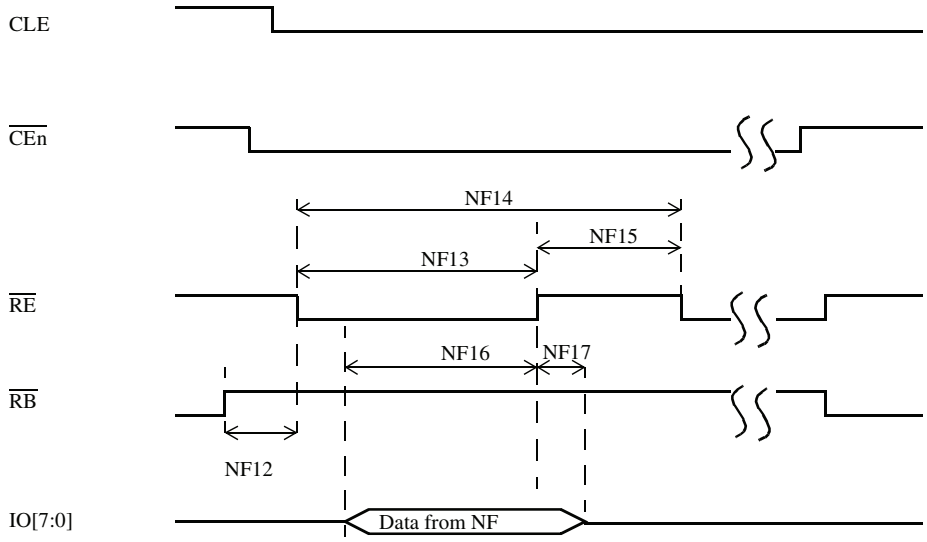


Figure 33. Read Data Latch Cycle Timing Diagram

Table 51. Asynchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Example Timing for GPMI Clock ≈ 100 MHz T = 10 ns		Unit
			Min.	Max.	Min.	Max.	
NF1	CLE setup time	tCLS	(AS+1) x T	—	10	—	ns
NF2	CLE hold time	tCLH	(DH+1) x T	—	20	—	ns
NF3	$\overline{\text{CE}}$n setup time	tCS	(AS+1) x T	—	10	—	ns
NF4	$\overline{\text{CE}}$ hold time	tCH	(DH+1) x T	—	20	—	ns

Table 59. SDR50/SDR104 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs CMD, DAT in SDR104 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	$0.5*t_{CLK}$	—	ns

[1]Data window in SDR100 mode is variable.

4.11.4.4 Bus Operation Condition for 3.3 V and 1.8 V Signaling

Signaling level of SD/eMMC4.3 and eMMC4.4 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1, NVCC_SD2 and NVCC_SD3 supplies are identical to those shown in Table 24, "GPIO DC Parameters," on page 38.

4.11.5 Ethernet Controller (ENET) AC Electrical Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

4.11.5.1 ENET MII Mode Timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

4.11.5.1.1 MII Receive Signal Timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

4.11.10.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.11.10.2.2, "Gated Clock Mode,") except for the SENSB_HSYNC signal, which is not used (see Figure 65). All incoming pixel clocks are valid and cause data to be latched into the input FIFO. The SENSB_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

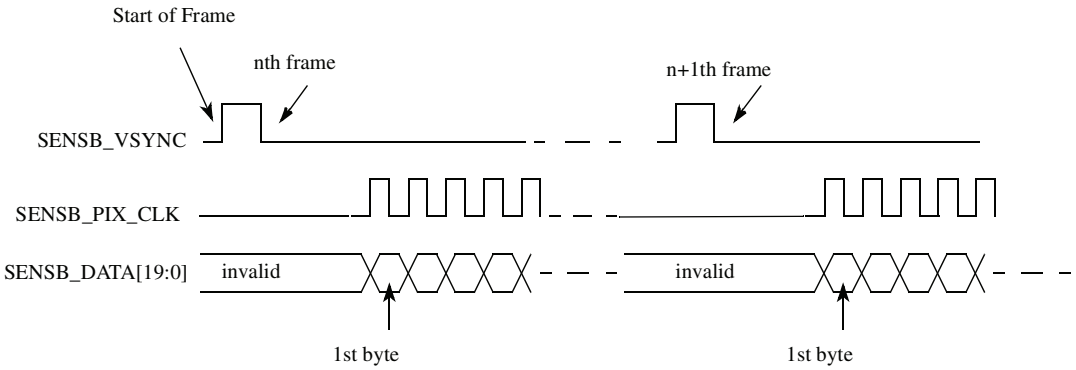


Figure 65. Non-Gated Clock Mode Timing Diagram

The timing described in Figure 65 is that of a typical sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered SENSB_VSYNC; active-high/low SENSB_HSYNC; and rising/falling-edge triggered SENSB_PIX_CLK.

Table 71. Video Signal Cross-Reference

i.MX 6Solo/6DualLite	LCD							Comment[1]
Port Name (x=0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[2]	16-bit YCrCb	20-bit YCrCb	
DISPx_DAT0	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	The restrictions are as follows: • There are maximal three continuous groups of bits that could be independently mapped to the external bus. Groups should not be overlapped. • The bit order is expressed in each of the bit groups, for example, B[0] = least significant blue pixel bit
DISPx_DAT1	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	
DISPx_DAT2	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	
DISPx_DAT3	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	
DISPx_DAT4	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	
DISPx_DAT5	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	
DISPx_DAT6	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	
DISPx_DAT7	DAT[7]	G[2]	G[1]	B[7]	Y/C[7]	C[7]	C[7]	
DISPx_DAT8	DAT[8]	G[3]	G[2]	G[0]	—	Y[0]	C[8]	
DISPx_DAT9	DAT[9]	G[4]	G[3]	G[1]	—	Y[1]	C[9]	
DISPx_DAT10	DAT[10]	G[5]	G[4]	G[2]	—	Y[2]	Y[0]	
DISPx_DAT11	DAT[11]	R[0]	G[5]	G[3]	—	Y[3]	Y[1]	
DISPx_DAT12	DAT[12]	R[1]	R[0]	G[4]	—	Y[4]	Y[2]	
DISPx_DAT13	DAT[13]	R[2]	R[1]	G[5]	—	Y[5]	Y[3]	
DISPx_DAT14	DAT[14]	R[3]	R[2]	G[6]	—	Y[6]	Y[4]	
DISPx_DAT15	DAT[15]	R[4]	R[3]	G[7]	—	Y[7]	Y[5]	
DISPx_DAT16	DAT[16]	—	R[4]	R[0]	—	—	Y[6]	
DISPx_DAT17	DAT[17]	—	R[5]	R[1]	—	—	Y[7]	
DISPx_DAT18	DAT[18]	—	—	R[2]	—	—	Y[8]	
DISPx_DAT19	DAT[19]	—	—	R[3]	—	—	Y[9]	
DISPx_DAT20	DAT[20]	—	—	R[4]	—	—	—	
DISPx_DAT21	DAT[21]	—	—	R[5]	—	—	—	

The maximal accuracy of UP/DOWN edge of IPP_DATA is:

$$Accuracy = T_{diclk} \pm 0.62ns$$

The DISP_CLK_PERIOD, DI_CLK_PERIOD parameters are programmed through the registers.

Figure 70 depicts the synchronous display interface timing for access level. The DISP_CLK_DOWN and DISP_CLK_UP parameters are set through the Register. Table 73 lists the synchronous display interface timing characteristics.

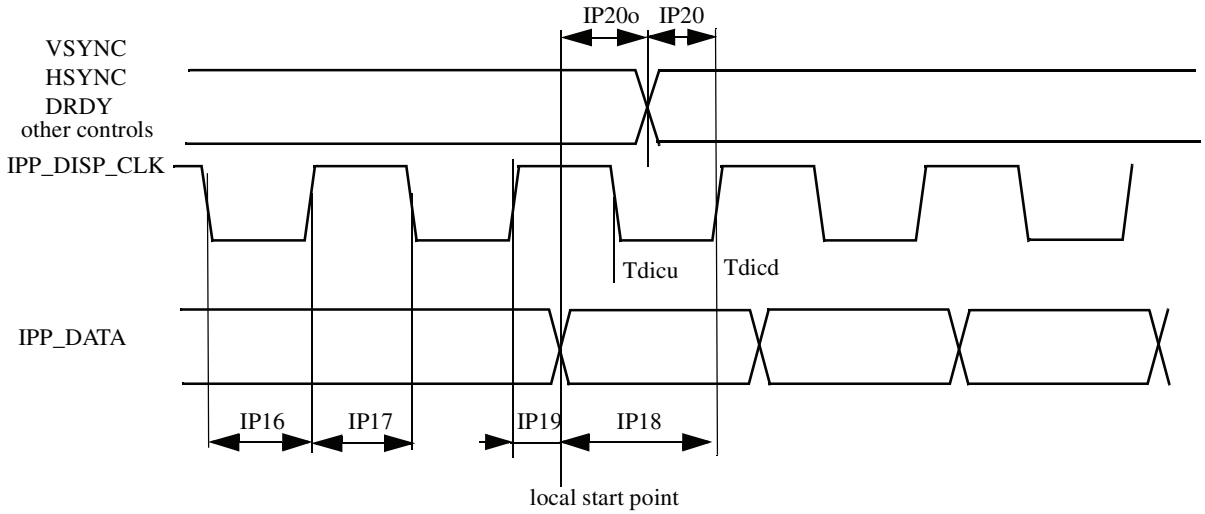


Figure 70. Synchronous Display Interface Timing Diagram—Access Level

Table 73. Synchronous Display Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP16	Display interface clock low time	Tckl	Tdicd-Tdicu-1.24	Tdicd[2]-Tdicu[3]	Tdicd-Tdicu+1.24	ns
IP17	Display interface clock high time	Tckh	Tdicp-Tdicd+Tdicu-1.24	Tdicp-Tdicd+Tdicu	Tdicp-Tdicd+Tdicu+1.2	ns
IP18	Data setup time	Tdsu	Tdicd-1.24	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp-Tdicd-1.24	Tdicp-Tdicu	—	ns
IP20o	Control signals offset times (defines for each pin)	Tocsu	Tocsu-1.24	Tocsu	Tocsu+1.24	ns
IP20	Control signals setup time to display interface clock (defines for each pin)	Tcsu	Tdicd-1.24-Tocsu%Tdicp	Tdicu	—	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

[2] Display interface clock down time

$$Tdicd = \frac{1}{2}\left(T_{diclk} \times ceil\left[\frac{2 \times DISP\_CLK\_DOWN}{DI\_CLK\_PERIOD}\right]\right)$$

4.11.12.4 Possible ΔVCMTX and ΔVOD Distortions of the Single-ended HS Signals

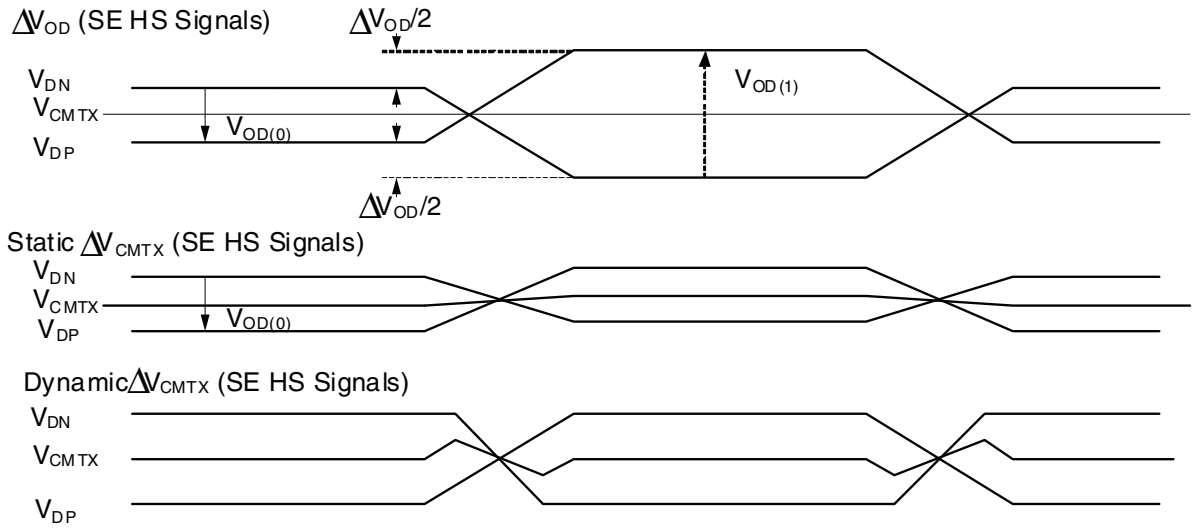


Figure 73. Possible ΔVCMTX and ΔVOD Distortions of the Single-ended HS Signals

4.11.12.5 MIPI D-PHY Switching Characteristics

Table 76. Electrical and Timing Information

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
HS Line Drivers AC Specifications						
—	Maximum serial data rate (forward direction)	On DATAP/N outputs. 80 Ω <= RL <= 125 Ω	80	—	1000	Mbps
F_{DDRCLK}	DDR CLK frequency	On DATAP/N outputs.	40	—	500	MHz
P_{DDRCLK}	DDR CLK period	80 Ω<= RL< = 125 Ω	2	—	25	ns
t_{CDC}	DDR CLK duty cycle	$t_{CDC} = t_{CPH} / P_{DDRCLK}$	—	50	—	%
t_{CPH}	DDR CLK high time		—	1	—	UI
t_{CPL}	DDR CLK low time		—	1	—	UI
—	DDR CLK / DATA Jitter		—	75	—	ps pk–pk
$t_{SKEW[PN]}$	Intra-Pair (Pulse) skew			0.075		UI
$t_{SKEW[TX]}$	Data to Clock Skew		0.350		0.650	UI
$t_{SETUP[RX]}$	Data to Clock Receiver Setup time		0.15			UI
$t_{HOLD[RX]}$	Clock to Data Receiver Hold time		0.15			UI
t_r	Differential output signal rise time	20% to 80%, RL = 50 Ω	150		0.3UI	ps
t_f	Differential output signal fall time	20% to 80%, RL = 50 Ω	150		0.3UI	ps
$\Delta V_{CMTX(HF)}$	Common level variation above 450 MHz	80 Ω<= RL< = 125 Ω			15	mV_{rms}

6 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 21x21 mm Package Information

6.1.1 Case 2240, 21 x 21 mm, 0.8 mm Pitch, 25 x 25 Ball Matrix

Figure 105 shows the top, bottom, and side views of the 21×21 mm BGA package.

Table 101. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
DISP0_DAT3	P21	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[24]	Input	100 kΩ pull-up
DISP0_DAT4	P20	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[25]	Input	100 kΩ pull-up
DISP0_DAT5	R25	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[26]	Input	100 kΩ pull-up
DISP0_DAT6	R23	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[27]	Input	100 kΩ pull-up
DISP0_DAT7	R24	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[28]	Input	100 kΩ pull-up
DISP0_DAT8	R22	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[29]	Input	100 kΩ pull-up
DISP0_DAT9	T25	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[30]	Input	100 kΩ pull-up
DRAM_A0	AC14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[0]	Output	Low
DRAM_A1	AB14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[1]	Output	Low
DRAM_A10	AA15	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[10]	Output	Low
DRAM_A11	AC12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[11]	Output	Low
DRAM_A12	AD12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[12]	Output	Low
DRAM_A13	AC17	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[13]	Output	Low
DRAM_A14	AA12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[14]	Output	Low
DRAM_A15	Y12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[15]	Output	Low
DRAM_A2	AA14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[2]	Output	Low
DRAM_A3	Y14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[3]	Output	Low
DRAM_A4	W14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[4]	Output	Low
DRAM_A5	AE13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[5]	Output	Low
DRAM_A6	AC13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[6]	Output	Low
DRAM_A7	Y13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[7]	Output	Low
DRAM_A8	AB13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[8]	Output	Low
DRAM_A9	AE12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[9]	Output	Low
DRAM_CAS	AE16	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_CAS	Output	Low
DRAM_CS0	Y16	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_CS[0]	Output	Low
DRAM_CS1	AD17	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_CS[1]	Output	Low
DRAM_D0	AD2	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[0]	Input	100 kΩ pull-up
DRAM_D1	AE2	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[1]	Input	100 kΩ pull-up
DRAM_D10	AA6	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[10]	Input	100 kΩ pull-up
DRAM_D11	AE7	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[11]	Input	100 kΩ pull-up

Table 101. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
LVDS0_TX1_N	U4	NVCC_LVDS2P5					
LVDS0_TX1_P	U3	NVCC_LVDS2P5		ALT0	ldb.LVDS0_TX1	Input	Keeper
LVDS0_TX2_N	V2	NVCC_LVDS2P5					
LVDS0_TX2_P	V1	NVCC_LVDS2P5		ALT0	ldb.LVDS0_TX2	Input	Keeper
LVDS0_TX3_N	W2	NVCC_LVDS2P5					
LVDS0_TX3_P	W1	NVCC_LVDS2P5		ALT0	ldb.LVDS0_TX3	Input	Keeper
LVDS1_CLK_N	Y3	NVCC_LVDS2P5					
LVDS1_CLK_P	Y4	NVCC_LVDS2P5		ALT0	ldb.LVDS1_CLK	Input	Keeper
LVDS1_TX0_N	Y1	NVCC_LVDS2P5					
LVDS1_TX0_P	Y2	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX0	Input	Keeper
LVDS1_TX1_N	AA2	NVCC_LVDS2P5					
LVDS1_TX1_P	AA1	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX1	Input	Keeper
LVDS1_TX2_N	AB1	NVCC_LVDS2P5					
LVDS1_TX2_P	AB2	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX2	Input	Keeper
LVDS1_TX3_N	AA3	NVCC_LVDS2P5					
LVDS1_TX3_P	AA4	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX3	Input	Keeper
MLB_CN	A11	VDDHIGH_CAP					
MLB_CP	B11	VDDHIGH_CAP					
MLB_DN	B10	VDDHIGH_CAP					
MLB_DP	A10	VDDHIGH_CAP					
MLB_SN	A9	VDDHIGH_CAP					
MLB_SP	B9	VDDHIGH_CAP					
NANDF_ALE	A16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[8]	Input	100 kΩ pull-up
NANDF_CLE	C15	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[7]	Input	100 kΩ pull-up
NANDF_CS0	F15	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[11]	Input	100 kΩ pull-up
NANDF_CS1	C16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[14]	Input	100 kΩ pull-up
NANDF_CS2	A17	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[15]	Input	100 kΩ pull-up
NANDF_CS3	D16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[16]	Input	100 kΩ pull-up
NANDF_D0	A18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[0]	Input	100 kΩ pull-up
NANDF_D1	C17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[1]	Input	100 kΩ pull-up

Table 103. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

Y	W	V	U	T	R	P	N
LVDS1_TX0_N	LVDS0_TX3_P	LVDS0_TX2_P	LVDS0_TX0_P	GPIO_2	GPIO_17	CSI0_PIXCLK	CSI0_DAT4
LVDS1_TX0_P	LVDS0_TX3_N	LVDS0_TX2_N	LVDS0_TX0_N	GPIO_9	GPIO_16	CSI0_DAT5	CSI0_VSYNC
LVDS1_CLK_N	GND	LVDS0_CLK_P	LVDS0_TX1_P	GPIO_6	GPIO_7	CSI0_DATA_EN	CSI0_DAT7
LVDS1_CLK_P	KEY_ROW2	LVDS0_CLK_N	LVDS0_TX1_N	GPIO_1	GPIO_5	CSI0_MCLK	CSI0_DAT6
GND	KEY_COL0	KEY_ROW4	KEY_COL3	GPIO_0	GPIO_8	GPIO_19	CSI0_DAT9
DRAM_RESET	KEY_COL2	KEY_ROW0	KEY_ROW1	KEY_COL4	GPIO_4	GPIO_18	CSI0_DAT8
DRAM_D20	GND	NVCC_LVDS2P5	KEY_COL1	KEY_ROW3	GPIO_3	NVCC_GPIO	NVCC_CSI
DRAM_D21	GND	GND	GND	GND	GND	GND	GND
DRAM_D19	GND	NVCC_DRAM	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN
DRAM_D25	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDSOC_CAP	GND	GND
DRAM_SDCKE0	GND	NVCC_DRAM	GND	GND	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
DRAM_A15	GND	NVCC_DRAM	GND	GND	GND	GND	NC
DRAM_A7	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
DRAM_A3	DRAM_A4	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_IN	VDDARM_IN	VDDARM_IN
DRAM_SDBA1	GND	NVCC_DRAM	GND	GND	GND	GND	GND
DRAM_CS0	GND	NVCC_DRAM	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN
DRAM_D36	GND	NVCC_DRAM	GND	GND	GND	VDDPU_CAP	VDDPU_CAP
DRAM_D37	GND	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	GND	GND
DRAM_D40	GND	GND	GND	GND	NVCC_ENET	NVCC_LCD	DI0_DISP_CLK
DRAM_D44	ENET_TXD1	ENET_MDC	ENET_TXD0	DISP0_DAT21	DISP0_DAT13	DISP0_DAT4	DI0_PIN3
DRAM_DQM7	ENET_RXD0	ENET_TX_EN	ENET_CRS_DV	DISP0_DAT16	DISP0_DAT10	DISP0_DAT3	DI0_PIN15
DRAM_D59	ENET_RXD1	ENET_REF_CLK	DISP0_DAT20	DISP0_DAT15	DISP0_DAT8	DISP0_DAT1	EIM_BCLK
DRAM_D62	ENET_RX_ER	ENET_MDIO	DISP0_DAT19	DISP0_DAT11	DISP0_DAT6	DISP0_DAT2	EIM_DA14
GND	DISP0_DAT23	DISP0_DAT22	DISP0_DAT17	DISP0_DAT12	DISP0_DAT7	DISP0_DAT0	EIM_DA15
DRAM_D58	DRAM_D63	DISP0_DAT18	DISP0_DAT14	DISP0_DAT9	DISP0_DAT5	DI0_PIN4	DI0_PIN2
Y	W	V	U	T	R	P	N

7 Revision History

Table 104 provides a revision history for this datasheet.

Table 104. i.MX 6Solo/6DualLite Datasheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 1	11/2012	• Updated Table 1, "Orderable Part Numbers," on page 3. • Updated Figure 1, "Part Number Nomenclature—i.MX 6DualLite and 6Solo," on page 4. • In Section 1.2, “Features,” added a footnote on the bottom of page 6 to specify performance limitation of 1 Gbps ENET. • In Table 7, "Absolute Maximum Ratings," on page 22, added details of VDD_SNVS_IN parameter. • Updated Table 9, "Operating Ranges," on page 24. • In Table 10, "On-Chip LDOs and their On-Chip Loads," on page 25, removed VDD_CACHE_CAP load. • Updated Table 12, "Maximal Supply Currents," on page 27. • Updated Table 15, "PCIe PHY Current Drain," on page 30. • Updated Table 16, "HDMI PHY Current Drain," on page 31. • In Table 23, "OSC32K Main Characteristics," on page 36, added 100 kΩ as ESR parameter max value. • Updated Table 27, "LVDS I/O DC Characteristics," on page 41. • In Table 42, "EIM Internal Module Multiplexing," on page 51, Multiplexed Address/Data mode, 16 Bit column, changed DSZ value to “001.” • In Table 54, "ECSPI Master Mode Timing Parameters," on page 78, updated CS5 and CS6 min values. • Updated Table 64, "RMII Signal Timing," on page 91. • Updated Section 4.11.5.3, “RGMII Signal Switching Specifications.” • Updated Section 4.11.6, “Flexible Controller Area Network (FLEXCAN) AC Electrical Specifications.” • Updated Table 64, "RMII Signal Timing," on page 91. • In Table 76, "Electrical and Timing Information," on page 116, updated $\Delta V_{CMTX(LF)}$ max value. • Updated Figure 88, "PWM Timing," on page 127. • Updated Table 83, "PWM Output Timing Parameters," on page 127. • Updated Section 4.11.22, “USB PHY Parameters.”
Rev. 0	10/2012	Initial public release.

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