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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx6s4avm08ab

- Snoop Control Unit (SCU)
- 512 KB unified I/D L2 cache:
  - Used by one core in i.MX 6Solo
  - Shared by two cores in i.MX 6DualLite
- Two Master AXI bus interfaces output of L2 cache
- Frequency of the core (including Neon and L1 cache), as per Table 9, "Operating Ranges," on page 24.
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The memory system consists of the following components:

- Level 1 Cache—32 KB Instruction, 32 KB Data cache per core
- Level 2 Cache—Unified instruction and data (512 KB)
- On-Chip Memory:
  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 128 KB)
  - Secure/non-secure RAM (16 KB)
- External memory interfaces: The i.MX 6Solo/6DualLite processors support latest, high volume, cost effective handheld DRAM, NOR, and NAND Flash memory standards.
  - 16/32-bit LP-DDR2-800, 16/32-bit DDR3-800 and LV-DDR3-800 in i.MX 6Solo; 16/32/64-bit LP-DDR2-800, 16/32/64-bit DDR3-800 and LV-DDR3-800, supporting DDR interleaving mode for 2x32 LPDDR2-800 in i.MX 6DualLite
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bit.
  - 16/32-bit NOR Flash. All WEIMv2 pins are muxed on other interfaces.
  - 16/32-bit PSRAM, Cellular RAM

Each i.MX 6Solo/6DualLite processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Displays—Total four interfaces available. Total raw pixel rate of all interfaces is up to 450 Mpixels/sec, 24 bpp. Up to two interfaces may be active in parallel.
  - One Parallel 24-bit display port, up to 225 Mpixels/sec (for example, WUXGA at 60 Hz or dual HD1080 and WXGA at 60 Hz)
  - LVDS serial ports—One port up to 165 Mpixels/sec or two ports up to 85 MP/sec (for example, WUXGA at 60 Hz) each
  - HDMI 1.4 port

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CCM GPC SRC	Clock Control Module, Global Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSI	MIPI CSI-2 i/f	Multimedia Peripherals	The CSI IP provides MIPI CSI-2 standard camera interface port. The CSI-2 interface supports from 80 Mbps to 1 Gbps speed per data lane.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6Solo/6DualLite platform.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCIC-0 DCIC-1	Display Content Integrity Checker	Automotive IP	The DCIC provides integrity check on portion(s) of the display. Each i.MX 6Solo/6DualLite processor has two such modules.
DSI	MIPI DSI i/f	Multimedia Peripherals	The MIPI DSI IP provides DSI standard display port interface. The DSI interface support 80 Mbps to 1 Gbps speed per data lane.
DTCP	DTCP	Multimedia Peripherals	Provides encryption function according to Digital Transmission Content Protection standard for traffic over MLB150.
eCSPI1-4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface, which is used on the AP to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options. The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.
TEMPMON	Temperature Monitor	System Control Peripherals	The Temperature sensor IP is used for detecting die temperature. The temperature read out does not reflect case or ambient temperature. It reflects the temperature in proximity of the sensor location on the die. Temperature distribution may not be uniformly distributed, therefore the read out value may not be the reflection of the temperature value of the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 4 MHz. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard and the i.MX31 UART modules. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOH3	USB 2.0 High Speed OTG and 3x HS Hosts	Connectivity Peripherals	USBOH3 contains: • One high-speed OTG module with integrated HS USB PHY • One high-speed Host module with integrated HS USB PHY • Two identical high-speed Host modules connected to HSIC USB ports.
VDOA	VDOA	Multimedia Peripherals	Video Data Order Adapter (VDOA): used to re-order video data from the “tiled” order used by the VPU to the conventional raster-scan order needed by the IPU.

4.1.3 Operating Ranges

Table 9 provides the operating ranges of the i.MX 6Solo/6DualLite processors. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

Table 9. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
Run mode: LDO enabled	VDDARM_IN	1.275[2]	—	1.5	V	LDO Output Set Point (VDDARM_CAP) = 1.150 V minimum for operation up to 792 MHz.
		1.175[2]	—	1.5	V	LDO Output Set Point (VDDARM_CAP) = 1.05 V minimum for operation up to 396 MHz.
	VDDSOC_IN[3]	1.275[2,4]	—	1.5	V	VPU </= 328 MHz, VDDSOC and VDDPU LDO outputs (VDDSOC_CAP and VDDPU_CAP) = 1.225 V maximum and 1.15 V minimum.
Run mode: LDO bypassed	VDDARM_IN	1.150	—	1.3	V	LDO bypassed for operation up to 792 MHz
		1.05	—	1.3	V	LDO bypassed for operation up to 396 MHz
	VDDSOC_IN[3]	1.15[4]	—	1.225	V	LDO bypassed for operation VPU </= 328 MHz
Standby/DSM mode	VDDARM_IN	0.9	—	1.3	V	Refer to Table 13, "Stop Mode Current and Power Consumption," on page 29.
	VDDSOC_IN	0.9	—	1.225	V	
VDDHIGH internal regulator	VDDHIGH_IN	2.8	—	3.3	V	Must match the range of voltges that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[5]	2.9	—	3.3	V	Should be supplied from the same supply as VDDHIGH_IN if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG_VBUS	4.4	—	5.25	V	
	USB_H1_VBUS	4.4	—	5.25	V	
DDR I/O supply voltage	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2, DDR3-U
		1.425	1.5	1.575	V	DDR3
		1.283	1.35	1.45	V	DDR3_L
Supply for RGMII I/O power group[6]	NVCC_RGMII	1.15	—	2.625	V	1.15 V – 1.30 V in HSIC 1.2 V mode 1.43 V – 1.58 V in RMGII 1.5 V mode 1.70 V – 1.90 V in RMGII 1.8 V mode 2.25 V – 2.625 V in RMGII 2.5 V mode

Table 9. Operating Ranges (continued)

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
GPIO supply voltages[6]	NVCC_CSI, NVCC_EIM, NVCC_ENET, NVCC_GPIO, NVCC_LCD, NVCC_NANDF, NVCC_SD1, NVCC_SD2, NVCC_SD3, NVCC_JTAG	1.65	1.8, 2.8, 3.3	3.6	V	
	NVCC_LVDS2P5[7] NVCC_MIPI	2.25	2.5	2.75	V	
HDMI supply voltages	HDMI_VP	0.99	1.1	1.3	V	
	HDMI_VPH	2.25	2.5	2.75	V	
PCIe supply voltages	PCIE_VP	1.023	1.1	1.225	V	
	PCIE_VPH	2.325	2.5	2.75	V	
	PCIE_VPTX	1.023	1.1	1.225	V	
Junction temperature	T_J	-40	—	125	°C	Refer to Automotive qualification report for details.

1 Applying the maximum voltage results in maximum power consumption and heat generation. Freescale recommends a voltage set point = (Vmin + the supply tolerance). This results in an optimized power/speed ratio.

2 VDDARM_IN and VDDSOC_IN must be 125 mV higher than the LDO Output Set Point for correct regulator supply voltage.

3 VDDSOC_CAP and VDDPU_CAP must be equal.

4 VDDSOC and VDDPU output voltage must be set to this rule: VDDARM - VDDSOC/PU < 100 mV.

5 While setting VDD_SNVS_IN voltage with respect to Charging Currents and RTC, refer to Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

6 All digital I/O supplies (NVCC_xxxx) must be powered under normal conditions whether the associated I/O pins are in use or not and associated IO pins need to have a Pullup or Pulldown resistor applied to limit any floating gate current.

7 This supply also powers the pre-drivers of the DDR IO pins, hence, it must be always provided, even when LVDS is not used

Table 10 shows on-chip LDO regulators that can supply on-chip loads.

Table 10. On-Chip LDOs[1] and their On-Chip Loads

Voltage Source	Load	Comment
VDDHIGH_CAP	NVCC_LVDS2P5	Board-level connection to VDDHIGH_CAP
	NVCC_MIPI	
	HDMI_VPH	
	PCIE_VPH	

[2] To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

[3] Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.2 DDR I/O DC Parameters

The DDR I/O pads support LPDDR2 and DDR3/DDR3L operational modes.

4.6.2.1 LPDDR2 Mode I/O DC Parameters

The LPDDR2 interface mode fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009.

Table 25. LPDDR2 I/O DC Electrical Parameters[1]

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -0.1mA	0.9*OVDD		V
Low-level output voltage	VOL	Iol= 0.1mA		0.1*OVDD	V
Input Reference Voltage	Vref		0.49*OVDD	0.51*OVDD	V
DC High-Level input voltage	Vih_DC		Vref+0.13	OVDD	V
DC Low-Level input voltage	Vil_DC		OVSS	Vref-0.13	V
Differential Input Logic High	Vih_diff		0.26	Note[2]	
Differential Input Logic Low	Vil_diff		Note[3]	-0.26	
Pull-up/Pull-down Impedance Mismatch	Mmpupd		-15	15	%
240 Ω unit calibration resolution	Rres			10	Ω
Keeper Circuit Resistance	Rkeep		110	175	kΩ
Input current (no pull-up/down)	Iin	VI = 0, VI = OVDD	-2.5	2.5	μA

[1] Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

[2] The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

2 Vid(ac) specifies the input differential voltage | Vtr - Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 32 shows the AC parameters for DDR I/O operating in DDR3/DDR3L mode.

Table 32. DDR I/O DDR3/DDR3L Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref - 0.175	V
AC differential input voltage[2]	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	Vref - 0.15	—	Vref + 0.15	V
Over/undershoot peak	Vpeak	—	—	—	0.4	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.5	V-ns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	Driver impedance = 34 Ω	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC JESD79_3C specification supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage | Vtr-Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.7.3 LVDS I/O AC Parameters

The differential output transition time waveform is shown in Figure 6.

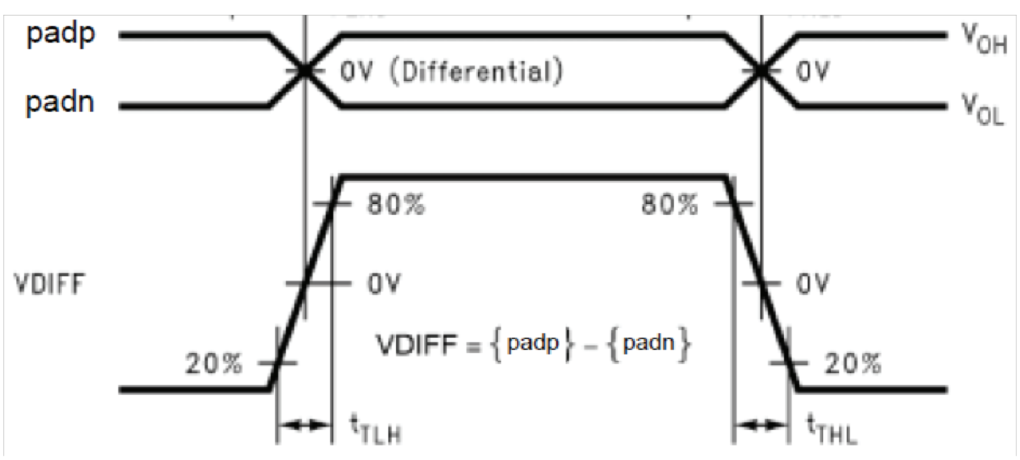

Figure 6. Differential LVDS Driver Transition Time Waveform

4.8.1 GPIO Output Buffer Impedance

Table 35 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 35. GPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	260 130 90 60 50 40 33	Ω

Table 36 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 36. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	150 75 50 37 30 25 20	Ω

4.8.2 DDR I/O Output Buffer Impedance

The LPDDR2 interface fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 37 shows DDR I/O output buffer impedance of i.MX 6Solo/6DualLite processors.

Table 37. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions DSE(Drive Strength)	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	000 001 010 011 100 101 110 111	Hi-Z 240 120 80 60 48 40 34	Hi-Z 240 120 80 60 48 40 34	Ω

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.

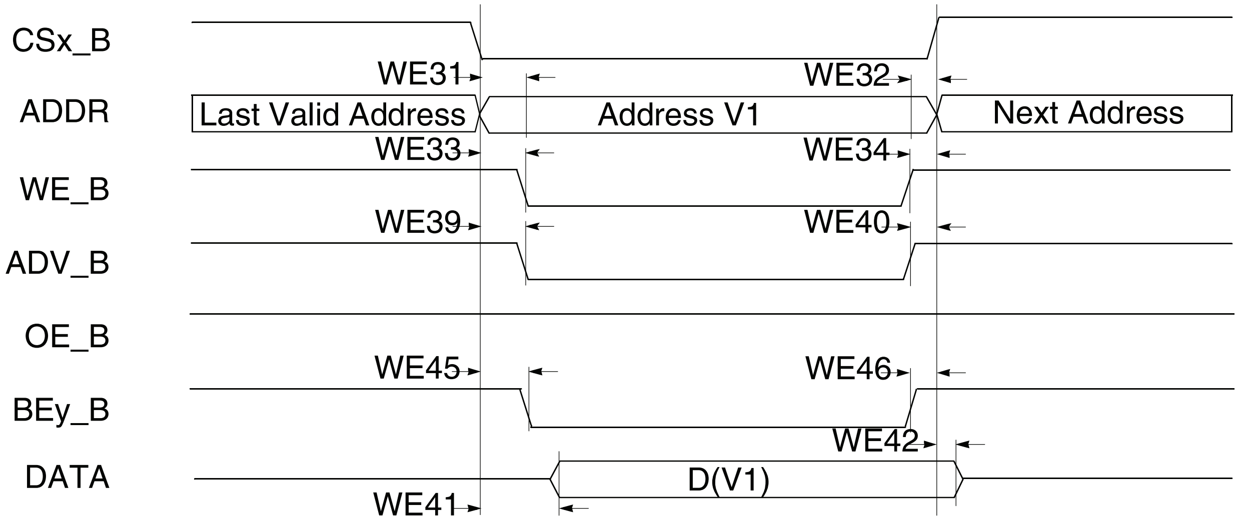

Figure 20. Asynchronous Memory Write Access

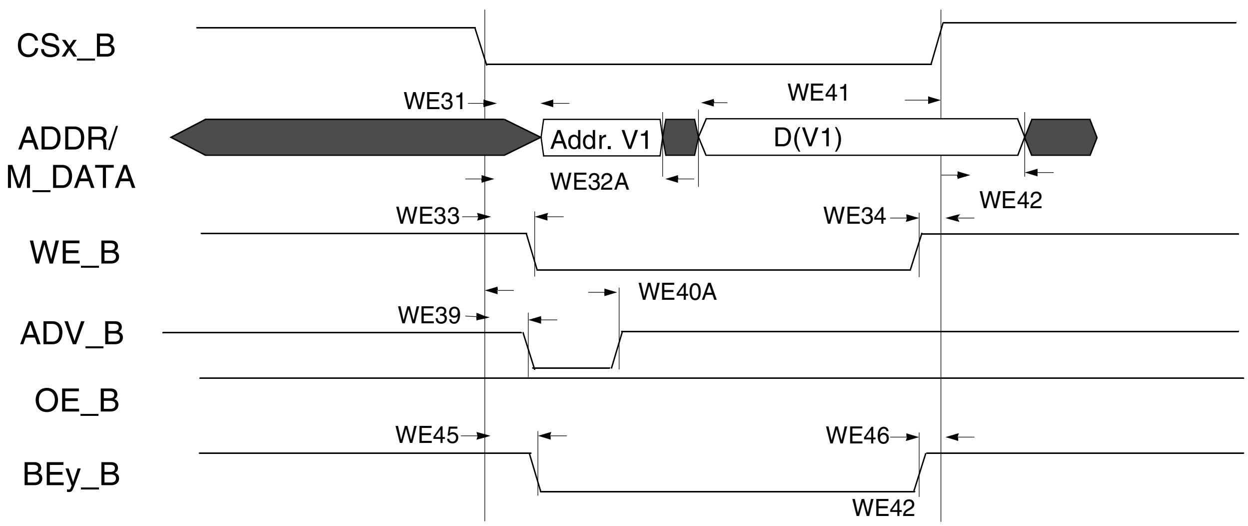

Figure 21. Asynchronous A/D Muxed Write Access

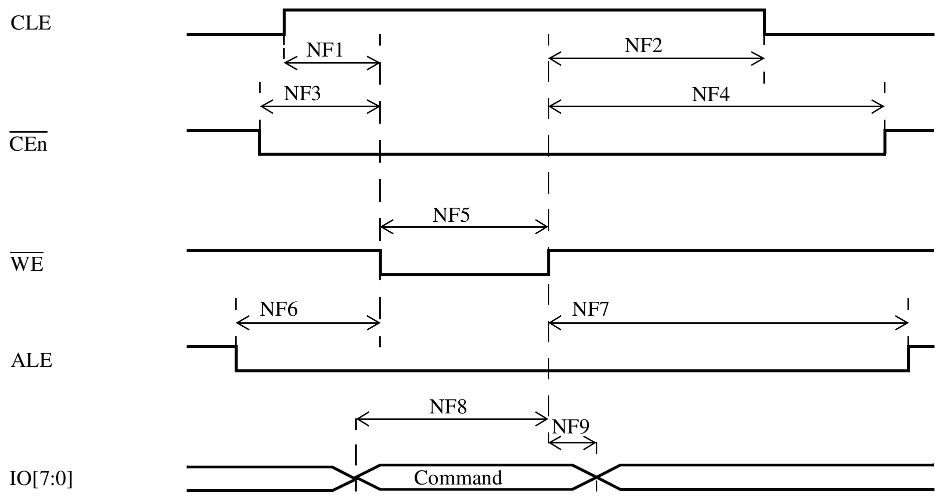

Figure 30. Command Latch Cycle Timing Diagram

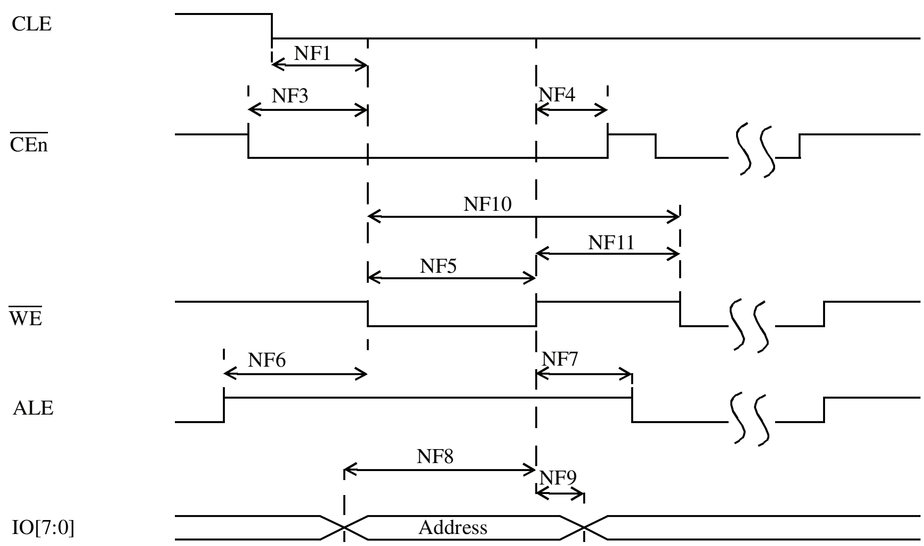

Figure 31. Address Latch Cycle Timing Diagram

Table 52. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	tCE	CE_DELAY x tCK	—	ns
NF19	CE# hold time	tCH	0.5 x tCK	—	ns
NF20	Command/address DQ setup time	tCAS	0.5 x tCK	—	ns
NF21	Command/address DQ hold time	tCAH	0.5 x tCK	—	ns
NF22	clock period	tCK	5	--	ns
NF23	preamble delay	tPRE	PRE_DELAY x tCK	—	ns
NF24	postamble delay	tPOST	POST_DELAY x tCK	—	ns
NF25	CLE and ALE setup time	tCALS	0.5 x tCK	—	ns
NF26	CLE and ALE hold time	tCALH	0.5 x tCK	—	ns
NF27	Data input to first DQS latching transition	tDQSS	tCK	—	ns

[1] GPMI's Sync Mode output timing could be controlled by module's internal registers, say HW_GPMI_TIMING2_CE_DELAY, HW_GPMI_TIMING_PREAMBLE_DELAY, and HW_GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers' settings. In the above table, we use CE_DELAY/PRE_DELAY/POST_DELAY to represent each of these settings.

For DDR Source sync mode, Figure 37 shows the timing diagram of DQS/DQ read valid window. The typical value of tDQSQ is 0.85ns (max) and 1ns (max) for tQHS at 200MB/s. GPMI will sample DQ[7:0] at both rising and falling edge of an delayed DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET(see the GPMI chapter of the i.MX 6Solo/6DualLite reference manual). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.10.3 Samsung Toggle Mode AC Timing

4.10.3.1 Command and Address Timing

NOTE

Samsung Toggle Mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 4.10.1, "Asynchronous Mode AC Timing (ONFI 1.0 Compatible)," for details.

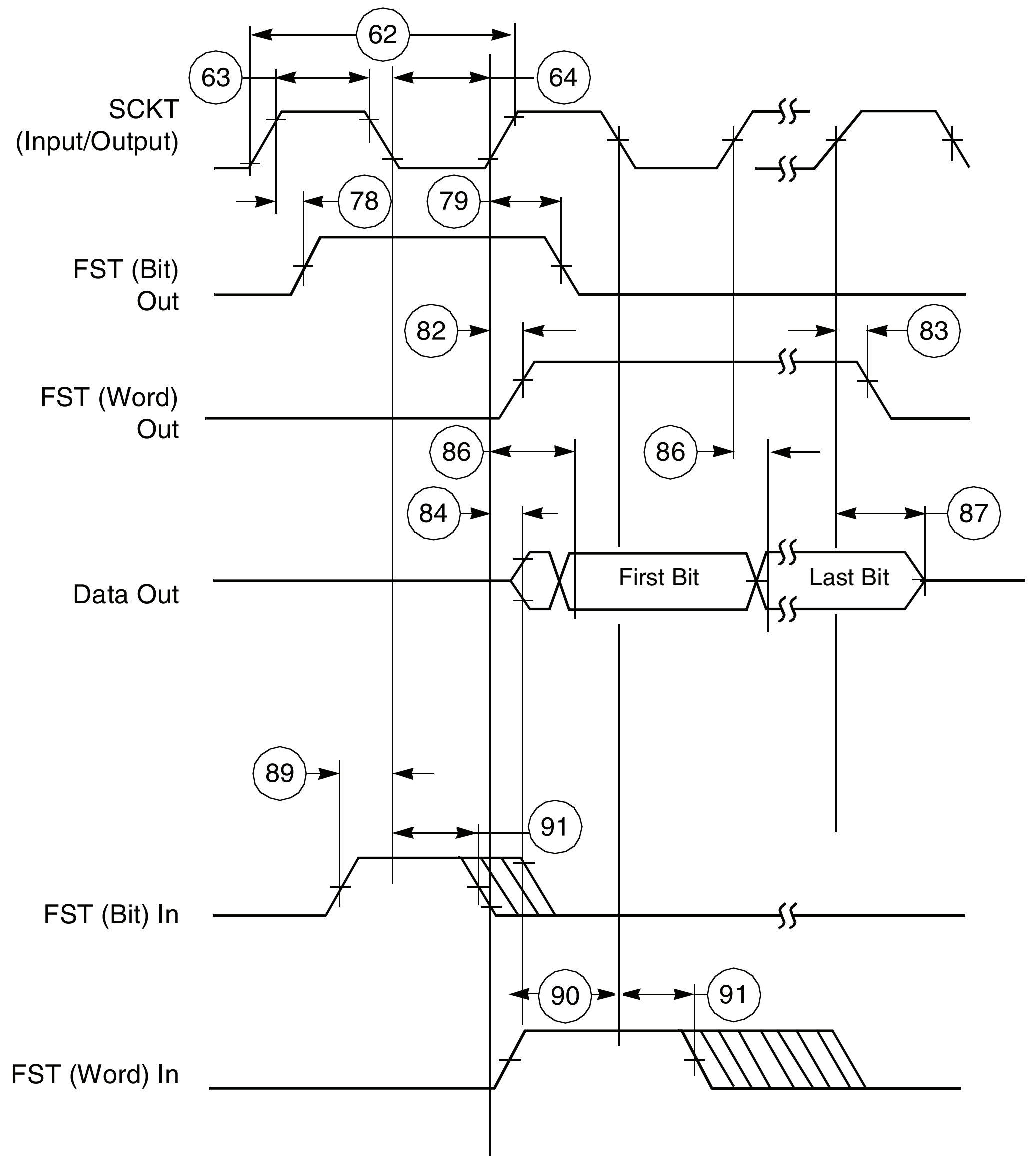

Figure 42. ESAI Transmitter Timing

4.11.10.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

4.11.10.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated “local start point”. The synchronous display controls can be placed on time axis with DI’s offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point. The data bus of the synchronous interface is output direction only.

4.11.10.6.2 LCD Interface Functional Description

Figure 67 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure, signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock is used for calculation of other controls.
- IPP_DISP_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, IPP_DISP_CLK runs continuously.
- HSYNC causes the panel to start a new line. (Usually IPP_PIN_2 is used as HSYNC.)
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse. (Usually IPP_PIN_3 is used as VSYNC.)
- DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.
  (DRDY can be used either synchronous or asynchronous generic purpose pin as well.)

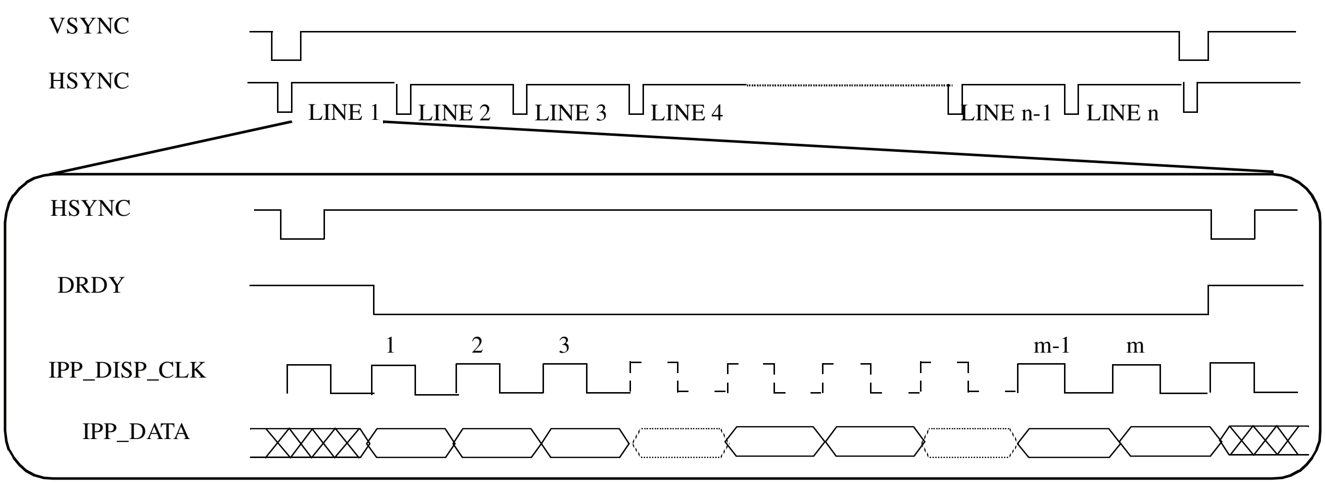

Figure 67. Interface Timing Diagram for TFT (Active Matrix) Panels

4.11.13 HSI Host Controller Timing Parameters

This section describes the timing parameters of the HSI Host Controller which are compliant with High-speed Synchronous Serial Interface (HSI) Physical Layer specification version1.01.

4.11.13.1 Synchronous Data Flow

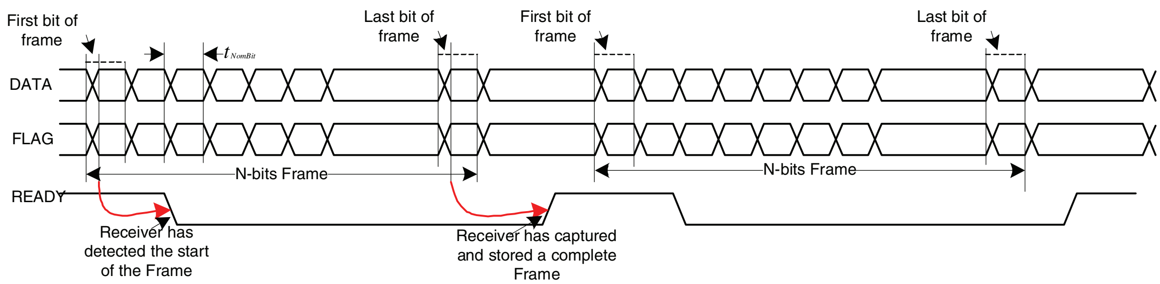

Figure 78. Synchronized Data Flow READY Signal Timing (Frame and Stream Transmission)

4.11.13.2 Pipelined Data Flow

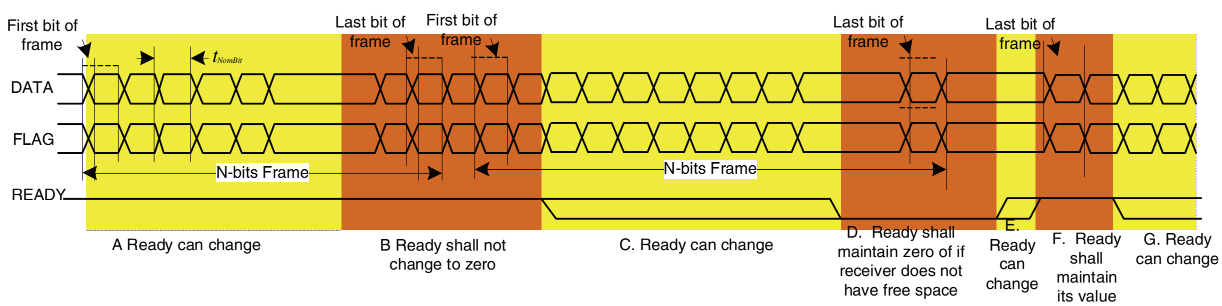

Figure 79. Pipelined Data Flow Ready Signal Timing (Frame Transmission Mode)

4.11.13.3 Receiver Real-Time Data Flow

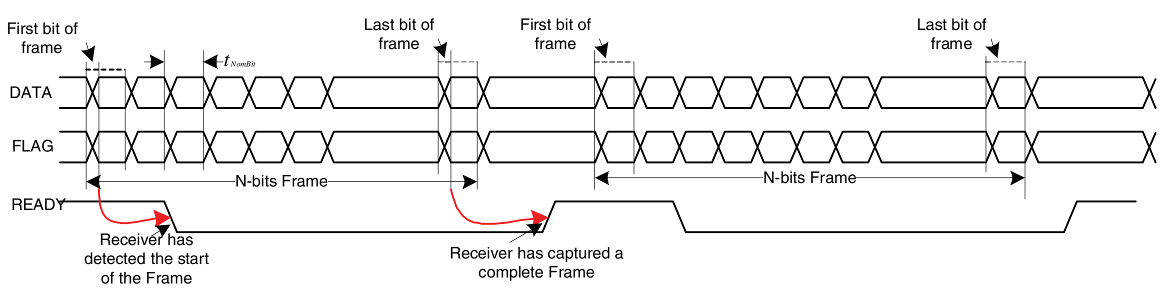

Figure 80. Receiver Real-Time Data Flow READY Signal Timing

Table 85. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIFIN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIFOUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIFOUT1 output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SRCK) period	srckp	40.0	—	ns
SRCK high period	srckph	16.0	—	ns
SRCK low period	srckpl	16.0	—	ns
Modulating Tx clock (STCLK) period	stclkp	40.0	—	ns
STCLK high period	stclkph	16.0	—	ns
STCLK low period	stclkpl	16.0	—	ns

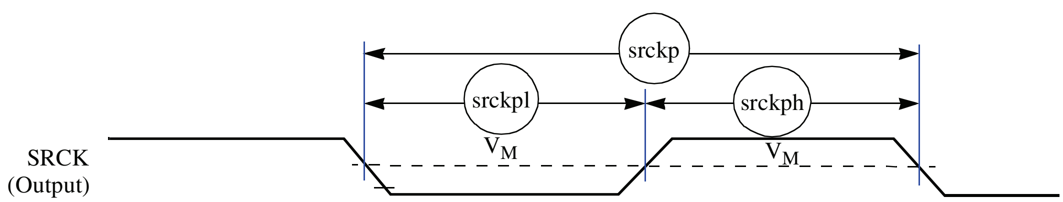

Figure 93. SRCK Timing Diagram

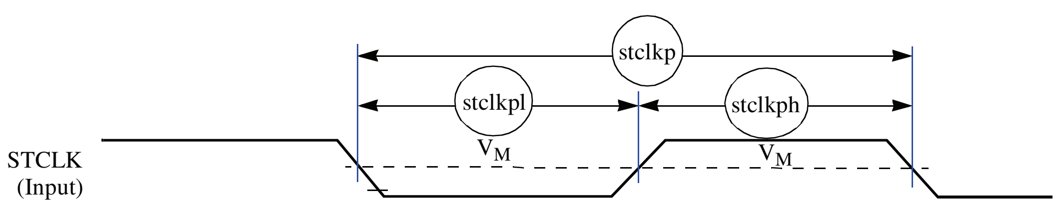

Figure 94. STCLK Timing Diagram

- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 98 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is ‘0’ (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6Solo/6DualLite Fuse Map document and the System Boot chapter in *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

Table 98. Fuses and Associated Pins Used for Boot

Pin	Direction at Reset	eFuse Name	Details
BOOT_MODE1	Input	N/A	Boot Mode selection
BOOT_MODE0	Input	N/A	Boot Mode Selection

Table 101. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
CSI0_DAT6	N4	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[24]	Input	100 kΩ pull-up
CSI0_DAT7	N3	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[25]	Input	100 kΩ pull-up
CSI0_DAT8	N6	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[26]	Input	100 kΩ pull-up
CSI0_DAT9	N5	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[27]	Input	100 kΩ pull-up
CSI0_DATA_EN	P3	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[20]	Input	100 kΩ pull-up
CSI0_MCLK	P4	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[19]	Input	100 kΩ pull-up
CSI0_PIXCLK	P1	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[18]	Input	100 kΩ pull-up
CSI0_VSYNC	N2	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[21]	Input	100 kΩ pull-up
DI0_DISP_CLK	N19	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[16]	Input	100 kΩ pull-up
DI0_PIN15	N21	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[17]	Input	100 kΩ pull-up
DI0_PIN2	N25	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[18]	Input	100 kΩ pull-up
DI0_PIN3	N20	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[19]	Input	100 kΩ pull-up
DI0_PIN4	P25	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[20]	Input	100 kΩ pull-up
DISP0_DAT0	P24	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[21]	Input	100 kΩ pull-up
DISP0_DAT1	P22	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[22]	Input	100 kΩ pull-up
DISP0_DAT10	R21	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[31]	Input	100 kΩ pull-up
DISP0_DAT11	T23	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[5]	Input	100 kΩ pull-up
DISP0_DAT12	T24	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[6]	Input	100 kΩ pull-up
DISP0_DAT13	R20	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[7]	Input	100 kΩ pull-up
DISP0_DAT14	U25	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[8]	Input	100 kΩ pull-up
DISP0_DAT15	T22	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[9]	Input	100 kΩ pull-up
DISP0_DAT16	T21	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[10]	Input	100 kΩ pull-up
DISP0_DAT17	U24	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[11]	Input	100 kΩ pull-up
DISP0_DAT18	V25	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[12]	Input	100 kΩ pull-up
DISP0_DAT19	U23	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[13]	Input	100 kΩ pull-up
DISP0_DAT2	P23	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[23]	Input	100 kΩ pull-up
DISP0_DAT20	U22	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[14]	Input	100 kΩ pull-up
DISP0_DAT21	T20	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[15]	Input	100 kΩ pull-up
DISP0_DAT22	V24	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[16]	Input	100 kΩ pull-up
DISP0_DAT23	W24	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[17]	Input	100 kΩ pull-up

Table 101. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
EIM_D19	G21	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[19]	Input	100 kΩ pull-up
EIM_D20	G20	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[20]	Input	100 kΩ pull-up
EIM_D21	H20	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[21]	Input	100 kΩ pull-up
EIM_D22	E23	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[22]	Input	100 kΩ pull-down
EIM_D23	D25	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[23]	Input	100 kΩ pull-up
EIM_D24	F22	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[24]	Input	100 kΩ pull-up
EIM_D25	G22	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[25]	Input	100 kΩ pull-up
EIM_D26	E24	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[26]	Input	100 kΩ pull-up
EIM_D27	E25	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[27]	Input	100 kΩ pull-up
EIM_D28	G23	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[28]	Input	100 kΩ pull-up
EIM_D29	J19	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[29]	Input	100 kΩ pull-up
EIM_D30	J20	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[30]	Input	100 kΩ pull-up
EIM_D31	H21	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[31]	Input	100 kΩ pull-down
EIM_DA0	L20	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[0]	Input	100 kΩ pull-up
EIM_DA1	J25	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[1]	Input	100 kΩ pull-up
EIM_DA10	M22	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[10]	Input	100 kΩ pull-up
EIM_DA11	M20	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[11]	Input	100 kΩ pull-up
EIM_DA12	M24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[12]	Input	100 kΩ pull-up
EIM_DA13	M23	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[13]	Input	100 kΩ pull-up
EIM_DA14	N23	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[14]	Input	100 kΩ pull-up
EIM_DA15	N24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[15]	Input	100 kΩ pull-up
EIM_DA2	L21	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[2]	Input	100 kΩ pull-up
EIM_DA3	K24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[3]	Input	100 kΩ pull-up
EIM_DA4	L22	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[4]	Input	100 kΩ pull-up
EIM_DA5	L23	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[5]	Input	100 kΩ pull-up
EIM_DA6	K25	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[6]	Input	100 kΩ pull-up
EIM_DA7	L25	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[7]	Input	100 kΩ pull-up
EIM_DA8	L24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[8]	Input	100 kΩ pull-up
EIM_DA9	M21	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[9]	Input	100 kΩ pull-up
EIM_EB0	K21	NVCC_EIM	GPIO	ALT0	weim.WEIM_EB[0]	Output	High

6.1.3 21 x 21 mm, 0.8 mm Pitch Ball Map

Table 102 shows the 21 x 21 mm, 0.8 mm pitch ball map for the i.MX 6Solo.

Table 102. 21 x 21 mm, 0.8 mm Pitch Ball Map

	A	B	C	D	E	F	G	
1	NC	PCIE_RXM	GND	CSI_D1M	NC	NC	DSI_D0P	1
2	PCIE_REXT	PCIE_RXP	JTAG_TRSTB	CSI_D1P	NC	NC	DSI_D0M	2
3	PCIE_TXM	PCIE_TXP	JTAG_TMS	GND	CSI_D0P	CSI_CLK0P	GND	3
4	GND	GND	GND	CSI_REXT	CSI_D0M	CSI_CLK0M	DSI_REXT	4
5	FA_ANA	VDD_FA	CLK2_N	CLK2_P	GND	GND	JTAG_TDI	5
6	USB_OTG_DP	USB_OTG_DN	GND	GND	GND	GND	JTAG_TDO	6
7	XTALI	XTALO	CLK1_N	CLK1_P	GND	GND	PCIE_VPH	7
8	GND	USB_OTG_CHD_B	GPANAIO	GND	NVCC_PLL_OUT	GND	PCIE_VPTX	8
9	MLB_SN	MLB_SP	RTC_XTALO	RTC_XTALI	USB_OTG_VBUS	VDDUSB_CAP	VDD_SNVS_CAP	9
10	MLB_DP	MLB_DN	GND	USB_H1_VBUS	USB_H1_DP	USB_H1_DN	GND	10
11	MLB_CN	MLB_CP	POR_B	PMIC_ON_REQ	TAMPER	PMIC_STBY_REQ	VDD_SNVS_IN	11
12	NC	NC	BOOT_MODE0	ONOFF	TEST_MODE	BOOT_MODE1	NC	12
13	GND	SD3_CMD	SD3_DAT5	SD3_DAT4	SD3_DAT6	SD3_DAT7	NC	13
14	NC	NC	NC	SD3_CLK	SD3_DAT0	SD3_DAT1	NVCC_SD3	14
15	SD3_DAT2	SD3_DAT3	NANDF_CLE	SD3_RST	NANDF_WP_B	NANDF_CS0	NVCC_NANDF	15
16	NANDF_ALE	NANDF_RB0	NANDF_CS1	NANDF_CS3	SD4_CLK	NANDF_D2	NVCC_SD1	16
17	NANDF_CS2	SD4_CMD	NANDF_D1	NANDF_D3	NANDF_D6	SD4_DAT2	NVCC_SD2	17
18	NANDF_D0	NANDF_D5	NANDF_D7	SD4_DAT0	SD4_DAT4	SD1_DAT3	NVCC_RGMII	18
19	NANDF_D4	SD4_DAT1	SD4_DAT5	SD4_DAT7	SD1_DAT2	SD2_CMD	GND	19
20	SD4_DAT3	SD4_DAT6	SD1_DAT1	SD1_CLK	SD2_DAT1	RGMII_TD1	EIM_D20	20
21	SD1_DAT0	SD1_CMD	SD2_CLK	RGMII_TXC	RGMII_TD2	EIM_D17	EIM_D19	21
22	SD2_DAT0	SD2_DAT3	RGMII_TD0	RGMII_RX_CTL	EIM_EB2	EIM_D24	EIM_D25	22
23	SD2_DAT2	RGMII_RD1	RGMII_TX_CTL	RGMII_RD3	EIM_D22	EIM_EB3	EIM_D28	23
24	RGMII_TD3	RGMII_RD2	RGMII_RD0	EIM_D18	EIM_D26	EIM_A22	EIM_A17	24
25	GND	RGMII_RXC	EIM_D16	EIM_D23	EIM_D27	EIM_A24	EIM_A19	25
	A	B	C	D	E	F	G	

Table 102. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

	AE	AD
1	GND	DRAM_D5
2	DRAM_D1	DRAM_D0
3	DRAM_SDQS0	DRAM_SDQS0_B
4	DRAM_D7	GND
5	DRAM_D9	DRAM_D8
6	DRAM_SDQS1_B	DRAM_SDQS1
7	DRAM_D11	GND
8	DRAM_SDQS2_B	DRAM_SDQS2
9	DRAM_D24	DRAM_D29
10	DRAM_DQM3	GND
11	DRAM_D26	DRAM_D30
12	DRAM_A9	DRAM_A12
13	DRAM_A5	GND
14	DRAM_SDCLK_1_B	DRAM_SDCLK_1
15	DRAM_SDCLK_0_B	DRAM_SDCLK_0
16	DRAM_CAS	GND
17	ZQPAD	DRAM_CS1
18	NC	NC
19	NC	GND
20	NC	NC
21	NC	NC
22	NC	GND
23	NC	NC
24	NC	NC
25	GND	NC
	AE	AD

Table 103 shows the 21 x 21 mm, 0.8 mm pitch ball map for the i.MX 6DualLite.

Table 103. 21 x 21 mm, 0.8 mm Pitch Ball Map

D	C	B	A	
CSI_D1M	GND	PCIE_RXM	NC	1
CSI_D1P	JTAG_TRSTB	PCIE_RXP	PCIE_REXT	2
GND	JTAG_TMS	PCIE_TXP	PCIE_TXM	3
CSI_REXT	GND	GND	GND	4
CLK2_P	CLK2_N	VDD_FA	FA_ANA	5
GND	GND	USB_OTG_DN	USB_OTG_DP	6
CLK1_P	CLK1_N	XTALO	XTALI	7
GND	GPANAIO	USB_OTG_CHD_B	GND	8
RTC_XTALI	RTC_XTALO	MLB_SP	MLB_SN	9
USB_H1_VBUS	GND	MLB_DN	MLB_DP	10
PMIC_ON_REQ	POR_B	MLB_CP	MLB_CN	11
ONOFF	BOOT_MODE0	NC	NC	12
SD3_DAT4	SD3_DAT5	SD3_CMD	GND	13
SD3_CLK	NC	NC	NC	14
SD3_RST	NANDF_CLE	SD3_DAT3	SD3_DAT2	15
NANDF_CS3	NANDF_CS1	NANDF_RB0	NANDF_ALE	16
NANDF_D3	NANDF_D1	SD4_CMD	NANDF_CS2	17
SD4_DAT0	NANDF_D7	NANDF_D5	NANDF_D0	18
SD4_DAT7	SD4_DAT5	SD4_DAT1	NANDF_D4	19
SD1_CLK	SD1_DAT1	SD4_DAT6	SD4_DAT3	20
RGMII_TXC	SD2_CLK	SD1_CMD	SD1_DAT0	21
RGMII_RX_CTL	RGMII_TD0	SD2_DAT3	SD2_DAT0	22
RGMII_RD3	RGMII_TX_CTL	RGMII_RD1	SD2_DAT2	23
EIM_D18	RGMII_RD0	RGMII_RD2	RGMII_TD3	24
EIM_D23	EIM_D16	RGMII_RXC	GND	25