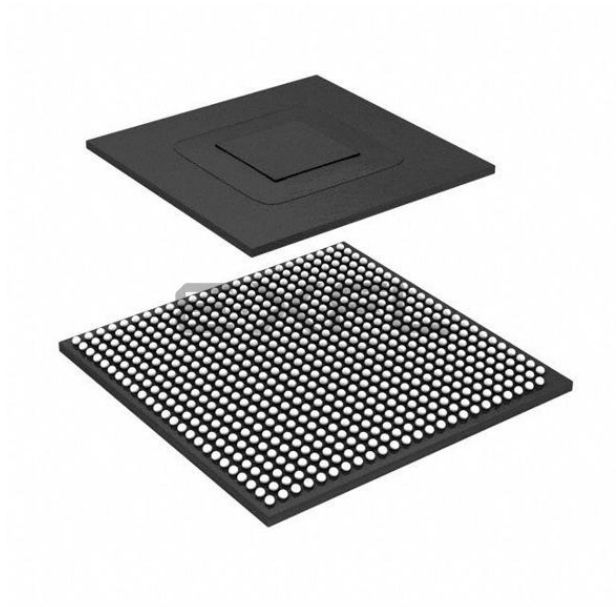

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6s4avm08acr

4.1.3 Operating Ranges

Table 9 provides the operating ranges of the i.MX 6Solo/6DualLite processors. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

Table 9. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
Run mode: LDO enabled	VDDARM_IN	1.275[2]	—	1.5	V	LDO Output Set Point (VDDARM_CAP) = 1.150 V minimum for operation up to 792 MHz.
		1.175[2]	—	1.5	V	LDO Output Set Point (VDDARM_CAP) = 1.05 V minimum for operation up to 396 MHz.
	VDDSOC_IN[3]	1.275[2,4]	—	1.5	V	VPU </= 328 MHz, VDDSOC and VDDPU LDO outputs (VDDSOC_CAP and VDDPU_CAP) = 1.225 V maximum and 1.15 V minimum.
Run mode: LDO bypassed	VDDARM_IN	1.150	—	1.3	V	LDO bypassed for operation up to 792 MHz
		1.05	—	1.3	V	LDO bypassed for operation up to 396 MHz
	VDDSOC_IN[3]	1.15[4]	—	1.225	V	LDO bypassed for operation VPU </= 328 MHz
Standby/DSM mode	VDDARM_IN	0.9	—	1.3	V	Refer to Table 13, "Stop Mode Current and Power Consumption," on page 29.
	VDDSOC_IN	0.9	—	1.225	V	
VDDHIGH internal regulator	VDDHIGH_IN	2.8	—	3.3	V	Must match the range of voltges that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[5]	2.9	—	3.3	V	Should be supplied from the same supply as VDDHIGH_IN if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG_VBUS	4.4	—	5.25	V	
	USB_H1_VBUS	4.4	—	5.25	V	
DDR I/O supply voltage	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2, DDR3-U
		1.425	1.5	1.575	V	DDR3
		1.283	1.35	1.45	V	DDR3_L
Supply for RGMII I/O power group[6]	NVCC_RGMII	1.15	—	2.625	V	1.15 V – 1.30 V in HSIC 1.2 V mode 1.43 V – 1.58 V in RMGII 1.5 V mode 1.70 V – 1.90 V in RMGII 1.8 V mode 2.25 V – 2.625 V in RMGII 2.5 V mode

— VDDARM_IN supply must be turned ON together with VDDSOC_IN supply or not delayed more than 1 ms

— VDDARM_CAP must not exceed VDDSOC_CAP by more than 50 mV.

NOTE

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the *i.MX 6Solo/6DualLite Reference Manual* for further details and to ensure that all necessary requirements are being met.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG_VBUS and USB_H1_VBUS are not part of the power supply sequence and may be powered at any time.

4.2.2 Power-Down Sequence

No special restrictions for i.MX 6Solo/6DualLite IC.

4.2.3 Power Supplies Usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Rail” columns in pin list tables of Section 6, “Package Information and Contact Assignments.”

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for details on the power tree scheme.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of

4.9.3.4 Examples of EIM Synchronous Accesses

Table 43. EIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	BCLK Cycle time[2]	t	—	2 x t		3 x t	—	4 x t	—
WE2	BCLK Low Level Width	0.4 x t	—	0.8 x t		1.2 x t	—	1.6 x t	—
WE3	BCLK High Level Width	0.4 x t	—	0.8 x t		1.2 x t	—	1.6 x t	—
WE4	Clock rise to address valid[3]	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE5	Clock rise to address invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE6	Clock rise to CSx_B valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE7	Clock rise to CSx_B invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE8	Clock rise to WE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE9	Clock rise to WE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE10	Clock rise to OE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE11	Clock rise to OE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE12	Clock rise to BEy_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE13	Clock rise to BEy_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE14	Clock rise to ADV_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE15	Clock rise to ADV_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE16	Clock rise to Output Data Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE17	Clock rise to Output Data Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE18	Input Data setup time to Clock rise	2	—	4	—	—	—	—	—

Table 43. EIM Bus Timing Parameters (continued)[1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE19	Input Data hold time from Clock rise	2	—	2	—	—	—	—	—
WE20	WAIT_B setup time to Clock rise	2	—	4	—	—	—	—	—
WE21	WAIT_B hold time from Clock rise	2	—	2	—	—	—	—	—

1 t is the maximal EIM logic (axi_clk) cycle time. The maximum allowed axi_clk frequency depends on the fixed/non-fixed latency configuration, whereas the maximum allowed BCLK frequency is:

—Fixed latency for both read and write is 132 MHz.

—Variable latency for read only is 132 MHz.

—Variable latency for write only is 52 MHz.

In variable latency configuration for write, if BCD = 0 & WBCDD = 1 or BCD = 1, axi_clk must be 104 MHz.Write BCD = 1 and 104 MHz axi_clk, will result in a BCLK of 52 MHz. When the clock branch to EIM is decreased to 104 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for a detailed clock tree description.

2 BCLK parameters are being measured from the 50% point, that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

3 For signal measurements, “High” is defined as 80% of signal value and “Low” is defined as 20% of signal value.

Figure 14 to Figure 17 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

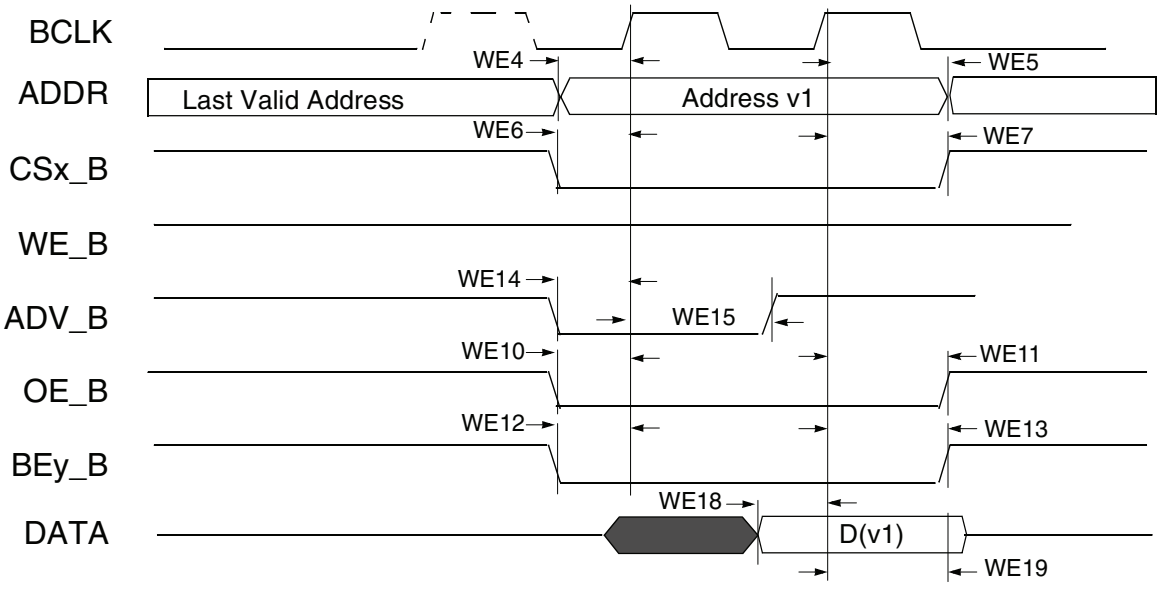

Figure 14. Synchronous Memory Read Access, WSC=1

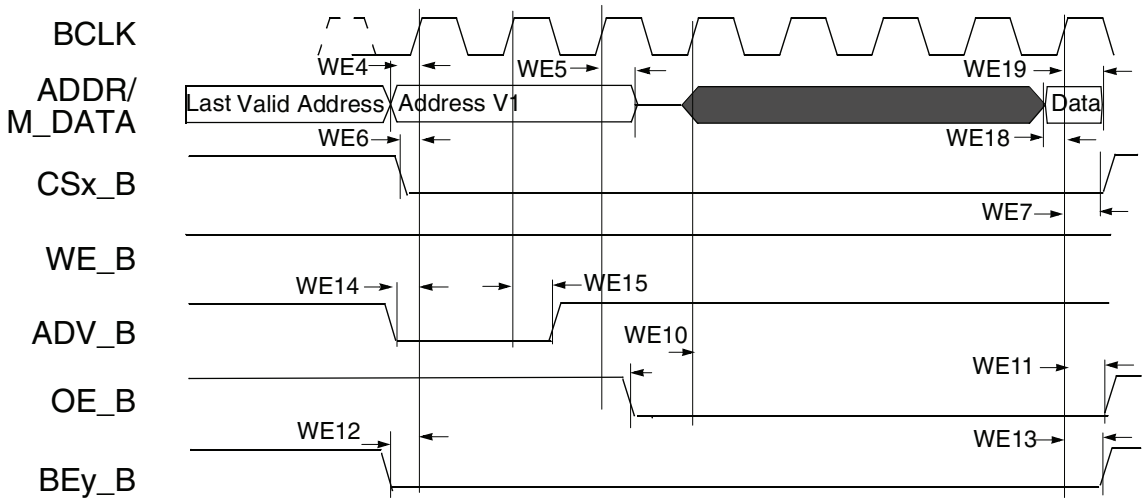

Figure 17. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.5 General EIM Timing-Asynchronous Mode

Figure 18 through Figure 22, and Table 44 help you determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 18 through Figure 21 as RWSC, OEN & CSN is configured differently. See the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for the EIM programming model.

4.10.3.2 Read and Write Timing

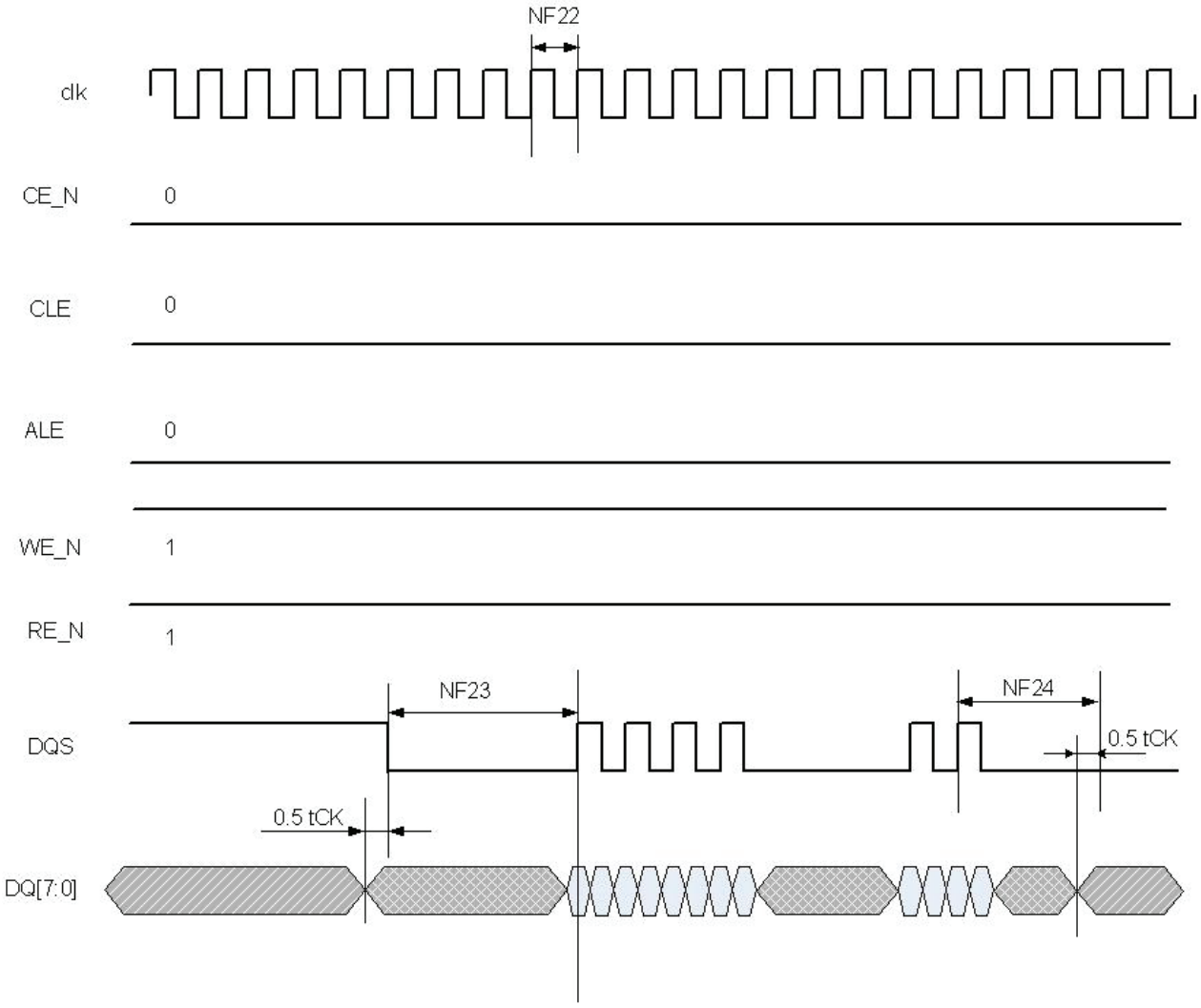

Figure 38. Samsung Toggle Mode Data Write Timing

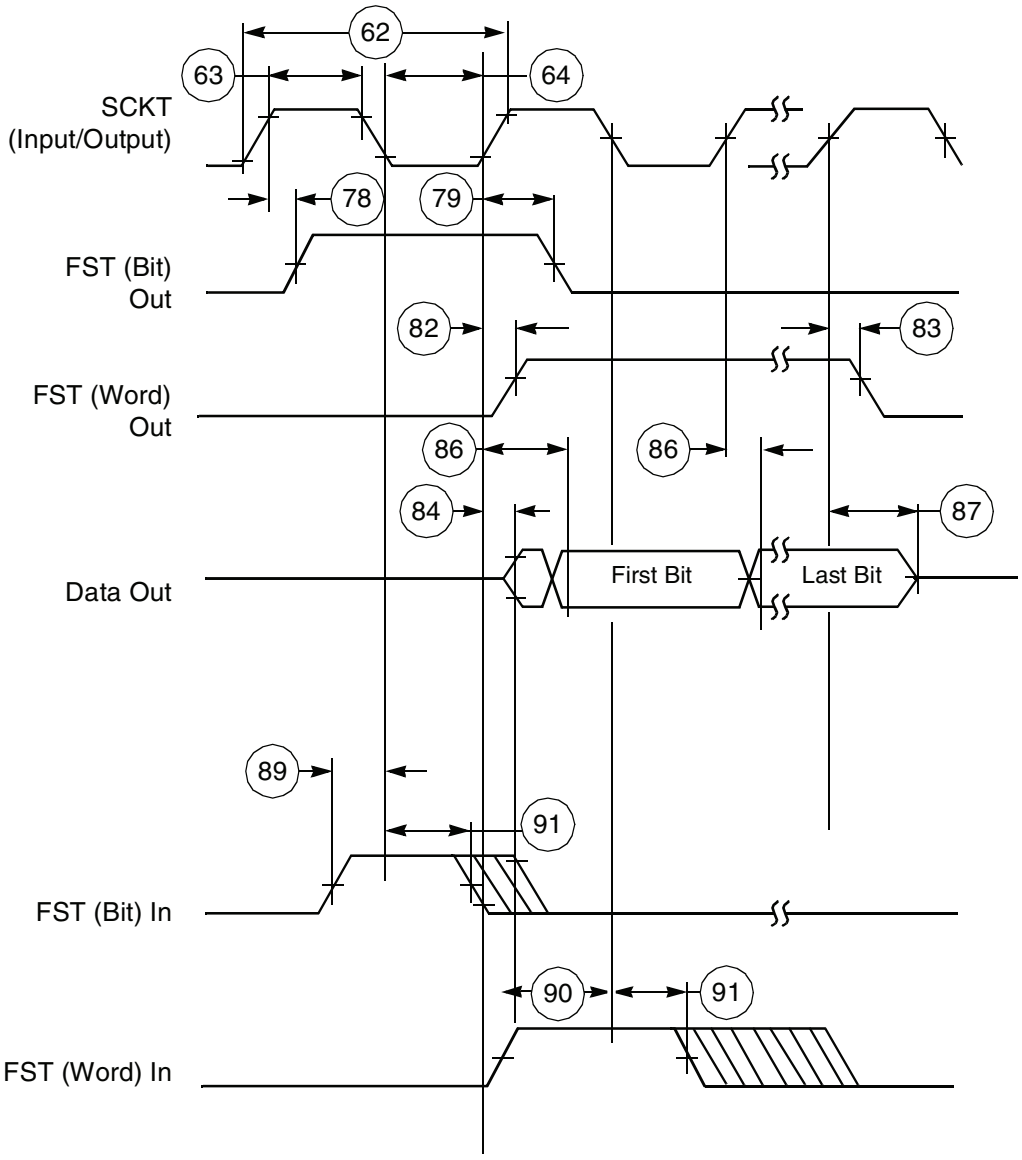

Figure 42. ESAI Transmitter Timing

Table 68. I²C Module Timing Parameters (continued)

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal.

3 A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2CLK line is released.

4 C_b = total capacitance of one bus line in pF.

4.11.10 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

[3] Display interface clock up time where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

$$Tdicu = \frac{1}{2}\left(T_{diclk} \times ceil\left[\frac{2 \times DISP\_CLK\_UP}{DI\_CLK\_PERIOD}\right]\right)$$

4.11.11 LVDS Display Bridge (LDB) Module Parameters

The LVDS interface complies with TIA/EIA 644-A standard. For more details, see TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits”.

Table 74. LVDS Display Bridge (LDB) Electrical Specification

Parameter	Symbol	Test Condition	Min	Max	Units
Differential Voltage Output Voltage	V_{OD}	100 Ω Differential load	250	450	mV
Output Voltage High	Voh	100 Ω differential load (0 V Diff—Output High Voltage static)	1.25	1.6	mV
Output Voltage Low	Vol	100 Ω differential load (0 V Diff—Output Low Voltage static)	0.9	1.25	mV
Offset Static Voltage	V_{OS}	Two 49.9 Ω resistors in series between N-P terminal, with output in either Zero or One state, the voltage measured between the 2 resistors.	1.15	1.375	V
VOS Differential	V_{OSDIFF}	Difference in V_{OS} between a One and a Zero state	-50	50	mV
Output short circuited to GND	ISA ISB	With the output common shorted to GND	-24	24	mA
VT Full Load Test	VTLoad	100 Ω Differential load with a 3.74 kΩ load between GND and IO Supply Voltage	247	454	mV

4.11.12 MIPI D-PHY Timing Parameters

This section describes MIPI D-PHY electrical specifications, compliant with MIPI CSI-2 version 1.0, D-PHY specification Rev. 1.0 (for MIPI sensor port x2 lanes) and MIPI DSI Version 1.01, and D-PHY specification Rev. 1.0 (and also DPI version 2.0, DBI version 2.0, DSC version 1.0a at protocol layer) (for MIPI display port x2 lanes).

4.11.12.1 Electrical and Timing Information

Table 75. Electrical and Timing Information

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
Input DC Specifications - Apply to CLKP/N and DATAP/N inputs						
V_I	Input signal voltage range	Transient voltage range is limited from -300 mV to 1600 mV	-50	—	1350	mV

4.11.12.2 MIPI D-PHY Signaling Levels

The signal levels are different for differential HS mode and single-ended LP mode. Figure 71 shows both the HS and LP signal levels on the left and right sides, respectively. The HS signaling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

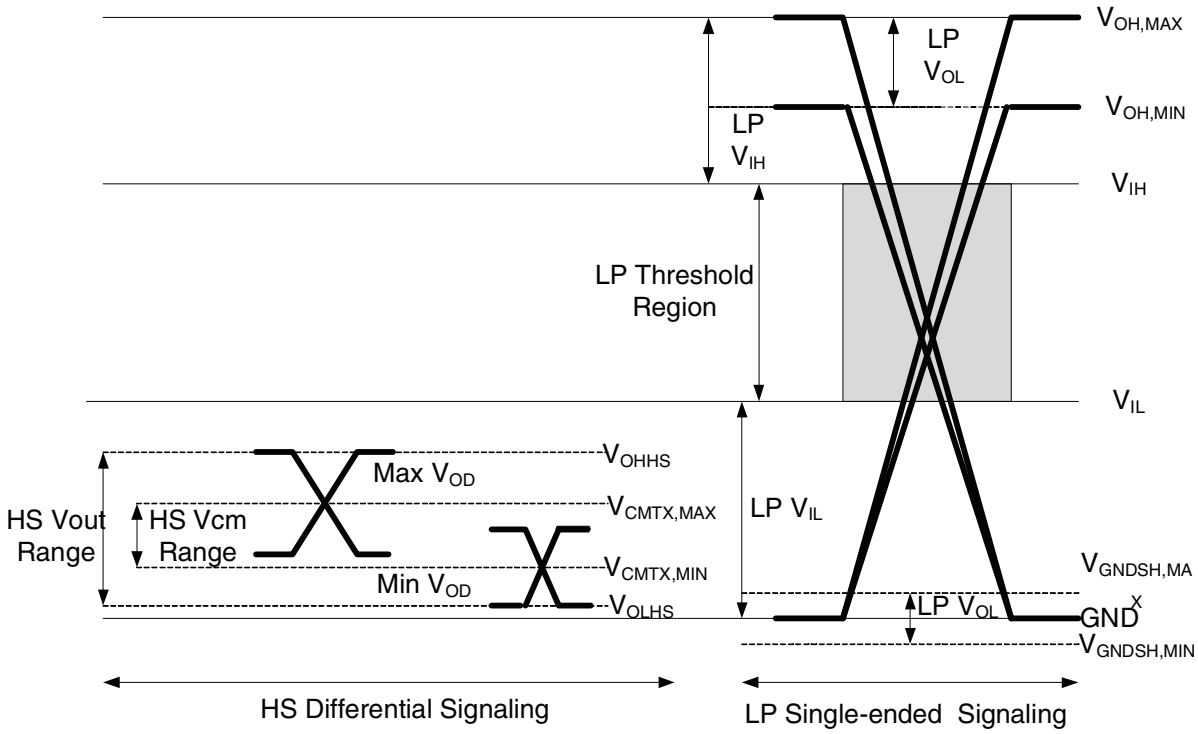

Figure 71. D-PHY Signaling Levels

4.11.12.3 MIPI HS Line Driver Characteristics

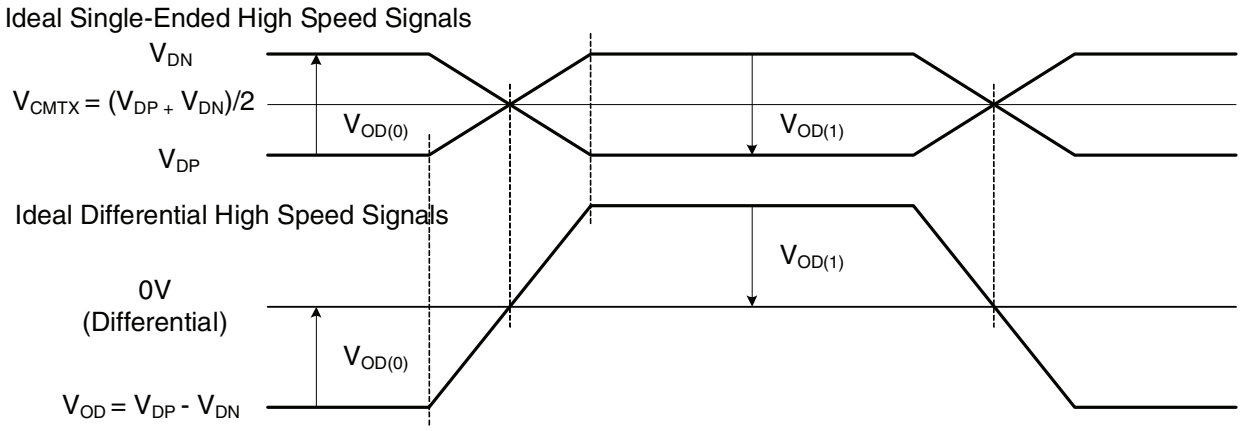

Figure 72. Ideal Single-ended and Resulting Differential HS Signals

Table 76. Electrical and Timing Information

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
$\Delta V_{CMTX(LF)}$	Common level variation between 50 MHz and 450 MHz.	80 Ω<= RL< = 125 Ω			25	mV_p
LP Line Drivers AC Specifications						
t_{rlp}, t_{flp}	Single ended output rise/fall time	15% to 85%, C_L<70 pF			25	ns
t_{reo}		30% to 85%, C_L<70 pF			35	ns
$\delta V/\delta t_{SR}$	Signal slew rate	15% to 85%, C_L<70 pF			120	mV/ns
C_L	Load capacitance		0		70	pF
HS Line Receiver AC Specifications						
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz				200	mVpp
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 MHz and 450 MHz.		-50		50	mVpp
C_{CM}	Common mode termination				60	pF
LP Line Receiver AC Specifications						
e_{SPIKE}	Input pulse rejection				300	Vps
T_{MIN}	Minimum pulse response		50			ns
V_{INT}	Pk-to-Pk interference voltage				400	mV
f_{INT}	Interference frequency		450			MHz
Model Parameters used for Driver Load switching performance evaluation						
C_{PAD}	Equivalent Single ended I/O PAD capacitance.				1	pF
C_{PIN}	Equivalent Single ended Package + PCB capacitance.				2	pF
L_S	Equivalent wire bond series inductance				1.5	nH
R_S	Equivalent wire bond series resistance				0.15	Ω
R_L	Load resistance		80	100	125	Ω

4.11.12.6 High-Speed Clock Timing

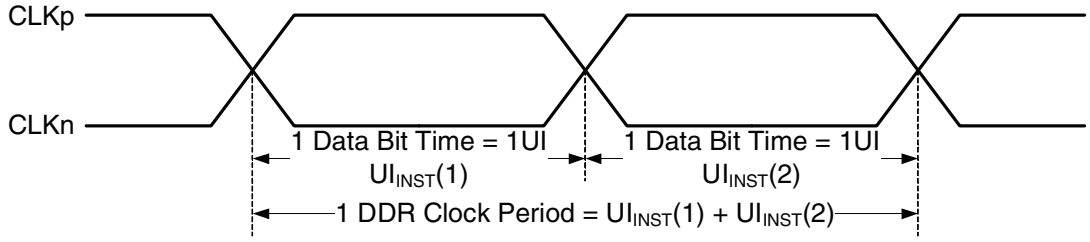

Figure 74. DDR Clock Definition

4.11.14 MediaLB (MLB) Characteristics

4.11.14.1 MediaLB (MLB) DC Characteristics

Table 78 lists the MediaLB 3-pin interface electrical characteristics.

Table 78. MediaLB 3-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum input voltage	—	—	—	3.6	V
Low level input threshold	V_{IL}	—	—	0.7	V
High level input threshold	V_{IH}	See Note[1]	1.8	—	V
Low level output threshold	V_{OL}	I_{OL} = 6 mA	—	0.4	V
High level output threshold	V_{OH}	I_{OH} = -6 mA	2.0	—	V
Input leakage current	I_L	$0 < V_{in} < VDD$	—	±10	µA

1 Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

Table 79 lists the MediaLB 6-pin interface electrical characteristics.

Table 79. MediaLB 6-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Driver Characteristics					
Differential output voltage (steady-state): $\lvert V_{O+} - V_{O-} \rvert$	V_{OD}	See Note[1]	300	500	mV
Difference in differential output voltage between (high/low) steady-states: $\lvert V_{OD, high} - V_{OD, low} \rvert$	ΔV_{OD}	—	-50	50	mV
Common-mode output voltage: $(V_{O+} - V_{O-}) / 2$	V_{OCM}	—	1.0	1.5	V
Difference in common-mode output between (high/low) steady-states: $\lvert V_{OCM, high} - V_{OCM, low} \rvert$	ΔV_{OCM}	—	-50	50	mV
Variations on common-mode output during a logic state transitions	V_{CMV}	See Note[2]	—	150	mVpp
Short circuit current	$\lvert I_{OS} \rvert$	See Note[3]	—	43	mA
Differential output impedance	Z_O	—	1.6	—	kΩ
Receiver Characteristics					

Table 101. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
DISP0_DAT3	P21	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[24]	Input	100 kΩ pull-up
DISP0_DAT4	P20	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[25]	Input	100 kΩ pull-up
DISP0_DAT5	R25	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[26]	Input	100 kΩ pull-up
DISP0_DAT6	R23	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[27]	Input	100 kΩ pull-up
DISP0_DAT7	R24	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[28]	Input	100 kΩ pull-up
DISP0_DAT8	R22	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[29]	Input	100 kΩ pull-up
DISP0_DAT9	T25	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[30]	Input	100 kΩ pull-up
DRAM_A0	AC14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[0]	Output	Low
DRAM_A1	AB14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[1]	Output	Low
DRAM_A10	AA15	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[10]	Output	Low
DRAM_A11	AC12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[11]	Output	Low
DRAM_A12	AD12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[12]	Output	Low
DRAM_A13	AC17	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[13]	Output	Low
DRAM_A14	AA12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[14]	Output	Low
DRAM_A15	Y12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[15]	Output	Low
DRAM_A2	AA14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[2]	Output	Low
DRAM_A3	Y14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[3]	Output	Low
DRAM_A4	W14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[4]	Output	Low
DRAM_A5	AE13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[5]	Output	Low
DRAM_A6	AC13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[6]	Output	Low
DRAM_A7	Y13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[7]	Output	Low
DRAM_A8	AB13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[8]	Output	Low
DRAM_A9	AE12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[9]	Output	Low
DRAM_CAS	AE16	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_CAS	Output	Low
DRAM_CS0	Y16	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_CS[0]	Output	Low
DRAM_CS1	AD17	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_CS[1]	Output	Low
DRAM_D0	AD2	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[0]	Input	100 kΩ pull-up
DRAM_D1	AE2	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[1]	Input	100 kΩ pull-up
DRAM_D10	AA6	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[10]	Input	100 kΩ pull-up
DRAM_D11	AE7	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[11]	Input	100 kΩ pull-up

Table 101. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
DRAM_D12	AB5	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[12]	Input	100 kΩ pull-up
DRAM_D13	AC5	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[13]	Input	100 kΩ pull-up
DRAM_D14	AB6	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[14]	Input	100 kΩ pull-up
DRAM_D15	AC7	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[15]	Input	100 kΩ pull-up
DRAM_D16	AB7	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[16]	Input	100 kΩ pull-up
DRAM_D17	AA8	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[17]	Input	100 kΩ pull-up
DRAM_D18	AB9	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[18]	Input	100 kΩ pull-up
DRAM_D19	Y9	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[19]	Input	100 kΩ pull-up
DRAM_D2	AC4	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[2]	Input	100 kΩ pull-up
DRAM_D20	Y7	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[20]	Input	100 kΩ pull-up
DRAM_D21	Y8	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[21]	Input	100 kΩ pull-up
DRAM_D22	AC8	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[22]	Input	100 kΩ pull-up
DRAM_D23	AA9	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[23]	Input	100 kΩ pull-up
DRAM_D24	AE9	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[24]	Input	100 kΩ pull-up
DRAM_D25	Y10	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[25]	Input	100 kΩ pull-up
DRAM_D26	AE11	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[26]	Input	100 kΩ pull-up
DRAM_D27	AB11	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[27]	Input	100 kΩ pull-up
DRAM_D28	AC9	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[28]	Input	100 kΩ pull-up
DRAM_D29	AD9	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[29]	Input	100 kΩ pull-up
DRAM_D3	AA5	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[3]	Input	100 kΩ pull-up
DRAM_D30	AD11	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[30]	Input	100 kΩ pull-up
DRAM_D31	AC11	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[31]	Input	100 kΩ pull-up
DRAM_D32	AA17	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[32]	Input	100 kΩ pull-up
DRAM_D33	AA18	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[33]	Input	100 kΩ pull-up
DRAM_D34	AC18	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[34]	Input	100 kΩ pull-up
DRAM_D35	AE19	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[35]	Input	100 kΩ pull-up
DRAM_D36	Y17	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[36]	Input	100 kΩ pull-up
DRAM_D37	Y18	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[37]	Input	100 kΩ pull-up
DRAM_D38	AB19	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[38]	Input	100 kΩ pull-up
DRAM_D39	AC19	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[39]	Input	100 kΩ pull-up

Table 101. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
EIM_D19	G21	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[19]	Input	100 kΩ pull-up
EIM_D20	G20	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[20]	Input	100 kΩ pull-up
EIM_D21	H20	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[21]	Input	100 kΩ pull-up
EIM_D22	E23	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[22]	Input	100 kΩ pull-down
EIM_D23	D25	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[23]	Input	100 kΩ pull-up
EIM_D24	F22	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[24]	Input	100 kΩ pull-up
EIM_D25	G22	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[25]	Input	100 kΩ pull-up
EIM_D26	E24	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[26]	Input	100 kΩ pull-up
EIM_D27	E25	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[27]	Input	100 kΩ pull-up
EIM_D28	G23	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[28]	Input	100 kΩ pull-up
EIM_D29	J19	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[29]	Input	100 kΩ pull-up
EIM_D30	J20	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[30]	Input	100 kΩ pull-up
EIM_D31	H21	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[31]	Input	100 kΩ pull-down
EIM_DA0	L20	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[0]	Input	100 kΩ pull-up
EIM_DA1	J25	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[1]	Input	100 kΩ pull-up
EIM_DA10	M22	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[10]	Input	100 kΩ pull-up
EIM_DA11	M20	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[11]	Input	100 kΩ pull-up
EIM_DA12	M24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[12]	Input	100 kΩ pull-up
EIM_DA13	M23	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[13]	Input	100 kΩ pull-up
EIM_DA14	N23	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[14]	Input	100 kΩ pull-up
EIM_DA15	N24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[15]	Input	100 kΩ pull-up
EIM_DA2	L21	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[2]	Input	100 kΩ pull-up
EIM_DA3	K24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[3]	Input	100 kΩ pull-up
EIM_DA4	L22	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[4]	Input	100 kΩ pull-up
EIM_DA5	L23	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[5]	Input	100 kΩ pull-up
EIM_DA6	K25	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[6]	Input	100 kΩ pull-up
EIM_DA7	L25	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[7]	Input	100 kΩ pull-up
EIM_DA8	L24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[8]	Input	100 kΩ pull-up
EIM_DA9	M21	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[9]	Input	100 kΩ pull-up
EIM_EB0	K21	NVCC_EIM	GPIO	ALT0	weim.WEIM_EB[0]	Output	High

Table 101. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
NANDF_D2	F16	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[2]	Input	100 kΩ pull-up
NANDF_D3	D17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[3]	Input	100 kΩ pull-up
NANDF_D4	A19	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[4]	Input	100 kΩ pull-up
NANDF_D5	B18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[5]	Input	100 kΩ pull-up
NANDF_D6	E17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[6]	Input	100 kΩ pull-up
NANDF_D7	C18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[7]	Input	100 kΩ pull-up
NANDF_RB0	B16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[10]	Input	100 kΩ pull-up
NANDF_WP_B	E15	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[9]	Input	100 kΩ pull-up
ONOFF	D12	VDD_SNVS_IN	GPIO	ALT0	src.RESET_B	Input	100 kΩ pull-up
PCIE_RXM	B1	PCIE_VPH					
PCIE_RXP	B2	PCIE_VPH					
PCIE_TXM	A3	PCIE_VPH					
PCIE_TXP	B3	PCIE_VPH					
PMIC_ON_REQ	D11	VDD_SNVS_IN	GPIO	ALT0	snvs_lp_wrapper.SNVS_WAKEUP_ALARM	Output	Low
PMIC_STBY_REQ	F11	VDD_SNVS_IN	GPIO	ALT0	ccm.PMIC_VSTBY_REQ	Output	Low
POR_B	C11	VDD_SNVS_IN	GPIO	ALT0	src.POR_B	Input	100 kΩ pull-up
RGMII_RD0	C24	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[25]	Input	100 kΩ pull-up
RGMII_RD1	B23	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[27]	Input	100 kΩ pull-up
RGMII_RD2	B24	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[28]	Input	100 kΩ pull-up
RGMII_RD3	D23	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[29]	Input	100 kΩ pull-up
RGMII_RX_CTL	D22	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[24]	Input	100 kΩ pull-down
RGMII_RXC	B25	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[30]	Input	100 kΩ pull-down
RGMII_TD0	C22	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[20]	Input	100 kΩ pull-up
RGMII_TD1	F20	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[21]	Input	100 kΩ pull-up
RGMII_TD2	E21	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[22]	Input	100 kΩ pull-up
RGMII_TD3	A24	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[23]	Input	100 kΩ pull-up
RGMII_TX_CTL	C23	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[26]	Input	100 kΩ pull-down
RGMII_TXC	D21	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[19]	Input	100 kΩ pull-down

Table 102. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

	AE	AD
1	GND	DRAM_D5
2	DRAM_D1	DRAM_D0
3	DRAM_SDQS0	DRAM_SDQS0_B
4	DRAM_D7	GND
5	DRAM_D9	DRAM_D8
6	DRAM_SDQS1_B	DRAM_SDQS1
7	DRAM_D11	GND
8	DRAM_SDQS2_B	DRAM_SDQS2
9	DRAM_D24	DRAM_D29
10	DRAM_DQM3	GND
11	DRAM_D26	DRAM_D30
12	DRAM_A9	DRAM_A12
13	DRAM_A5	GND
14	DRAM_SDCLK_1_B	DRAM_SDCLK_1
15	DRAM_SDCLK_0_B	DRAM_SDCLK_0
16	DRAM_CAS	GND
17	ZQPAD	DRAM_CS1
18	NC	NC
19	NC	GND
20	NC	NC
21	NC	NC
22	NC	GND
23	NC	NC
24	NC	NC
25	GND	NC
	AE	AD

Table 103 shows the 21 x 21 mm, 0.8 mm pitch ball map for the i.MX 6DualLite.

Table 103. 21 x 21 mm, 0.8 mm Pitch Ball Map

	D	C	B	A	
1	CSI_D1M	GND	PCIE_RXM	NC	1
2	CSI_D1P	JTAG_TRSTB	PCIE_RXP	PCIE_REXT	2
3	GND	JTAG_TMS	PCIE_TXP	PCIE_TXM	3
4	CSI_REXT	GND	GND	GND	4
5	CLK2_P	CLK2_N	VDD_FA	FA_ANA	5
6	GND	GND	USB_OTG_DN	USB_OTG_DP	6
7	CLK1_P	CLK1_N	XTALO	XTALI	7
8	GND	GPANAIO	USB_OTG_CHD_B	GND	8
9	RTC_XTALI	RTC_XTALO	MLB_SP	MLB_SN	9
10	USB_H1_VBUS	GND	MLB_DN	MLB_DP	10
11	PMIC_ON_REQ	POR_B	MLB_CP	MLB_CN	11
12	ONOFF	BOOT_MODE0	NC	NC	12
13	SD3_DAT4	SD3_DAT5	SD3_CMD	GND	13
14	SD3_CLK	NC	NC	NC	14
15	SD3_RST	NANDF_CLE	SD3_DAT3	SD3_DAT2	15
16	NANDF_CS3	NANDF_CS1	NANDF_RB0	NANDF_ALE	16
17	NANDF_D3	NANDF_D1	SD4_CMD	NANDF_CS2	17
18	SD4_DAT0	NANDF_D7	NANDF_D5	NANDF_D0	18
19	SD4_DAT7	SD4_DAT5	SD4_DAT1	NANDF_D4	19
20	SD1_CLK	SD1_DAT1	SD4_DAT6	SD4_DAT3	20
21	RGMII_TXC	SD2_CLK	SD1_CMD	SD1_DAT0	21
22	RGMII_RX_CTL	RGMII_TD0	SD2_DAT3	SD2_DAT0	22
23	RGMII_RD3	RGMII_TX_CTL	RGMII_RD1	SD2_DAT2	23
24	EIM_D18	RGMII_RD0	RGMII_RD2	RGMII_TD3	24
25	EIM_D23	EIM_D16	RGMII_RXC	GND	25
	D	C	B	A	

Table 103. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

M	L	K	J	H	G	F	E
CSI0_DAT10	CSI0_DAT13	HDMI_HPD	HDMI_REF	DSI_D1P	DSI_D0P	NC	NC
CSI0_DAT12	GND	HDMI_DDCCEC	GND	DSI_D1M	DSI_D0M	NC	NC
CSI0_DAT11	CSI0_DAT17	HDMI_D2M	HDMI_D1M	DSI_CLK0M	GND	CSI_CLK0P	CSI_D0P
CSI0_DAT14	CSI0_DAT16	HDMI_D2P	HDMI_D1P	DSI_CLK0P	DSI_REXT	CSI_CLK0M	CSI_D0M
CSI0_DAT15	GND	HDMI_D0M	HDMI_CLKM	JTAG_TCK	JTAG_TDI	GND	GND
CSI0_DAT18	CSI0_DAT19	HDMI_D0P	HDMI_CLKP	JTAG_MOD	JTAG_TDO	GND	GND
HDMI_VPH	HDMI_VP	NVCC_MIPI	NVCC_JTAG	PCIE_VP	PCIE_VPH	GND	GND
GND	GND	GND	GND	GND	PCIE_VPTX	GND	NVCC_PLL_OUT
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDHIGH_IN	VDDHIGH_IN	VDD_SNVS_CAP	VDDUSB_CAP	USB_OTG_VBUS
GND	GND	GND	VDDHIGH_CAP	VDDHIGH_CAP	GND	USB_H1_DN	USB_H1_DP
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDD_SNVS_IN	PMIC_STBY_REQ	TAMPER
GND	GND	GND	GND	GND	NC	BOOT_MODE1	TEST_MODE
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	NC	SD3_DAT7	SD3_DAT6
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	NVCC_SD3	SD3_DAT1	SD3_DAT0
GND	GND	GND	GND	GND	NVCC_NANDF	NANDF_CS0	NANDF_WP_B
VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	NVCC_SD1	NANDF_D2	SD4_CLK
VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	NVCC_SD2	SD4_DAT2	NANDF_D6
GND	GND	GND	GND	GND	NVCC_RGMII	SD1_DAT3	SD4_DAT4
NVCC_EIM	NVCC_EIM	NVCC_EIM	EIM_D29	EIM_A25	GND	SD2_CMD	SD1_DAT2
EIM_DA11	EIM_DA0	EIM_RW	EIM_D30	EIM_D21	EIM_D20	RGMII_TD1	SD2_DAT1
EIM_DA9	EIM_DA2	EIM_EB0	EIM_A23	EIM_D31	EIM_D19	EIM_D17	RGMII_TD2
EIM_DA10	EIM_DA4	EIM_LBA	EIM_A18	EIM_A20	EIM_D25	EIM_D24	EIM_EB2
EIM_DA13	EIM_DA5	EIM_EB1	EIM_CS1	EIM_A21	EIM_D28	EIM_EB3	EIM_D22
EIM_DA12	EIM_DA8	EIM_DA3	EIM_OE	EIM_CS0	EIM_A17	EIM_A22	EIM_D26
EIM_WAIT	EIM_DA7	EIM_DA6	EIM_DA1	EIM_A16	EIM_A19	EIM_A24	EIM_D27
M	L	K	J	H	G	F	E

Table 103. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

Y	W	V	U	T	R	P	N
LVDS1_TX0_N	LVDS0_TX3_P	LVDS0_TX2_P	LVDS0_TX0_P	GPIO_2	GPIO_17	CSI0_PIXCLK	CSI0_DAT4
LVDS1_TX0_P	LVDS0_TX3_N	LVDS0_TX2_N	LVDS0_TX0_N	GPIO_9	GPIO_16	CSI0_DAT5	CSI0_VSYNC
LVDS1_CLK_N	GND	LVDS0_CLK_P	LVDS0_TX1_P	GPIO_6	GPIO_7	CSI0_DATA_EN	CSI0_DAT7
LVDS1_CLK_P	KEY_ROW2	LVDS0_CLK_N	LVDS0_TX1_N	GPIO_1	GPIO_5	CSI0_MCLK	CSI0_DAT6
GND	KEY_COL0	KEY_ROW4	KEY_COL3	GPIO_0	GPIO_8	GPIO_19	CSI0_DAT9
DRAM_RESET	KEY_COL2	KEY_ROW0	KEY_ROW1	KEY_COL4	GPIO_4	GPIO_18	CSI0_DAT8
DRAM_D20	GND	NVCC_LVDS2P5	KEY_COL1	KEY_ROW3	GPIO_3	NVCC_GPIO	NVCC_CSI
DRAM_D21	GND	GND	GND	GND	GND	GND	GND
DRAM_D19	GND	NVCC_DRAM	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN
DRAM_D25	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDSOC_CAP	GND	GND
DRAM_SDCKE0	GND	NVCC_DRAM	GND	GND	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
DRAM_A15	GND	NVCC_DRAM	GND	GND	GND	GND	NC
DRAM_A7	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
DRAM_A3	DRAM_A4	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_IN	VDDARM_IN	VDDARM_IN
DRAM_SDBA1	GND	NVCC_DRAM	GND	GND	GND	GND	GND
DRAM_CS0	GND	NVCC_DRAM	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN
DRAM_D36	GND	NVCC_DRAM	GND	GND	GND	VDDPU_CAP	VDDPU_CAP
DRAM_D37	GND	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	GND	GND
DRAM_D40	GND	GND	GND	GND	NVCC_ENET	NVCC_LCD	DI0_DISP_CLK
DRAM_D44	ENET_TXD1	ENET_MDC	ENET_TXD0	DISP0_DAT21	DISP0_DAT13	DISP0_DAT4	DI0_PIN3
DRAM_DQM7	ENET_RXD0	ENET_TX_EN	ENET_CRS_DV	DISP0_DAT16	DISP0_DAT10	DISP0_DAT3	DI0_PIN15
DRAM_D59	ENET_RXD1	ENET_REF_CLK	DISP0_DAT20	DISP0_DAT15	DISP0_DAT8	DISP0_DAT1	EIM_BCLK
DRAM_D62	ENET_RX_ER	ENET_MDIO	DISP0_DAT19	DISP0_DAT11	DISP0_DAT6	DISP0_DAT2	EIM_DA14
GND	DISP0_DAT23	DISP0_DAT22	DISP0_DAT17	DISP0_DAT12	DISP0_DAT7	DISP0_DAT0	EIM_DA15
DRAM_D58	DRAM_D63	DISP0_DAT18	DISP0_DAT14	DISP0_DAT9	DISP0_DAT5	DI0_PIN4	DI0_PIN2
Y	W	V	U	T	R	P	N

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Document Number: IMX6SDLAEC
Rev. 1
11/2012