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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx6s6avm08ab

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CCM GPC SRC	Clock Control Module, Global Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSI	MIPI CSI-2 i/f	Multimedia Peripherals	The CSI IP provides MIPI CSI-2 standard camera interface port. The CSI-2 interface supports from 80 Mbps to 1 Gbps speed per data lane.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6Solo/6DualLite platform.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCIC-0 DCIC-1	Display Content Integrity Checker	Automotive IP	The DCIC provides integrity check on portion(s) of the display. Each i.MX 6Solo/6DualLite processor has two such modules.
DSI	MIPI DSI i/f	Multimedia Peripherals	The MIPI DSI IP provides DSI standard display port interface. The DSI interface support 80 Mbps to 1 Gbps speed per data lane.
DTCP	DTCP	Multimedia Peripherals	Provides encryption function according to Digital Transmission Content Protection standard for traffic over MLB150.
eCSPI1-4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
VPU	Video Processing Unit	Multimedia Peripherals	A high-performing video processing unit (VPU), which covers many SD-level and HD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing, such as rotation and mirroring. See the i.*MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for complete list of VPU's decoding/encoding capabilities.
WDOG-1	Watch Dog	Timer Peripherals	The Watch Dog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watch Dog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW.
WEIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The WEIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
XTALOSC	Crystal Oscillator I/F	Clocks, Resets, and Power Control	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator to provide USB required frequency.

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6Solo/6DualLite processors.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 6Solo/6DualLite Chip-Level Conditions

For these characteristics, …	Topic appears …
Absolute Maximum Ratings	on page 22
BGA Case 2240 Package Thermal Resistance	on page 23
Operating Ranges	on page 24
External Clock Sources	on page 26
Maximal Supply Currents	on page 27
Low Power Mode Supply Currents	on page 29
USB PHY Current Consumption	on page 30
PCIe 2.0 Power Consumption	on page 30

4.1.1 Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core supply voltages	VDDARM_IN VDDSOC_IN	-0.3	1.5	V
Internal supply voltages	VDDARM_CAP VDDSOC_CAP VDDPU_CAP	-0.3	1.3	V
GPIO supply voltage	Supplies denoted as I/O supply	-0.5	3.6	V
DDR I/O supply voltage	Supplies denoted as I/O supply	-0.4	1.975	V
MLB I/O supply voltage	Supplies denoted as I/O supply	-0.3	2.8	V
LVDS I/O supply voltage	Supplies denoted as I/O supply	-0.3	2.8	V
VDD_SNVS_IN supply voltage	VDD_SNVS_IN	-0.3	3.3	V
VDDHIGH_IN supply voltage	VDDHIGH_IN	-0.3	3.6	V
USB VBUS	VBUS	—	5.25	V
Input voltage on USB_OTG_DP, USB_OTG_DN, USB_H1_DP, USB_H1_DN pins	USB_DP/USB_DN	-0.3	3.63	V
Input/output voltage range	V_{in}/V_{out}	-0.5	OVDD[1]+0.3	V

Table 27 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 27. LVDS I/O DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Differential Voltage	VOD	Rload-100 Ω Diff	250	350	450	mV
Output High Voltage	VOH	IOH = 0 mA	1.25	1.375	1.6	V
Output Low Voltage	VOL	IOL = 0 mA	0.9	1.025	1.25	V
Offset Voltage	VOS		1.125	1.2	1.375	V

4.6.4 MLB I/O DC Parameters

The MLB interface complies with Analog Interface of 6-pin differential Media Local Bus specification version 4.1. See 6-pin differential MLB specification v4.1, “MediaLB 6-pin interface Electrical Characteristics” for details.

NOTE

The MLB 6-pin interface does not support speed mode 8192 fs.

Table 28 shows the Media Local Bus (MLB) I/O DC parameters.

Table 28. MLB I/O DC Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Differential Voltage	VOD	Rload-50Ω Diff	300	500	mV
Output High Voltage	VOH	Rload-50Ω Diff	1.25	1.75	V
Output Low Voltage	VOL	Rload-50Ω Diff	0.75	1.25	V
Common-mode output voltage ((Vpadp*+Vpadn*)/2)	Vocm	Rload-50Ω Diff	1	1.5	V
Differential output impedance	Zo		1.6		kΩ

4.7 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O
- MLB I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 4 and Figure 5.

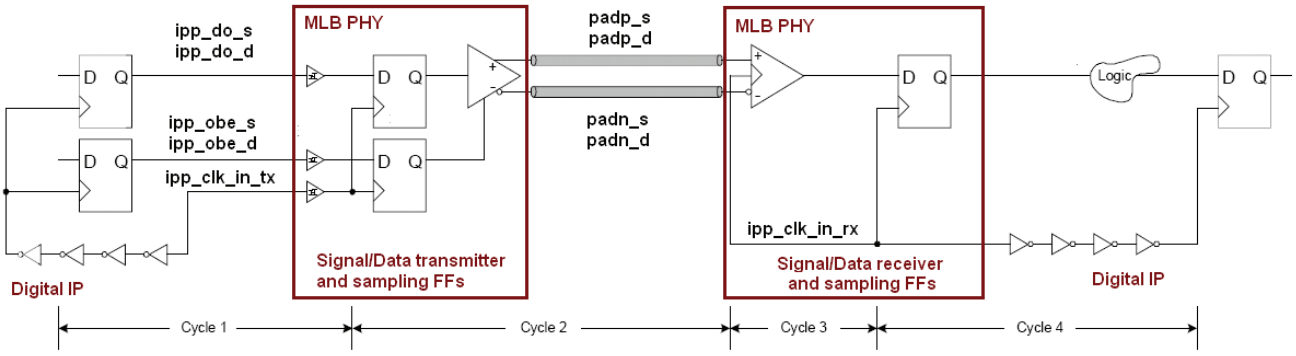


Figure 8. MLB 6-Pin Pipeline Diagram

Table 34 shows the AC parameters for MLB I/O.

Table 34. I/O AC Parameters of MLB PHY

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential pulse skew[1]	t_{SKD}	Rload = 50 Ω between padp and padn	—	—	0.1	ns
Transition Low to High Time[2]	t_{TLH}		—	—	1	
Transition High to Low Time	t_{THL}		—	—	1	
MLB external clock Operating Frequency	fclk_ext	—	—	—	102.4	MHz
MLB PLL clock Operating Frequency	fclk_pll	—	—	—	307.2	MHz

1 t_{SKD} = | t_{PHLD} - t_{PLHD} |, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

2 Measurement levels are 20-80% from output voltage.

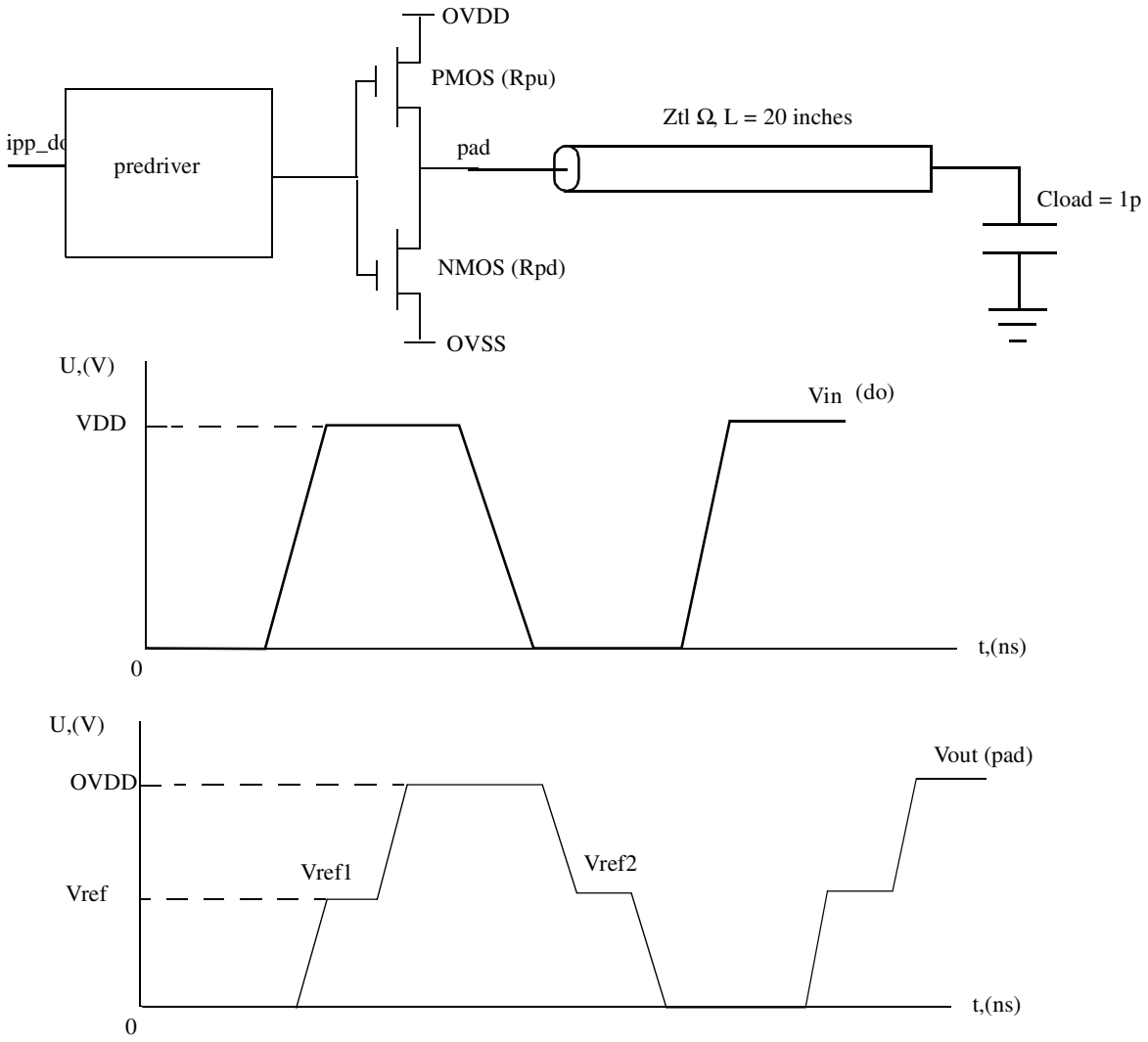
4.8 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters of the i.MX 6Solo/6DualLite processors for the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2, and DDR3/DDR3L modes
- LVDS I/O
- MLB I/O

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 9).



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 9. Impedance Matching Load for Measurement

Table 43. EIM Bus Timing Parameters (continued)[1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE19	Input Data hold time from Clock rise	2	—	2	—	—	—	—	—
WE20	WAIT_B setup time to Clock rise	2	—	4	—	—	—	—	—
WE21	WAIT_B hold time from Clock rise	2	—	2	—	—	—	—	—

1 t is the maximal EIM logic (axi_clk) cycle time. The maximum allowed axi_clk frequency depends on the fixed/non-fixed latency configuration, whereas the maximum allowed BCLK frequency is:

—Fixed latency for both read and write is 132 MHz.

—Variable latency for read only is 132 MHz.

—Variable latency for write only is 52 MHz.

In variable latency configuration for write, if BCD = 0 & WBCDD = 1 or BCD = 1, axi_clk must be 104 MHz.Write BCD = 1 and 104 MHz axi_clk, will result in a BCLK of 52 MHz. When the clock branch to EIM is decreased to 104 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for a detailed clock tree description.

2 BCLK parameters are being measured from the 50% point, that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

3 For signal measurements, “High” is defined as 80% of signal value and “Low” is defined as 20% of signal value.

Figure 14 to Figure 17 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

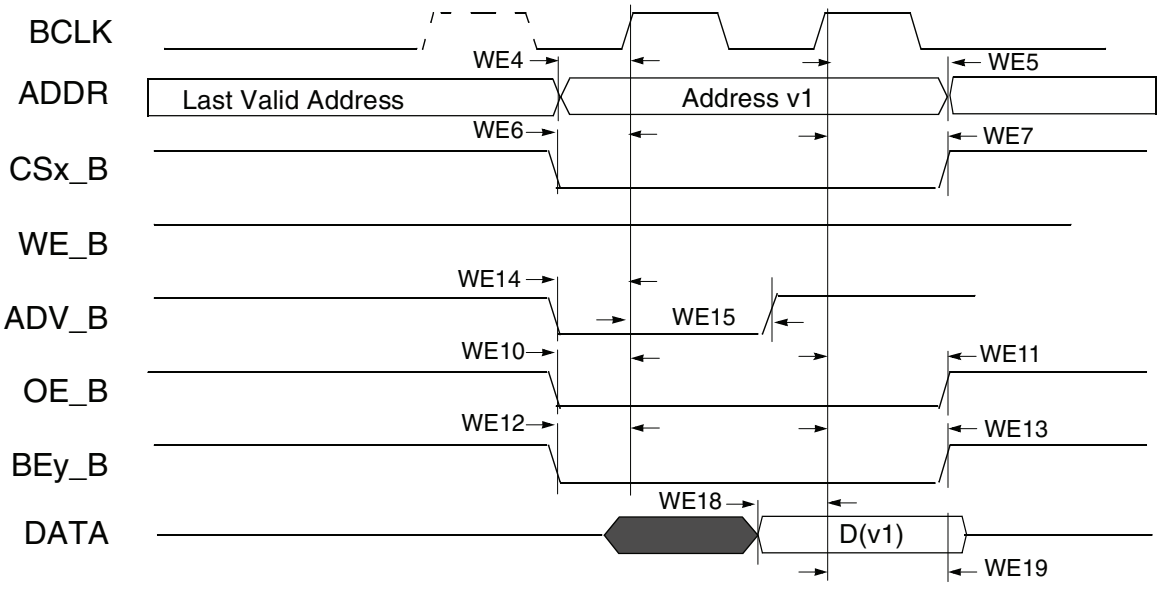


Figure 14. Synchronous Memory Read Access, WSC=1

4.9.4.2 LPDDR2 Parameters

Figure 27 shows the basic timing parameters. The timing parameters for this diagram appear in Table 48.

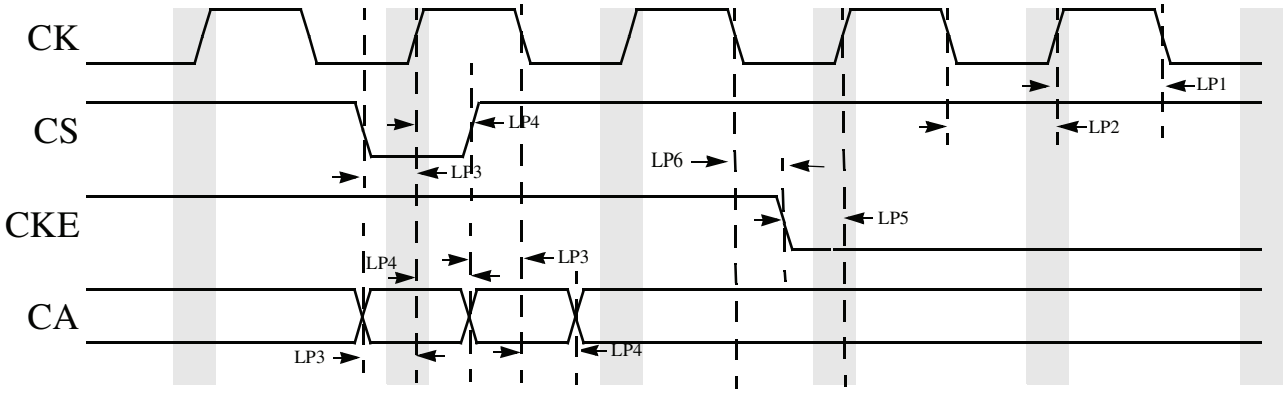


Figure 27. LPDDR2 Command and Address Timing Parameters

Table 48. LPDDR2 Timing Parameter

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP1	SDRAM clock high-level width	t_{CH}	0.45	0.55	t_{CK}
LP2	SDRAM clock low-level width	t_{CL}	0.45	0.55	t_{CK}
LP3	CA, CS setup time	t_{IS}	380	—	ps
LP4	CA, CS hold time	t_{IH}	380	—	ps
LP5	CKE setup time	t_{ISCKE}	770	—	tck
LP6	CKE hold time	t_{IHCKE}	770	—	tck

1 All measurements are in reference to Vref level.

2 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 29 shows the read timing parameters. The timing parameters for this diagram appear in Table 50.

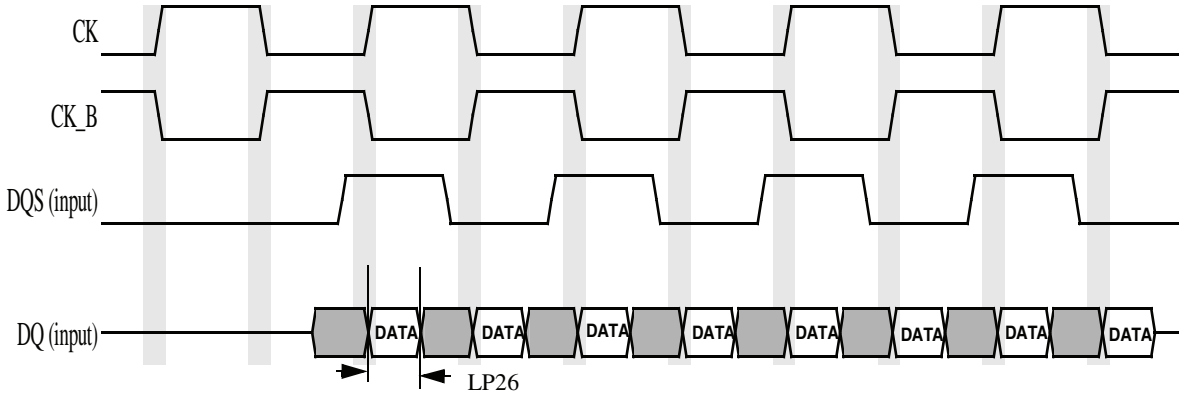


Figure 29. LPDDR2 Read Cycle

Table 50. LPDDR2 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP26	Minimum required DQ valid window width for LPDDR2	—	270	—	ps

1 To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

2 All measurements are in reference to Vref level.

3 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

4.10 General-Purpose Media Interface (GPMI) Timing

The i.MX 6Solo/6DualLite GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous timing mode, Source Synchronous timing mode and Samsung Toggle timing mode separately described in the following subsections.

4.10.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The maximum I/O speed of GPMI in asynchronous mode is about 50 MB/s. Figure 30 through Figure 33 depicts the relative timing between GPMI signals at the module level for different operations under asynchronous mode. Table 51 describes the timing parameters (NF1–NF17) that are shown in the figures.

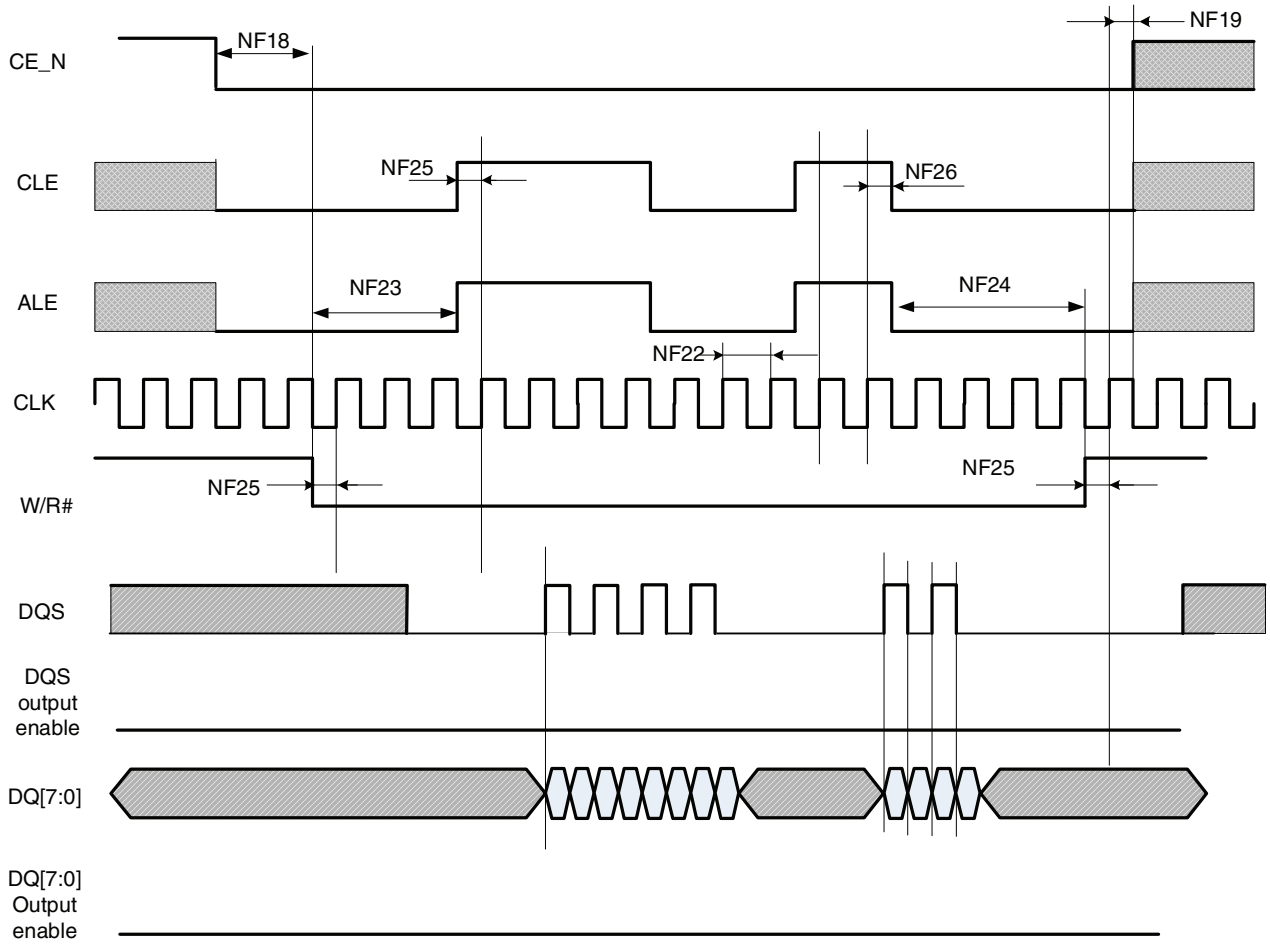


Figure 36. Source Synchronous Mode Data Read Timing Diagram

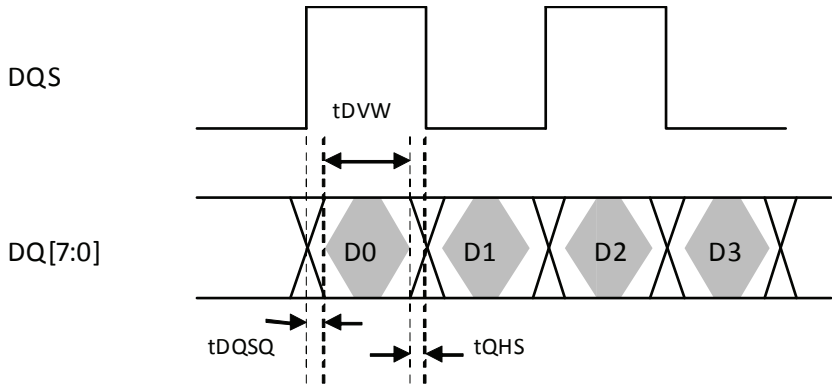


Figure 37. DQS/DQ Read Valid Window

Table 52. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	tCE	CE_DELAY x tCK	—	ns
NF19	CE# hold time	tCH	0.5 x tCK	—	ns
NF20	Command/address DQ setup time	tCAS	0.5 x tCK	—	ns
NF21	Command/address DQ hold time	tCAH	0.5 x tCK	—	ns
NF22	clock period	tCK	5	--	ns
NF23	preamble delay	tPRE	PRE_DELAY x tCK	—	ns
NF24	postamble delay	tPOST	POST_DELAY x tCK	—	ns
NF25	CLE and ALE setup time	tCALS	0.5 x tCK	—	ns
NF26	CLE and ALE hold time	tCALH	0.5 x tCK	—	ns
NF27	Data input to first DQS latching transition	tDQSS	tCK	—	ns

1 GPMI's Sync Mode output timing could be controlled by module's internal registers, say HW_GPMI_TIMING2_CE_DELAY, HW_GPMI_TIMING_PREAMBLE_DELAY, and HW_GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers' settings. In the above table, we use CE_DELAY/PRE_DELAY/POST_DELAY to represent each of these settings.

For DDR Source sync mode, Figure 37 shows the timing diagram of DQS/DQ read valid window. The typical value of tDQSQ is 0.85ns (max) and 1ns (max) for tQHS at 200MB/s. GPMI will sample DQ[7:0] at both rising and falling edge of an delayed DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET(see the GPMI chapter of the i.MX 6Solo/6DualLite reference manual). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.10.3 Samsung Toggle Mode AC Timing

4.10.3.1 Command and Address Timing

NOTE

Samsung Toggle Mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 4.10.1, "Asynchronous Mode AC Timing (ONFI 1.0 Compatible)," for details.

4.11.2.1 ECSPI Master Mode Timing

Figure 40 depicts the timing of ECSPI in master mode. Table 54 lists the ECSPI master mode timing characteristics.

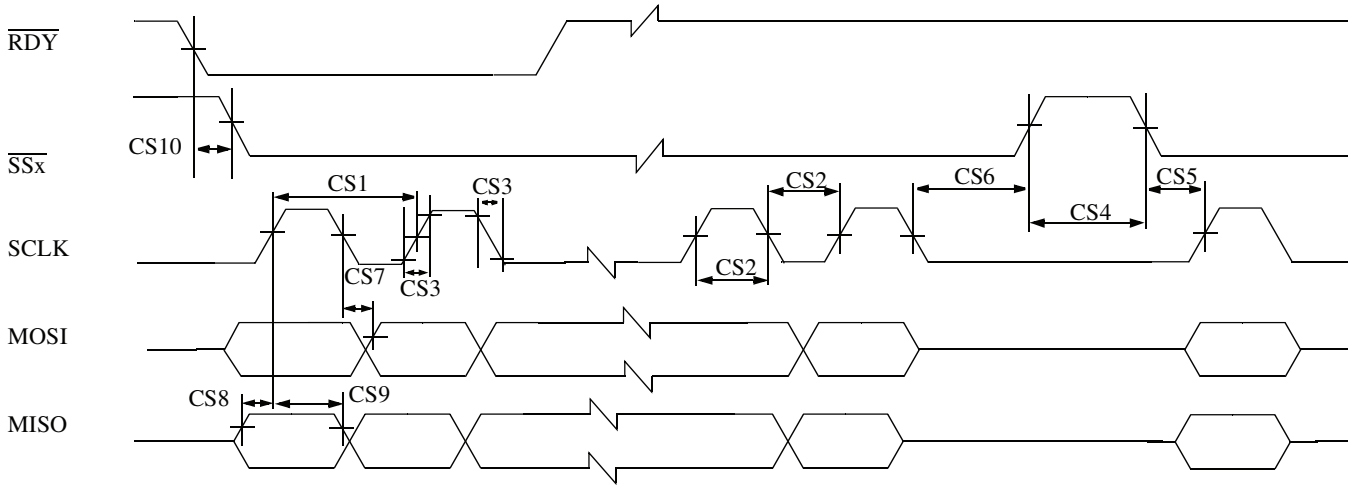


Figure 40. ECSPI Master Mode Timing Diagram

Table 54. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time–Read SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	SCLK High or Low Time–Read SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS3	SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	Half SCLK period - 4	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	Half SCLK period - 2	—	ns
CS7	MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	MISO Setup Time	t_{Smiso}	18	—	ns
CS9	MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to SSx Time[2]	t_{SDRY}	5	—	ns

1 See specific I/O AC parameters Section 4.7, “I/O AC Parameters.”

2 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.11.2.2 ECSPI Slave Mode Timing

Figure 41 depicts the timing of ECSPI in slave mode. Table 55 lists the ECSPI slave mode timing characteristics.

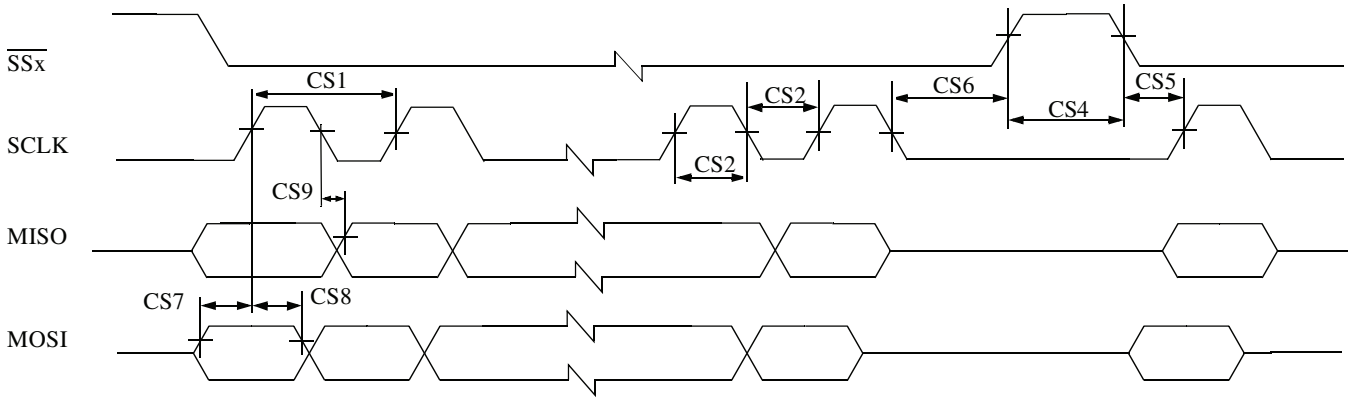


Figure 41. ECSPI Slave Mode Timing Diagram

Table 55. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time–Read SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	SCLK High or Low Time–Read SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	19	ns

Table 57. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	5.6	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.11.4.2 eMMC4.4 (Dual Data Rate) AC Timing

Figure 45 depicts the timing of eMMC4.4. Table 58 lists the eMMC4.4 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

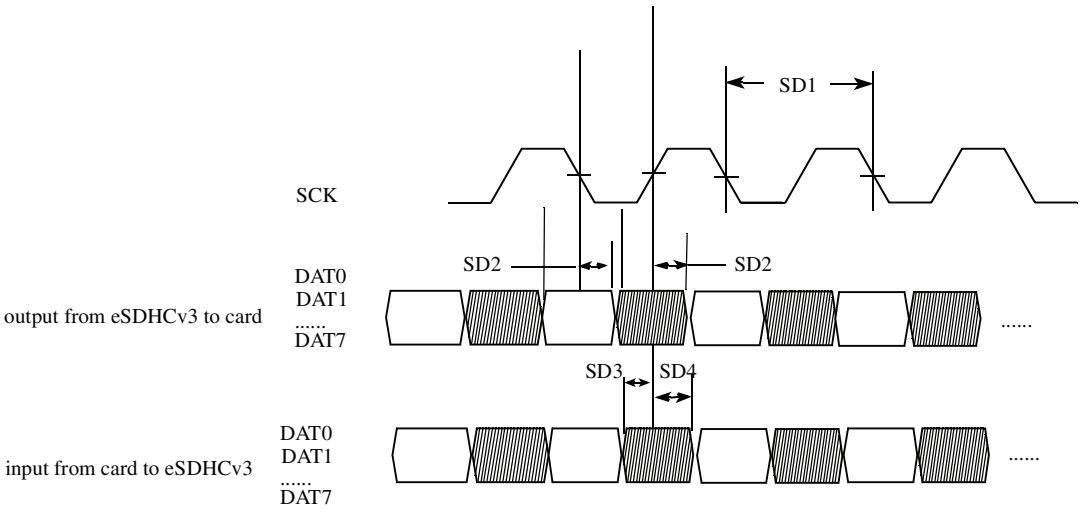


Figure 45. eMMC4.4 Timing

Table 58. eMMC4.4 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (EMMC4.4 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs CMD, DAT (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.5	7.1	ns

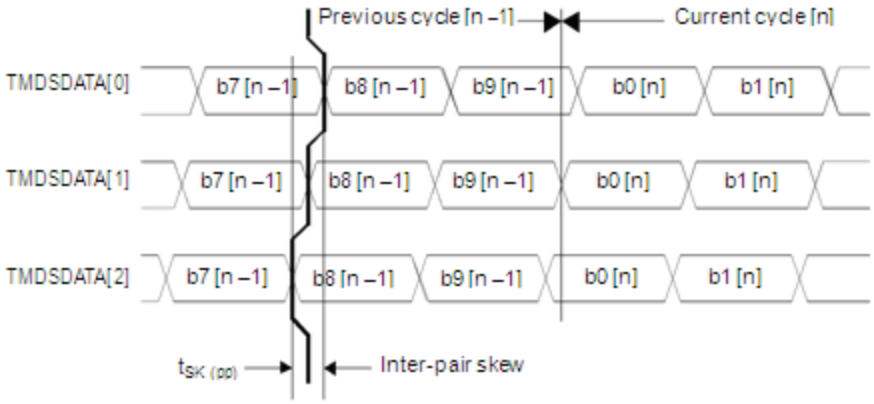


Figure 61. Inter-Pair Skew Definition

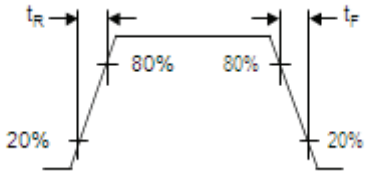


Figure 62. TMDS Output Signals Rise and Fall Time Definition

Table 67. Switching Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
TMDS Drivers Specifications						
—	Maximum serial data rate	—	—	—	3.4	Gbps
$F_{TMDSCLK}$	TMDSCLK frequency	On TMDSCLKP/N outputs	25	—	340	MHz
$P_{TMDSCLK}$	TMDSCLK period	RL = 50 Ω See Figure 58.	2.94	—	40	ns
t_{CDC}	TMDSCLK duty cycle	$t_{CDC} = t_{CPH} / P_{TMDSCLK}$ RL = 50 Ω See Figure 58.	40	50	60	%
t_{CPH}	TMDSCLK high time	RL = 50 Ω See Figure 58.	4	5	6	UI[1]
t_{CPL}	TMDSCLK low time	RL = 50 Ω See Figure 58.	4	5	6	UI[1]
—	TMDSCLK jitter[2]	RL = 50 Ω	—	—	0.25	UI[1]
$t_{SK(p)}$	Intra-pair (pulse) skew	RL = 50 Ω See Figure 60.	—	—	0.15	UI[1]

Table 71. Video Signal Cross-Reference

i.MX 6Solo/6DualLite	LCD							Comment[1]
Port Name (x=0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[2]	16-bit YCrCb	20-bit YCrCb	
DISPx_DAT0	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	The restrictions are as follows: • There are maximal three continuous groups of bits that could be independently mapped to the external bus. Groups should not be overlapped. • The bit order is expressed in each of the bit groups, for example, B[0] = least significant blue pixel bit
DISPx_DAT1	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	
DISPx_DAT2	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	
DISPx_DAT3	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	
DISPx_DAT4	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	
DISPx_DAT5	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	
DISPx_DAT6	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	
DISPx_DAT7	DAT[7]	G[2]	G[1]	B[7]	Y/C[7]	C[7]	C[7]	
DISPx_DAT8	DAT[8]	G[3]	G[2]	G[0]	—	Y[0]	C[8]	
DISPx_DAT9	DAT[9]	G[4]	G[3]	G[1]	—	Y[1]	C[9]	
DISPx_DAT10	DAT[10]	G[5]	G[4]	G[2]	—	Y[2]	Y[0]	
DISPx_DAT11	DAT[11]	R[0]	G[5]	G[3]	—	Y[3]	Y[1]	
DISPx_DAT12	DAT[12]	R[1]	R[0]	G[4]	—	Y[4]	Y[2]	
DISPx_DAT13	DAT[13]	R[2]	R[1]	G[5]	—	Y[5]	Y[3]	
DISPx_DAT14	DAT[14]	R[3]	R[2]	G[6]	—	Y[6]	Y[4]	
DISPx_DAT15	DAT[15]	R[4]	R[3]	G[7]	—	Y[7]	Y[5]	
DISPx_DAT16	DAT[16]	—	R[4]	R[0]	—	—	Y[6]	
DISPx_DAT17	DAT[17]	—	R[5]	R[1]	—	—	Y[7]	
DISPx_DAT18	DAT[18]	—	—	R[2]	—	—	Y[8]	
DISPx_DAT19	DAT[19]	—	—	R[3]	—	—	Y[9]	
DISPx_DAT20	DAT[20]	—	—	R[4]	—	—	—	
DISPx_DAT21	DAT[21]	—	—	R[5]	—	—	—	

Table 76. Electrical and Timing Information

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
$\Delta V_{CMTX(LF)}$	Common level variation between 50 MHz and 450 MHz.	80 Ω<= RL< = 125 Ω			25	mV_p
LP Line Drivers AC Specifications						
t_{rlp}, t_{flp}	Single ended output rise/fall time	15% to 85%, C_L<70 pF			25	ns
t_{reo}		30% to 85%, C_L<70 pF			35	ns
$\delta V/\delta t_{SR}$	Signal slew rate	15% to 85%, C_L<70 pF			120	mV/ns
C_L	Load capacitance		0		70	pF
HS Line Receiver AC Specifications						
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz				200	mVpp
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 MHz and 450 MHz.		-50		50	mVpp
C_{CM}	Common mode termination				60	pF
LP Line Receiver AC Specifications						
e_{SPIKE}	Input pulse rejection				300	Vps
T_{MIN}	Minimum pulse response		50			ns
V_{INT}	Pk-to-Pk interference voltage				400	mV
f_{INT}	Interference frequency		450			MHz
Model Parameters used for Driver Load switching performance evaluation						
C_{PAD}	Equivalent Single ended I/O PAD capacitance.				1	pF
C_{PIN}	Equivalent Single ended Package + PCB capacitance.				2	pF
L_S	Equivalent wire bond series inductance				1.5	nH
R_S	Equivalent wire bond series resistance				0.15	Ω
R_L	Load resistance		80	100	125	Ω

4.11.12.6 High-Speed Clock Timing

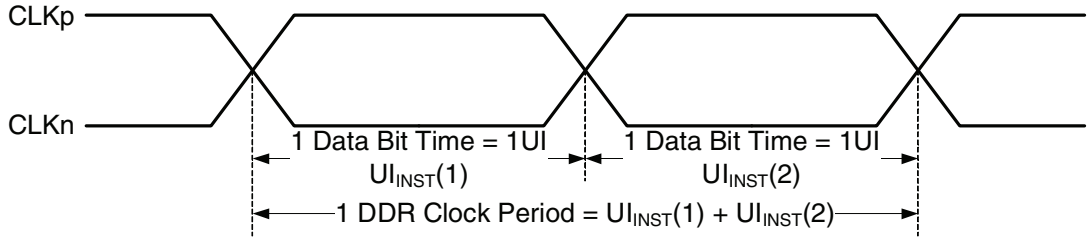


Figure 74. DDR Clock Definition

Table 80. MLB 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK operating frequency[1]	f_{mck}	11.264	25.6	MHz	256xFs at 44.0 kHz 512xFs at 50.0 kHz
MLBCLK rise time	t_{mckr}	—	3	ns	V_{IL} TO V_{IH}
MLBCLK fall time	t_{mckf}	—	3	ns	V_{IH} TO V_{IL}
MLBCLK low time[2]	t_{mckl}	30 14	—	ns	256xFs 512xFs
MLBCLK high time	t_{mckh}	30 14	—	ns	256xFs 512xFs
MLBSIG/MLBDAT receiver input valid to MLBCLK falling	t_{dsmcf}	1	—	ns	—
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	t_{mdzh}	—	ns	—
MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0	t_{mckl}	ns	[3]
Bus Hold from MLBCLK low	t_{mdzh}	4	—	ns	—
MLBSIG/MLBDAT output valid from transition of MLBCLK (low to high)	t_{delay}		10	ns	—

1 The controller can shut off MLBCLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLBCLK.

2 MLBCLK low/high time includes the pulse width variation.

3 The MediaLB driver can release the MLBDAT/MLBSIG line as soon as MLBCLK is low; however, the logic state of the final driven bit on the line must remain on the bus for t_{mdzh}. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Ground = 0.0 V; load capacitance = 40 pF; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed in Table 81; unless otherwise noted.

Table 81. MLB 1024 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK Operating Frequency[1]	f_{mck}	45.056	51.2	MHz	1024xfs at 44.0 kHz 1024xfs at 50.0 kHz
MLBCLK rise time	t_{mckr}	—	1	ns	V_{IL} TO V_{IH}
MLBCLK fall time	t_{mckf}	—	1	ns	V_{IH} TO V_{IL}
MLBCLK low time	t_{mckl}	6.1	—	ns	[2]
MLBCLK high time	t_{mckh}	9.3	—	ns	—
MLBSIG/MLBDAT receiver input valid to MLBCLK falling	t_{dsmcf}	1	—	ns	—
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	t_{mdzh}	—	ns	—

Table 101. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
DRAM_D4	AC1	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[4]	Input	100 kΩ pull-up
DRAM_D40	Y19	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[40]	Input	100 kΩ pull-up
DRAM_D41	AB20	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[41]	Input	100 kΩ pull-up
DRAM_D42	AB21	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[42]	Input	100 kΩ pull-up
DRAM_D43	AD21	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[43]	Input	100 kΩ pull-up
DRAM_D44	Y20	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[44]	Input	100 kΩ pull-up
DRAM_D45	AA20	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[45]	Input	100 kΩ pull-up
DRAM_D46	AE21	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[46]	Input	100 kΩ pull-up
DRAM_D47	AC21	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[47]	Input	100 kΩ pull-up
DRAM_D48	AC22	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[48]	Input	100 kΩ pull-up
DRAM_D49	AE22	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[49]	Input	100 kΩ pull-up
DRAM_D5	AD1	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[5]	Input	100 kΩ pull-up
DRAM_D50	AE24	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[50]	Input	100 kΩ pull-up
DRAM_D51	AC24	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[51]	Input	100 kΩ pull-up
DRAM_D52	AB22	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[52]	Input	100 kΩ pull-up
DRAM_D53	AC23	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[53]	Input	100 kΩ pull-up
DRAM_D54	AD25	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[54]	Input	100 kΩ pull-up
DRAM_D55	AC25	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[55]	Input	100 kΩ pull-up
DRAM_D56	AB25	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[56]	Input	100 kΩ pull-up
DRAM_D57	AA21	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[57]	Input	100 kΩ pull-up
DRAM_D58	Y25	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[58]	Input	100 kΩ pull-up
DRAM_D59	Y22	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[59]	Input	100 kΩ pull-up
DRAM_D6	AB4	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[6]	Input	100 kΩ pull-up
DRAM_D60	AB23	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[60]	Input	100 kΩ pull-up
DRAM_D61	AA23	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[61]	Input	100 kΩ pull-up
DRAM_D62	Y23	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[62]	Input	100 kΩ pull-up
DRAM_D63	W25	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[63]	Input	100 kΩ pull-up
DRAM_D7	AE4	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[7]	Input	100 kΩ pull-up
DRAM_D8	AD5	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[8]	Input	100 kΩ pull-up
DRAM_D9	AE5	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[9]	Input	100 kΩ pull-up

6.1.3 21 x 21 mm, 0.8 mm Pitch Ball Map

Table 102 shows the 21 x 21 mm, 0.8 mm pitch ball map for the i.MX 6Solo.

Table 102. 21 x 21 mm, 0.8 mm Pitch Ball Map

	A	B	C	D	E	F	G
1	NC	PCIE_RXM	GND	CSI_D1M	NC	NC	DSI_D0P
2	PCIE_REXT	PCIE_RXP	JTAG_TRSTB	CSI_D1P	NC	NC	DSI_D0M
3	PCIE_TXM	PCIE_TXP	JTAG_TMS	GND	CSI_D0P	CSI_CLK0P	GND
4	GND	GND	GND	CSI_REXT	CSI_D0M	CSI_CLK0M	DSI_REXT
5	FA_ANA	VDD_FA	CLK2_N	CLK2_P	GND	GND	JTAG_TDI
6	USB_OTG_DP	USB_OTG_DN	GND	GND	GND	GND	JTAG_TDO
7	XTALI	XTALO	CLK1_N	CLK1_P	GND	GND	PCIE_VPH
8	GND	USB_OTG_CHD_B	GPANAIO	GND	NVCC_PLL_OUT	GND	PCIE_VPTX
9	MLB_SN	MLB_SP	RTC_XTALO	RTC_XTALI	USB_OTG_VBUS	VDDUSB_CAP	VDD_SNVS_CAP
10	MLB_DP	MLB_DN	GND	USB_H1_VBUS	USB_H1_DP	USB_H1_DN	GND
11	MLB_CN	MLB_CP	POR_B	PMIC_ON_REQ	TAMPER	PMIC_STBY_REQ	VDD_SNVS_IN
12	NC	NC	BOOT_MODE0	ONOFF	TEST_MODE	BOOT_MODE1	NC
13	GND	SD3_CMD	SD3_DAT5	SD3_DAT4	SD3_DAT6	SD3_DAT7	NC
14	NC	NC	NC	SD3_CLK	SD3_DAT0	SD3_DAT1	NVCC_SD3
15	SD3_DAT2	SD3_DAT3	NANDF_CLE	SD3_RST	NANDF_WP_B	NANDF_CS0	NVCC_NANDF
16	NANDF_ALE	NANDF_RB0	NANDF_CS1	NANDF_CS3	SD4_CLK	NANDF_D2	NVCC_SD1
17	NANDF_CS2	SD4_CMD	NANDF_D1	NANDF_D3	NANDF_D6	SD4_DAT2	NVCC_SD2
18	NANDF_D0	NANDF_D5	NANDF_D7	SD4_DAT0	SD4_DAT4	SD1_DAT3	NVCC_RGMII
19	NANDF_D4	SD4_DAT1	SD4_DAT5	SD4_DAT7	SD1_DAT2	SD2_CMD	GND
20	SD4_DAT3	SD4_DAT6	SD1_DAT1	SD1_CLK	SD2_DAT1	RGMII_TD1	EIM_D20
21	SD1_DAT0	SD1_CMD	SD2_CLK	RGMII_TXC	RGMII_TD2	EIM_D17	EIM_D19
22	SD2_DAT0	SD2_DAT3	RGMII_TD0	RGMII_RX_CTL	EIM_EB2	EIM_D24	EIM_D25
23	SD2_DAT2	RGMII_RD1	RGMII_TX_CTL	RGMII_RD3	EIM_D22	EIM_EB3	EIM_D28
24	RGMII_TD3	RGMII_RD2	RGMII_RD0	EIM_D18	EIM_D26	EIM_A22	EIM_A17
25	GND	RGMII_RXC	EIM_D16	EIM_D23	EIM_D27	EIM_A24	EIM_A19
	A	B	C	D	E	F	G