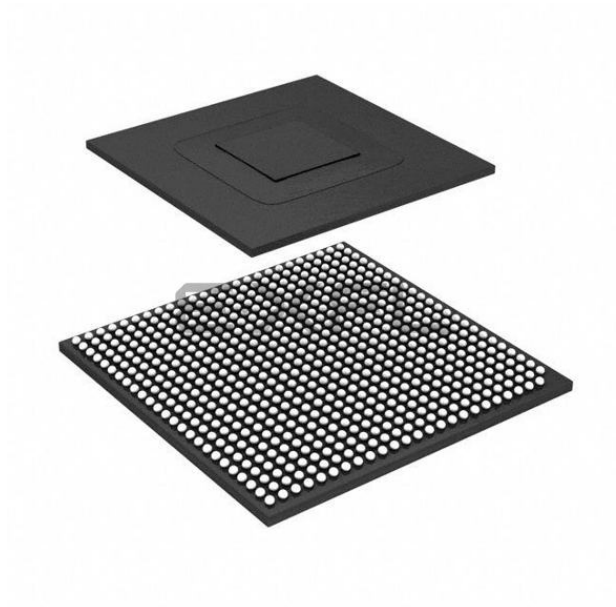

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6s6avm08abr

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
ENET	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the reference manual for details. **Note:** The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Solo/6DualLite errata document (IMX6SDLCE).
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
VPU	Video Processing Unit	Multimedia Peripherals	A high-performing video processing unit (VPU), which covers many SD-level and HD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing, such as rotation and mirroring. See the i.*MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for complete list of VPU's decoding/encoding capabilities.
WDOG-1	Watch Dog	Timer Peripherals	The Watch Dog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watch Dog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW.
WEIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The WEIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
XTALOSC	Crystal Oscillator I/F	Clocks, Resets, and Power Control	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator to provide USB required frequency.

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6Solo/6DualLite processors.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 6Solo/6DualLite Chip-Level Conditions

For these characteristics, …	Topic appears …
Absolute Maximum Ratings	on page 22
BGA Case 2240 Package Thermal Resistance	on page 23
Operating Ranges	on page 24
External Clock Sources	on page 26
Maximal Supply Currents	on page 27
Low Power Mode Supply Currents	on page 29
USB PHY Current Consumption	on page 30
PCIe 2.0 Power Consumption	on page 30

4.1.1 Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core supply voltages	VDDARM_IN VDDSOC_IN	-0.3	1.5	V
Internal supply voltages	VDDARM_CAP VDDSOC_CAP VDDPU_CAP	-0.3	1.3	V
GPIO supply voltage	Supplies denoted as I/O supply	-0.5	3.6	V
DDR I/O supply voltage	Supplies denoted as I/O supply	-0.4	1.975	V
MLB I/O supply voltage	Supplies denoted as I/O supply	-0.3	2.8	V
LVDS I/O supply voltage	Supplies denoted as I/O supply	-0.3	2.8	V
VDD_SNVS_IN supply voltage	VDD_SNVS_IN	-0.3	3.3	V
VDDHIGH_IN supply voltage	VDDHIGH_IN	-0.3	3.6	V
USB VBUS	VBUS	—	5.25	V
Input voltage on USB_OTG_DP, USB_OTG_DN, USB_H1_DP, USB_H1_DN pins	USB_DP/USB_DN	-0.3	3.63	V
Input/output voltage range	V_{in}/V_{out}	-0.5	OVDD[1]+0.3	V

4.1.6 Low Power Mode Supply Currents

Table 13 shows the current core consumption (not including I/O) of i.MX 6Solo/6DualLite processors in selected low power modes.

Table 13. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Units
WAIT	• ARM, SoC, and PU LDOs are set to 1.225 • HIGH LDO set to 2.5 V • Clocks are gated. • DDR is in self refresh. • PLLs are active in bypass (24MHz) • Supply Voltages remain ON	VDDARM_IN (1.4V)	4.5	mA
		VDDSOC_IN (1.4V)	23	
		VDDHIGH_IN (3.0V)	13.5	
		Total	79	mW
STOP_ON	• ARM LDO set to 0.9V • SoC and PU LDOs set to 1.225 V • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh.	VDDARM_IN (1.4V)	4	mA
		VDDSOC_IN (1.4V)	22	
		VDDHIGH_IN (3.0V)	8.5	
		Total	61.9	mW
STOP_OFF	• ARM LDO set to 0.9V • SoC LDO set to: 1.225 V • PU LDO is power gated • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDDARM_IN (1.4V)	4	mA
		VDDSOC_IN (1.4V)	13.5	
		VDDHIGH_IN (3.0V)	7.5	
		Total	47	mW
STANDBY	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5V • PLLs are disabled • Low Voltage • Well Bias ON • XTAL is enabled	VDDARM_IN (0.9V)	0.1	mA
		VDDSOC_IN (0.9V)	5	
		VDDHIGH_IN (3.0V)	5	
		Total	19.6	mW
Deep Sleep Mode (DSM)	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5V • PLLs are disabled • Low Voltage • Well Bias ON • XTAL and bandgap are disabled	VDDARM_IN (0.9V)	0.1	mA
		VDDSoC_IN (0.9V)	2	
		VDDHIGH_IN (3.0V)	0.5	
		Total	3.4	mW

[1] The typical values shown here are for information only and are not guaranteed. These values are average values measured on a typical wafer at 25°C.

4.1.9 HDMI Power Consumption

Table 16 provides HDMI PHY currents for both Active 3D Tx with LFSR15 data and power-down modes.

Table 16. HDMI PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
Active	Bit rate 251.75 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.1	mA
	Bit rate 279.27 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.2	mA
	Bit rate 742.5 Mbps	HDMI_VPH	17	mA
		HDMI_VP	7.5	mA
	Bit rate 1.485 Gbps	HDMI_VPH	17	mA
		HDMI_VP	12	mA
	Bit rate 2.275 Gbps	HDMI_VPH	16	mA
		HDMI_VP	17	mA
	Bit rate 2.97 Gbps	HDMI_VPH	19	mA
		HDMI_VP	22	mA
Power-down		HDMI_VPH	49	µA
		HDMI_VP	1100	µA

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.2.1 Power-Up Sequence

The below restrictions must be followed:

- VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDDHIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- If VDDARM_IN and VDDSOC_IN are connected to different external supply sources, then the following restrictions apply:

2. Calibration is done against 240 Ω external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.8.3 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits" for details.

4.8.4 MLB I/O Differential Output Impedance

Table 38 shows MLB I/O differential output impedance of the i.MX 6Solo/6DualLite processors.

Table 38. MLB I/O Differential Output Impedance

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Differential Output Impedance	Zo		1.6 K		—	Ω

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6Solo/6DualLite processor.

4.9.1 Reset Timings Parameters

Figure 10 shows the reset timing and Table 39 lists the timing parameters.

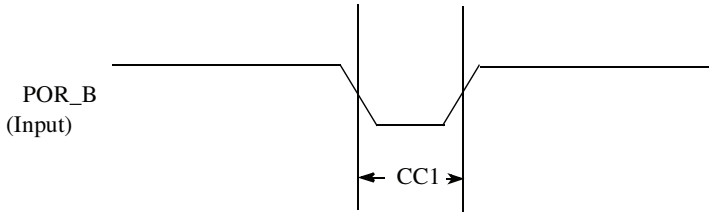

Figure 10. Reset Timing Diagram

Table 39. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid (input slope = 5 ns)	1	—	RTC_XTALI cycle

4.9.2 WDOG Reset Timing Parameters

Figure 11 shows the WDOG reset timing and Table 40 lists the timing parameters.

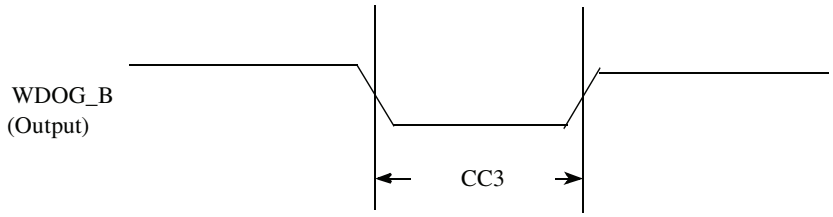

Figure 11. WDOG_B Timing Diagram

Table 40. WDOG_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG_B Assertion	1	—	RTC_XTALI cycle

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 µs.

NOTE

WDOG_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM.

4.9.3.1 EIM Signal Cross Reference

Table 41 is a guide intended to help the user identify signals in the External Interface Module chapter of the reference manual that are identical to those mentioned in this data sheet.

Table 41. EIM Signal Cross Reference

Reference Manual EIM Chapter Nomenclature	Data Sheet Nomenclature, Reference Manual External Signals and Pin Multiplexing Chapter, and IOMUXC Controller Chapter Nomenclature
BCLK	EIM_BCLK
CSx_B	EIM_CSx
WE_B	EIM_RW
OE_B	EIM_OE
BEy_B	EIM_EBx

Table 44. EIM Asynchronous Timing Parameters Table Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max (If 132 MHz is supported by SoC)	Unit
WE31	CSx_B valid to Address Valid	WE4 - WE6 - CSA[2]	—	3 - CSA	ns
WE32	Address Invalid to CSx_B invalid	WE7 - WE5 - CSN[3]	—	3 - CSN	ns
WE32A(muxed A/D	CSx_B valid to Address Invalid	t[4] + WE4 - WE7 + (ADVN[5] + ADVA[6] + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	—	ns
WE33	CSx_B Valid to WE_B Valid	WE8 - WE6 + (WEA - WCSA)	—	3 + (WEA - WCSA)	ns
WE34	WE_B Invalid to CSx_B Invalid	WE7 - WE9 + (WEN - WCSN)	—	3 - (WEN_WCSN)	ns
WE35	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA - RCSA)	—	3 + (OEA - RCSA)	ns
WE35A (muxed A/D)	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - RCSA)	-3 + (OEA + RADVN+RADVA+ ADH+1-RCSA)	3 + (OEA + RADVN+RADVA+AD H+1-RCSA)	ns
WE36	OE_B Invalid to CSx_B Invalid	WE7 - WE11 + (OEN - RCSN)	—	3 - (OEN - RCSN)	ns
WE37	CSx_B Valid to BEy_B Valid (Read access)	WE12 - WE6 + (RBEA - RCSA)	—	3 + (RBEA - RCSA)	ns
WE38	BEy_B Invalid to CSx_B Invalid (Read access)	WE7 - WE13 + (RBEN - RCSN)	—	3 - (RBEN- RCSN)	ns
WE39	CSx_B Valid to ADV_B Valid	WE14 - WE6 + (ADVA - CSA)	—	3 + (ADVA - CSA)	ns
WE40	ADV_B Invalid to CSx_B Invalid (ADVL is asserted)	WE7 - WE15 - CSN	—	3 - CSN	ns
WE40A (muxed A/D)	CSx_B Valid to ADV_B Invalid	WE14 - WE6 + (ADVN + ADVA + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	3 + (ADVN + ADVA + 1 - CSA)	ns
WE41	CSx_B Valid to Output Data Valid	WE16 - WE6 - WCSA	—	3 - WCSA	ns
WE41A (muxed A/D)	CSx_B Valid to Output Data Valid	WE16 - WE6 + (WADVN + WADVA + ADH + 1 - WCSA)	—	3 + (WADVN + WADVA + ADH + 1 - WCSA)	ns
WE42	Output Data Invalid to CSx_B Invalid	WE17 - WE7 - CSN	—	3 - CSN	ns
MAXCO	Output max. delay from internal driving ADDR/control FFs to chip outputs.	10	—	—	ns
MAXCS O	Output max. delay from CSx internal driving FFs to CSx out.	10	—	—	
MAXDI	DATA MAXIMUM delay from chip input data to its internal FF	5	—	—	

4.9.4 DDR SDRAM Specific Parameters (DDR3/DDR3L and LPDDR2)

4.9.4.1 DDR3/DDR3L Parameters

Figure 24 shows the basic timing parameters. The timing parameters for this diagram appear in Table 45.

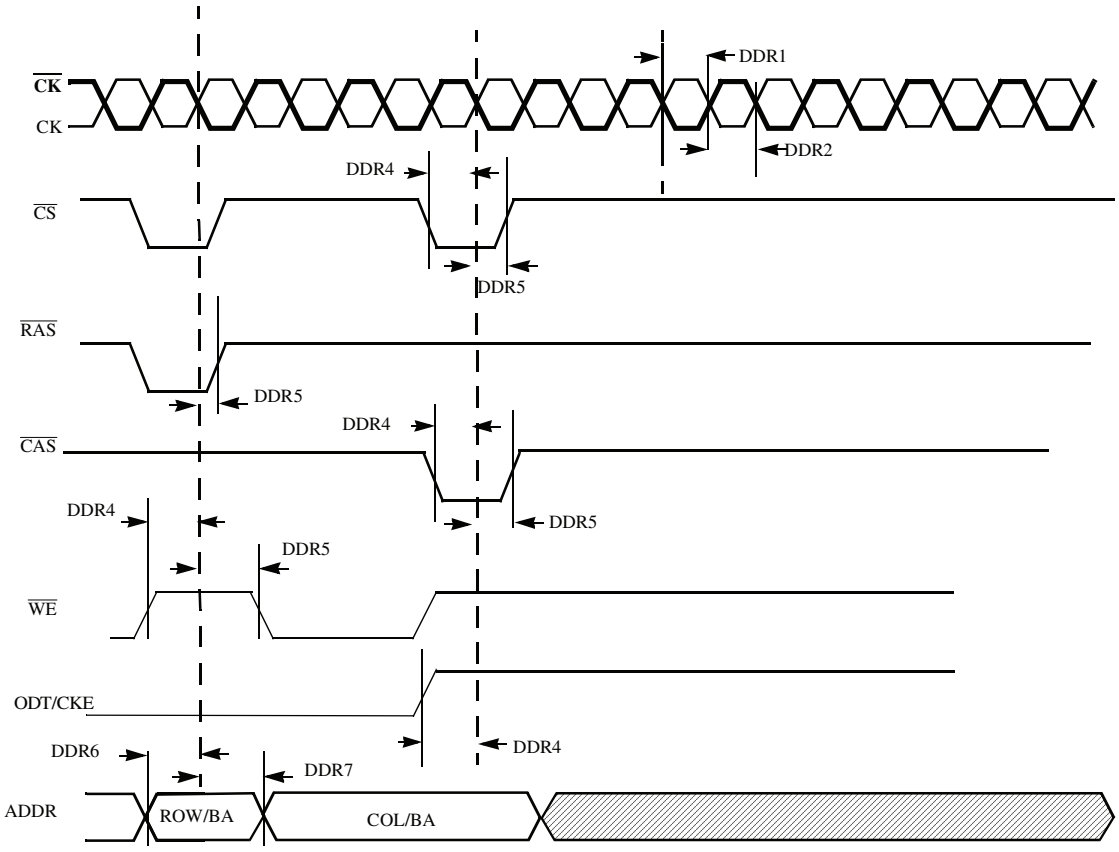

Figure 24. DDR3 Command and Address Timing Parameters

Table 45. DDR3/DDR3L Timing Parameter Table

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR1	CK clock high-level width	t_{CH}	0.47	0.53	t_{CK}
DDR2	CK clock low-level width	t_{CL}	0.47	0.53	t_{CK}
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	t_{IS}	800	—	ps
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	t_{IH}	580	—	ps
DDR6	Address output setup time	t_{IS}	800	—	ps
DDR7	Address output hold time	t_{IH}	580	—	ps

4.11.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing, eMMC4.4 (Dual Date Rate) timing and SDR104/50(SD3.0) timing.

4.11.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 44 depicts the timing of SD/eMMC4.3, and Table 57 lists the SD/eMMC4.3 timing characteristics.

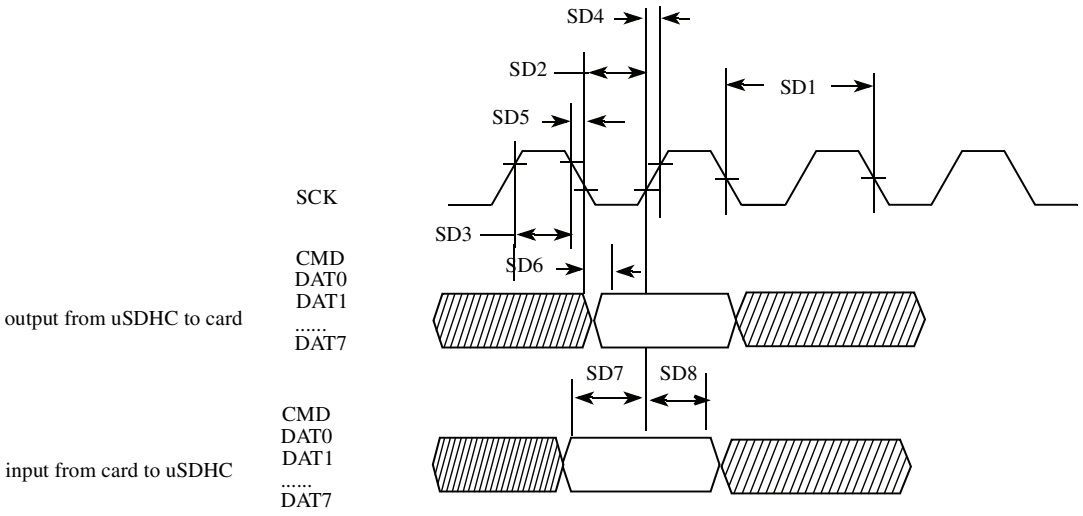

Figure 44. SD/eMMC4.3 Timing

Table 57. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	-6.6	3.6	ns

Figure 47 shows MII receive signal timings. Table 60 describes the timing parameters (M1–M4) shown in the figure.

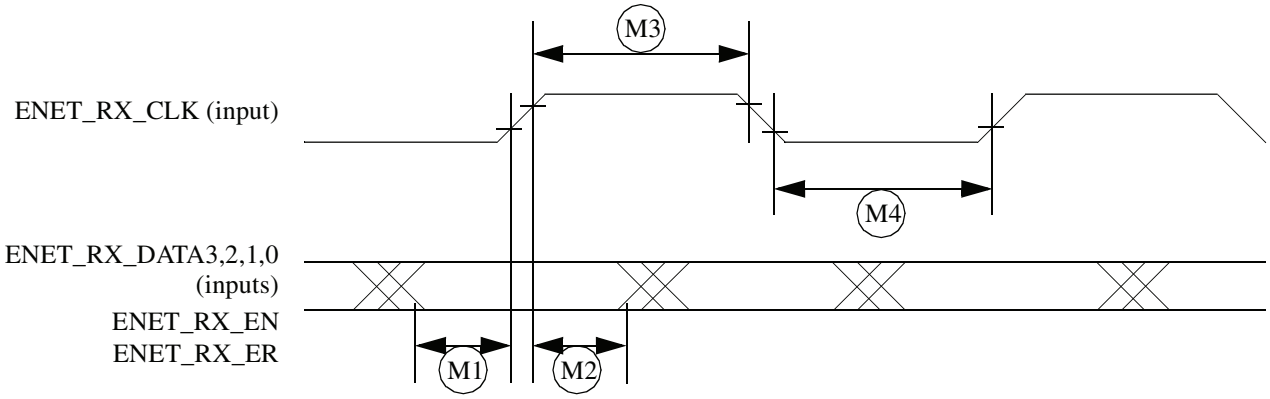

Figure 47. MII Receive Signal Timing Diagram

Table 60. MII Receive Signal Timing

ID	Characteristic[1]	Min.	Max.	Unit
M1	ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup	5	—	ns
M2	ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold	5	—	ns
M3	ENET_RX_CLK pulse width high	35%	65%	ENET_RX_CLK period
M4	ENET_RX_CLK pulse width low	35%	65%	ENET_RX_CLK period

[1] ENET_RX_EN, ENET_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

4.11.5.1.2 MII Transmit Signal Timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_TX_CLK frequency.

NOTE

Table 71 provides information for both the Disp0 and Disp1 ports. However, Disp1 port has reduced pinout depending on IOMUXC configuration and therefore may not support all the above configurations. See the IOMUXC table for details.

4.11.10.5 IPU Display Interface Timing

The IPU Display Interface supports two kinds of display accesses: synchronous and asynchronous. There are two groups of external interface pins to provide synchronous and asynchronous controls accordantly.

4.11.10.5.1 Synchronous Controls

The synchronous control changes its value as a function of a system or of an external clock. This control has a permanent period and a permanent wave form.

There are special physical outputs to provide synchronous controls:

- The ipp_disp_clk is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as, HSYNC/VSYCN) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counters system can be found in the IPU chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

4.11.10.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cs pins are dedicated to provide chip select signals to two displays.
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data in the bus, a new internal start (local start point) is generated. The signals generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

4.11.10.6.3 TFT Panel Sync Pulse Timing Diagrams

Figure 68 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All the parameters shown in the figure are programmable. All controls are started by corresponding internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC, and DRDY signals.

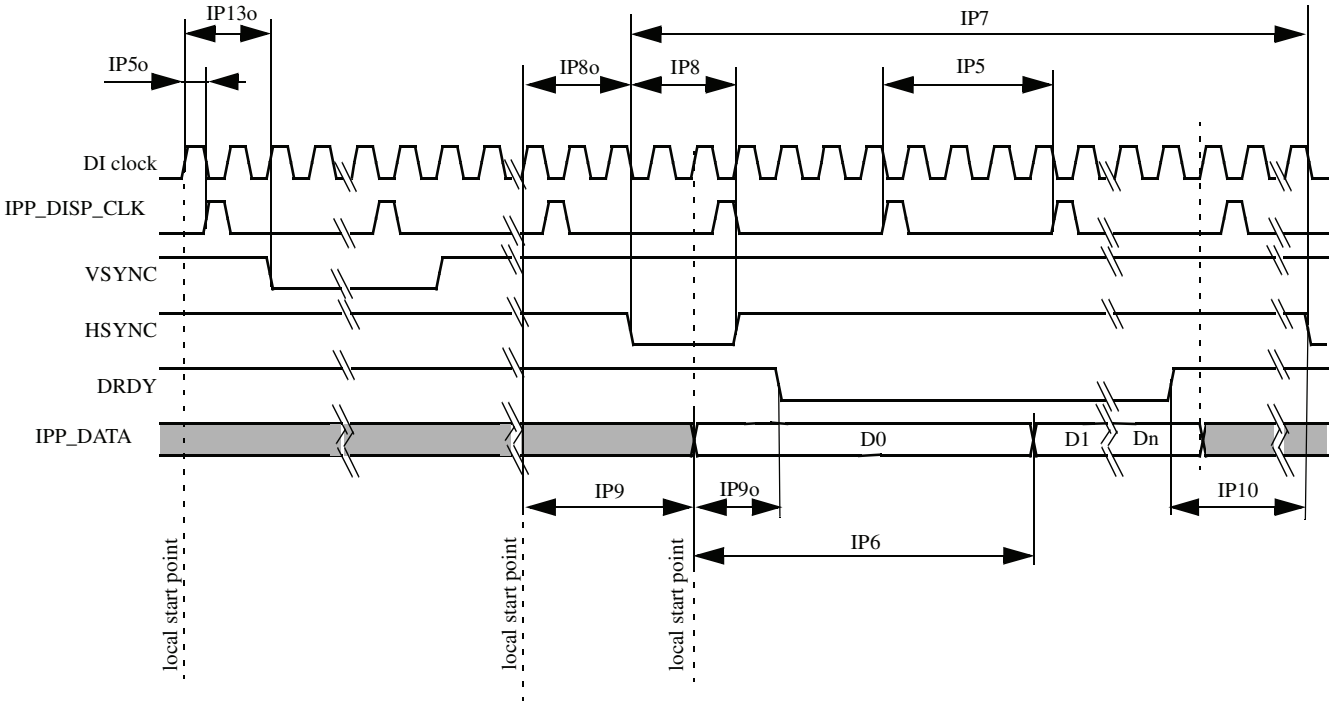

Figure 68. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 69 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

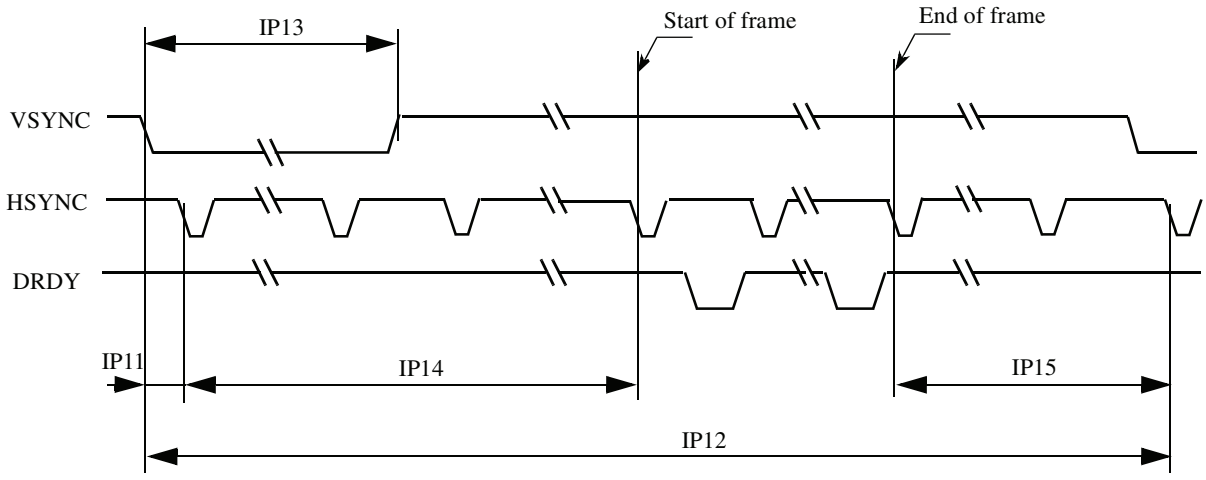

Figure 69. TFT Panels Timing Diagram—Vertical Sync Pulse

4.11.13.4 Synchronized Data Flow Transmission with Wake

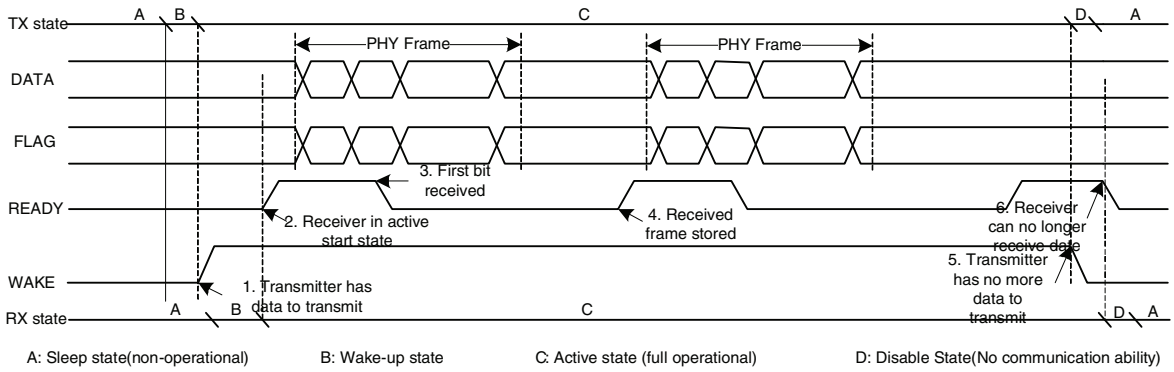

Figure 81. Synchronized Data Flow Transmission with WAKE

4.11.13.5 Stream Transmission Mode Frame Transfer

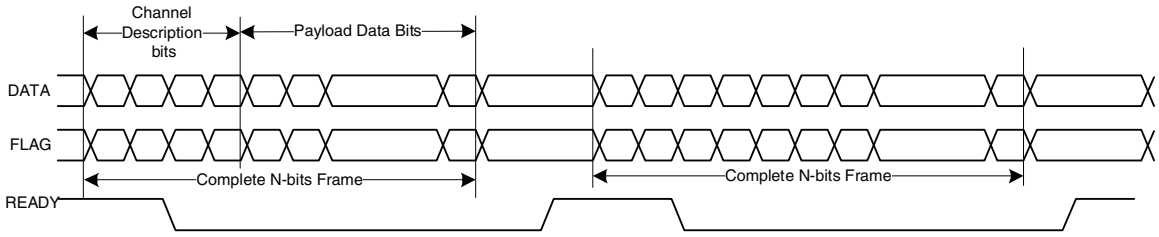

Figure 82. Stream Transmission Mode Frame Transfer (Synchronized Data Flow)

4.11.13.6 Frame Transmission Mode (Synchronized Data Flow)

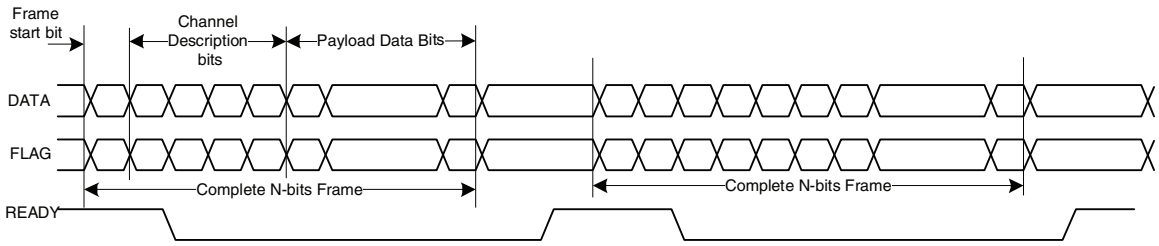

Figure 83. Frame Transmission Mode Transfer of Two Frames (Synchronized Data Flow)

4.11.14 MediaLB (MLB) Characteristics

4.11.14.1 MediaLB (MLB) DC Characteristics

Table 78 lists the MediaLB 3-pin interface electrical characteristics.

Table 78. MediaLB 3-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum input voltage	—	—	—	3.6	V
Low level input threshold	V_{IL}	—	—	0.7	V
High level input threshold	V_{IH}	See Note[1]	1.8	—	V
Low level output threshold	V_{OL}	I_{OL} = 6 mA	—	0.4	V
High level output threshold	V_{OH}	I_{OH} = -6 mA	2.0	—	V
Input leakage current	I_L	$0 < V_{in} < VDD$	—	±10	µA

1 Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

Table 79 lists the MediaLB 6-pin interface electrical characteristics.

Table 79. MediaLB 6-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Driver Characteristics					
Differential output voltage (steady-state): $\lvert V_{O+} - V_{O-} \rvert$	V_{OD}	See Note[1]	300	500	mV
Difference in differential output voltage between (high/low) steady-states: $\lvert V_{OD, high} - V_{OD, low} \rvert$	ΔV_{OD}	—	-50	50	mV
Common-mode output voltage: $(V_{O+} - V_{O-}) / 2$	V_{OCM}	—	1.0	1.5	V
Difference in common-mode output between (high/low) steady-states: $\lvert V_{OCM, high} - V_{OCM, low} \rvert$	ΔV_{OCM}	—	-50	50	mV
Variations on common-mode output during a logic state transitions	V_{CMV}	See Note[2]	—	150	mVpp
Short circuit current	$\lvert I_{OS} \rvert$	See Note[3]	—	43	mA
Differential output impedance	Z_O	—	1.6	—	kΩ
Receiver Characteristics					

Table 85. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIFIN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIFOUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIFOUT1 output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SRCK) period	srckp	40.0	—	ns
SRCK high period	srckph	16.0	—	ns
SRCK low period	srckpl	16.0	—	ns
Modulating Tx clock (STCLK) period	stclkp	40.0	—	ns
STCLK high period	stclkph	16.0	—	ns
STCLK low period	stclkpl	16.0	—	ns

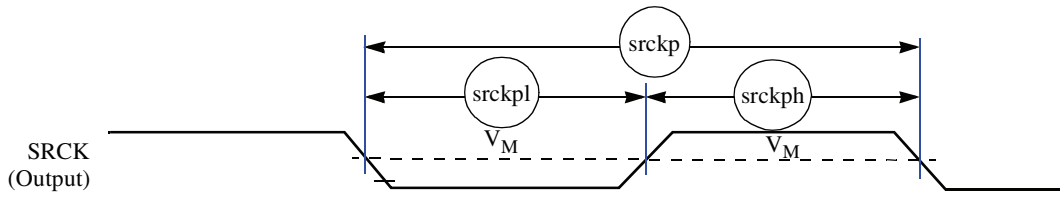

Figure 93. SRCK Timing Diagram

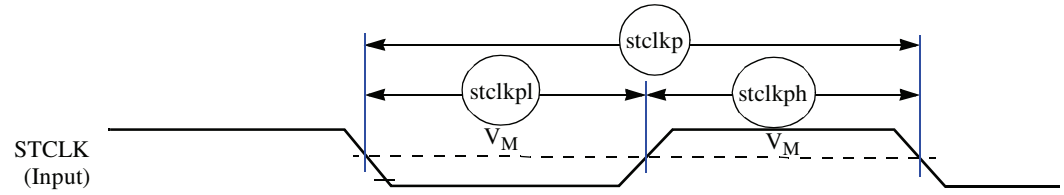

Figure 94. STCLK Timing Diagram

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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TITLE: PBGA, LOW PROFILE, FINE PITCH, 624 I/O, 21 X 21 PKG, 0.8 MM PITCH (MAP)		DOCUMENT NO: 98ASA00404D	REV: O
		CASE NUMBER: 2240–01	27 SEP 2011
		STANDARD: NON–JEDEC	

Figure 105. 21 x 21 mm BGA, Case 2240 Package Top, Bottom, and Side Views

Table 101. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
RTC_XTALI	D9	VDD_SNVS_CAP					
RTC_XTALO	C9	VDD_SNVS_CAP					
SD1_CLK	D20	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[20]	Input	100 kΩ pull-up
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[18]	Input	100 kΩ pull-up
SD1_DAT0	A21	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[16]	Input	100 kΩ pull-up
SD1_DAT1	C20	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[17]	Input	100 kΩ pull-up
SD1_DAT2	E19	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[19]	Input	100 kΩ pull-up
SD1_DAT3	F18	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[21]	Input	100 kΩ pull-up
SD2_CLK	C21	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[10]	Input	100 kΩ pull-up
SD2_CMD	F19	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[11]	Input	100 kΩ pull-up
SD2_DAT0	A22	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[15]	Input	100 kΩ pull-up
SD2_DAT1	E20	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[14]	Input	100 kΩ pull-up
SD2_DAT2	A23	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[13]	Input	100 kΩ pull-up
SD2_DAT3	B22	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[12]	Input	100 kΩ pull-up
SD3_CLK	D14	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[3]	Input	100 kΩ pull-up
SD3_CMD	B13	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[2]	Input	100 kΩ pull-up
SD3_DAT0	E14	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[4]	Input	100 kΩ pull-up
SD3_DAT1	F14	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[5]	Input	100 kΩ pull-up
SD3_DAT2	A15	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[6]	Input	100 kΩ pull-up
SD3_DAT3	B15	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[7]	Input	100 kΩ pull-up
SD3_DAT4	D13	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[1]	Input	100 kΩ pull-up
SD3_DAT5	C13	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[0]	Input	100 kΩ pull-up
SD3_DAT6	E13	NVCC_SD3	GPIO	ALT5	gpio6.GPIO[18]	Input	100 kΩ pull-up
SD3_DAT7	F13	NVCC_SD3	GPIO	ALT5	gpio6.GPIO[17]	Input	100 kΩ pull-up
SD3_RST	D15	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[8]	Input	100 kΩ pull-up
SD4_CLK	E16	NVCC_NANDF	GPIO	ALT5	gpio7.GPIO[10]	Input	100 kΩ pull-up
SD4_CMD	B17	NVCC_NANDF	GPIO	ALT5	gpio7.GPIO[9]	Input	100 kΩ pull-up
SD4_DAT0	D18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[8]	Input	100 kΩ pull-up
SD4_DAT1	B19	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[9]	Input	100 kΩ pull-up
SD4_DAT2	F17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[10]	Input	100 kΩ pull-up

Table 102. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

	AE	AD
1	GND	DRAM_D5
2	DRAM_D1	DRAM_D0
3	DRAM_SDQS0	DRAM_SDQS0_B
4	DRAM_D7	GND
5	DRAM_D9	DRAM_D8
6	DRAM_SDQS1_B	DRAM_SDQS1
7	DRAM_D11	GND
8	DRAM_SDQS2_B	DRAM_SDQS2
9	DRAM_D24	DRAM_D29
10	DRAM_DQM3	GND
11	DRAM_D26	DRAM_D30
12	DRAM_A9	DRAM_A12
13	DRAM_A5	GND
14	DRAM_SDCLK_1_B	DRAM_SDCLK_1
15	DRAM_SDCLK_0_B	DRAM_SDCLK_0
16	DRAM_CAS	GND
17	ZQPAD	DRAM_CS1
18	NC	NC
19	NC	GND
20	NC	NC
21	NC	NC
22	NC	GND
23	NC	NC
24	NC	NC
25	GND	NC
	AE	AD

Table 103 shows the 21 x 21 mm, 0.8 mm pitch ball map for the i.MX 6DualLite.

Table 103. 21 x 21 mm, 0.8 mm Pitch Ball Map

	D	C	B	A	
1	CSI_D1M	GND	PCIE_RXM	NC	1
2	CSI_D1P	JTAG_TRSTB	PCIE_RXP	PCIE_REXT	2
3	GND	JTAG_TMS	PCIE_TXP	PCIE_TXM	3
4	CSI_REXT	GND	GND	GND	4
5	CLK2_P	CLK2_N	VDD_FA	FA_ANA	5
6	GND	GND	USB_OTG_DN	USB_OTG_DP	6
7	CLK1_P	CLK1_N	XTALO	XTALI	7
8	GND	GPANAIO	USB_OTG_CHD_B	GND	8
9	RTC_XTALI	RTC_XTALO	MLB_SP	MLB_SN	9
10	USB_H1_VBUS	GND	MLB_DN	MLB_DP	10
11	PMIC_ON_REQ	POR_B	MLB_CP	MLB_CN	11
12	ONOFF	BOOT_MODE0	NC	NC	12
13	SD3_DAT4	SD3_DAT5	SD3_CMD	GND	13
14	SD3_CLK	NC	NC	NC	14
15	SD3_RST	NANDF_CLE	SD3_DAT3	SD3_DAT2	15
16	NANDF_CS3	NANDF_CS1	NANDF_RB0	NANDF_ALE	16
17	NANDF_D3	NANDF_D1	SD4_CMD	NANDF_CS2	17
18	SD4_DAT0	NANDF_D7	NANDF_D5	NANDF_D0	18
19	SD4_DAT7	SD4_DAT5	SD4_DAT1	NANDF_D4	19
20	SD1_CLK	SD1_DAT1	SD4_DAT6	SD4_DAT3	20
21	RGMII_TXC	SD2_CLK	SD1_CMD	SD1_DAT0	21
22	RGMII_RX_CTL	RGMII_TD0	SD2_DAT3	SD2_DAT0	22
23	RGMII_RD3	RGMII_TX_CTL	RGMII_RD1	SD2_DAT2	23
24	EIM_D18	RGMII_RD0	RGMII_RD2	RGMII_TD3	24
25	EIM_D23	EIM_D16	RGMII_RXC	GND	25
	D	C	B	A	

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