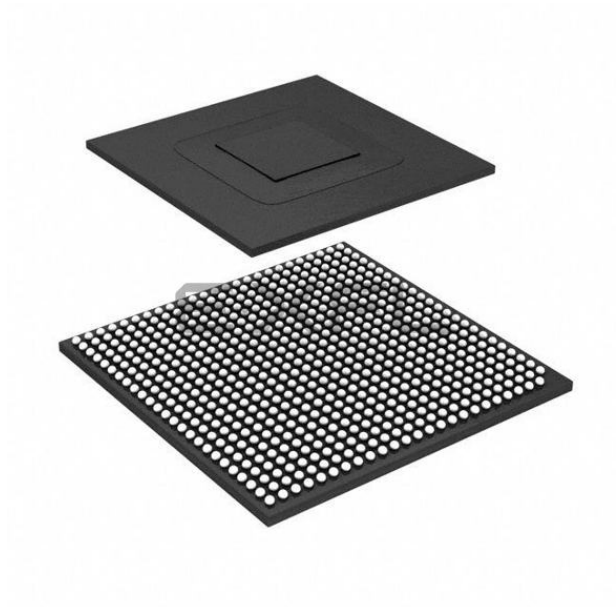

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6s6avm08ac

— Two Controller Area Network (FlexCAN), 1 Mbps each
— Two Watchdog timers (WDOG)
— Audio MUX (AUDMUX)
— MLB (MediaLB) provides interface to MOST Networks (MOST25, MOST50, MOST150) with the option of DTCP cipher accelerator

The i.MX 6Solo/6DualLite processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use SW State Retention and Power Gating for ARM and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6Solo/6DualLite processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6Solo/6DualLite processors incorporate the following hardware accelerators:

- VPU—Video Processing Unit
- IPUv3H—Image Processing Unit version 3H
- GPU3Dv5—3D Graphics Processing Unit (OpenGL ES 2.0) version 5
- GPU2Dv2—2D Graphics Processing Unit (BitBlt)
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing cryptographic and hash engines, 16 KB secure RAM, and True and Pseudo Random Number Generator (NIST certified).
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock
- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

NOTE

The actual feature set depends on the part numbers as described in Table 1, "Orderable Part Numbers," on page 3. Functions, such as video hardware acceleration, and 2D and 3D hardware graphics acceleration may not be enabled for specific part numbers.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CCM GPC SRC	Clock Control Module, Global Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSI	MIPI CSI-2 i/f	Multimedia Peripherals	The CSI IP provides MIPI CSI-2 standard camera interface port. The CSI-2 interface supports from 80 Mbps to 1 Gbps speed per data lane.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6Solo/6DualLite platform.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCIC-0 DCIC-1	Display Content Integrity Checker	Automotive IP	The DCIC provides integrity check on portion(s) of the display. Each i.MX 6Solo/6DualLite processor has two such modules.
DSI	MIPI DSI i/f	Multimedia Peripherals	The MIPI DSI IP provides DSI standard display port interface. The DSI interface support 80 Mbps to 1 Gbps speed per data lane.
DTCP	DTCP	Multimedia Peripherals	Provides encryption function according to Digital Transmission Content Protection standard for traffic over MLB150.
eCSPI1-4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.

Table 10. On-Chip LDOs[1] and their On-Chip Loads (continued)

Voltage Source	Load	Comment
VDDSOC_CAP	HDMI_VP	Board-level connection to VDDSOC_CAP[2 3]
	PCIE_VP	
	PCIE_VPTX	

1 On-chip LDOs are designed to supply i.MX6 loads and must not be used to supply external loads.

2 VDDARM_CAP should not exceed VDDSOC_CAP by more than 50 mV.

3 There is no requirement for VDDSOC_CAP to track within 50 mV as long as it is greater than VDDARM_CAP.

4.1.4 External Clock Sources

Each i.MX 6Solo/6DualLite processor has two external input system clocks: a low frequency (CKIL) and a high frequency (XTAL).

The CKIL is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can substitute the CKIL, in case accuracy is not important.

The system clock input XTAL is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

Table 11 shows the interface frequency requirements.

Table 11. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
CKIL Oscillator[1,2]	f_{ckil}	—	32.768[3]/32.0	—	kHz
XTAL Oscillator[2,4]	f_{xtal}		24		MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 The required frequency stability of this clock source is application dependent. For recommendations, see the Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

3 Recommended nominal frequency 32.768 kHz.

Table 23. OSC32K Main Characteristics

	Min	Typ	Max	Comments
Bias resistor		14 MΩ		This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Crystal Properties				
Cload		10 pF		Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR		50 kΩ	100 kΩ	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes
- LVDS I/O
- MLB I/O

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

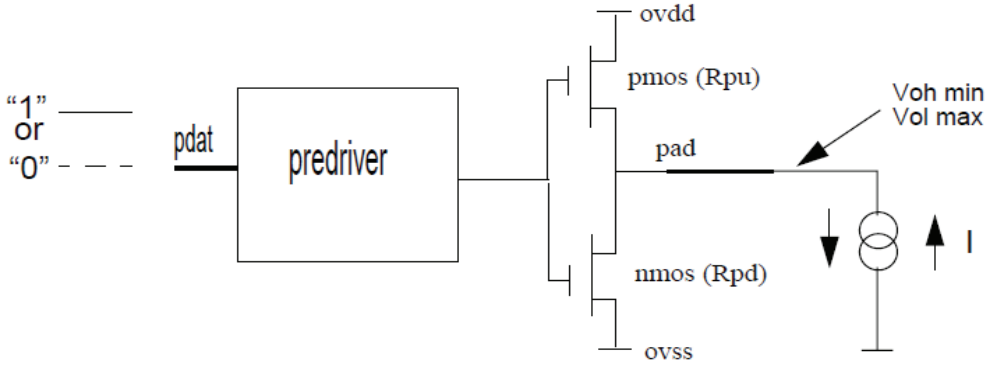

Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

4.8.1 GPIO Output Buffer Impedance

Table 35 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 35. GPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	260 130 90 60 50 40 33	Ω

Table 36 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 36. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	150 75 50 37 30 25 20	Ω

4.8.2 DDR I/O Output Buffer Impedance

The LPDDR2 interface fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 37 shows DDR I/O output buffer impedance of i.MX 6Solo/6DualLite processors.

Table 37. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions DSE(Drive Strength)	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	000 001 010 011 100 101 110 111	Hi-Z 240 120 80 60 48 40 34	Hi-Z 240 120 80 60 48 40 34	Ω

Note:
1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.

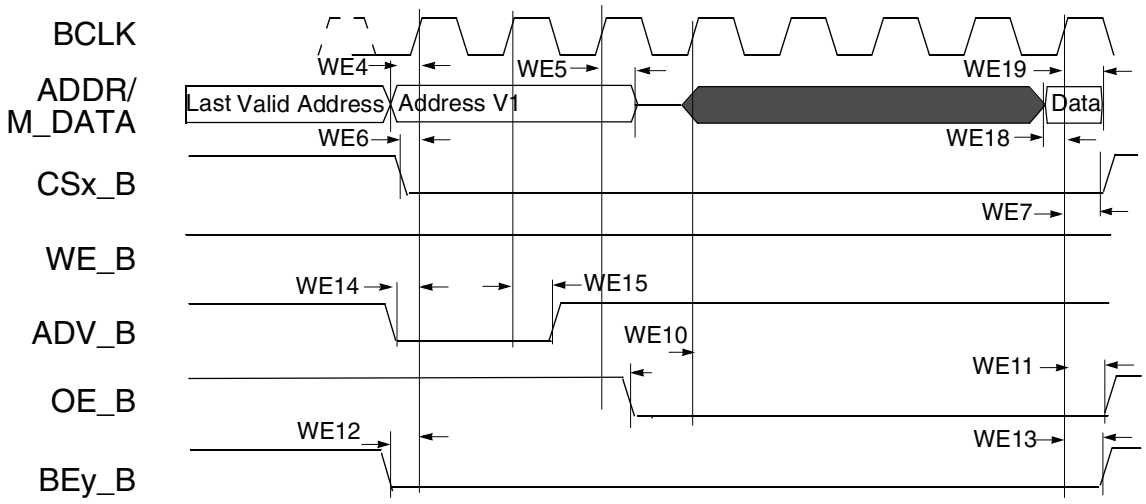

Figure 17. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.5 General EIM Timing-Asynchronous Mode

Figure 18 through Figure 22, and Table 44 help you determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 18 through Figure 21 as RWSC, OEN & CSN is configured differently. See the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for the EIM programming model.

Table 58. eMMC4.4 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input / Card Outputs CMD, DAT (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	2.6	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

4.11.4.3 SDR50/SDR104 AC Timing

Figure 46 depicts the timing of SDR50/SDR104, and Table 59 lists the SDR50/SDR104 timing characteristics.

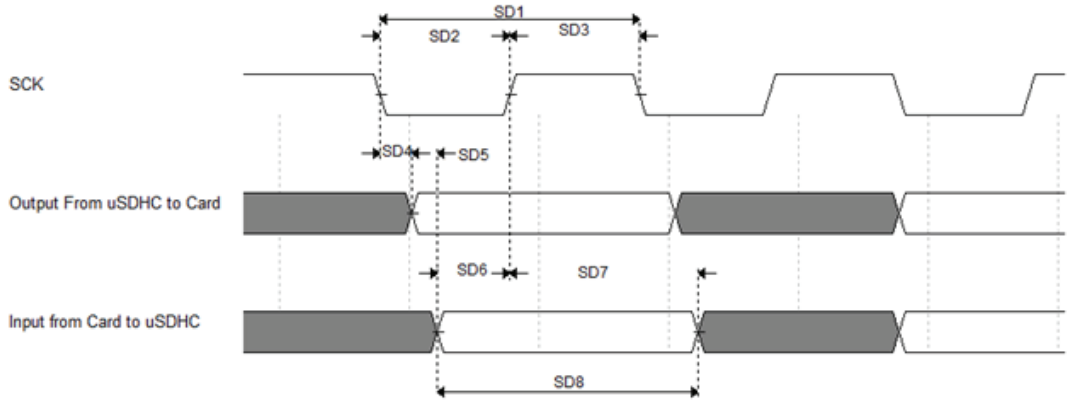

Figure 46. SDR50/SDR104 Timing

Table 59. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	$0.3*t_{CLK}$	$0.7*t_{CLK}$	ns
SD2	Clock High Time	t_{CH}	$0.3*t_{CLK}$	$0.7*t_{CLK}$	ns
uSDHC Output/Card Inputs CMD, DAT in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs CMD, DAT in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	1	ns
uSDHC Input/Card Outputs CMD, DAT in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns

Table 66. Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Operating conditions for HDMI						
avddtmds	Termination supply voltage	-	3.15	3.3	3.45	V
R_T	Termination resistance	-	45	50	55	Ω
TMDS drivers DC specifications						
V_{OFF}	Single-ended standby voltage	RT = 50 Ω For measurement conditions and definitions, see the first two figures above. Compliance point TP1 as defined in the HDMI specification, version 1.3a, section 4.2.4.	avddtmds ± 10 mV			mV
V_{SWING}	Single-ended output swing voltage		400	-	600	mV
V_H	Single-ended output high voltage For definition, see the second figure above	If attached sink supports TMDSCLK < or = 165 MHz	avddtmds ± 10 mV			mV
		If attached sink supports TMDSCLK > 165 MHz	avddtmds - 200 mV	-	avddtmds + 10 mV	mV
V_L	Single-ended output low voltage For definition, see the second figure above	If attached sink supports TMDSCLK < or = 165 MHz	avddtmds - 600 mV	-	avddtmds - 400mV	mV
		If attached sink supports TMDSCLK > 165 MHz	avddtmds - 700 mV	-	avddtmds - 400 mV	mV
R_{TERM}	Differential source termination load (inside HDMI 3D Tx PHY) Although the HDMI 3D Tx PHY includes differential source termination, the user-defined value is set for each single line (for illustration, see the third figure above). **Note:** R_{TERM} can also be configured to be open and not present on TMDS channels.	-	50	-	200	Ω
Hot plug detect specifications						
HPD^{VH}	Hot plug detect high range	-	2.0	-	5.3	V
$^{VHPD}_{VL}$	Hot plug detect low range	-	0	-	0.8	V
$^{HPD}_{Z}$	Hot plug detect input impedance	-	10	-	-	kΩ
$^{HPD}_{t}$	Hot plug detect time delay	-	-	-	100	µs

4.11.8 Switching Characteristics

Table 67 describes switching characteristics for the HDMI 3D Tx PHY. Figure 58 to Figure 62 illustrate various parameters specified in table.

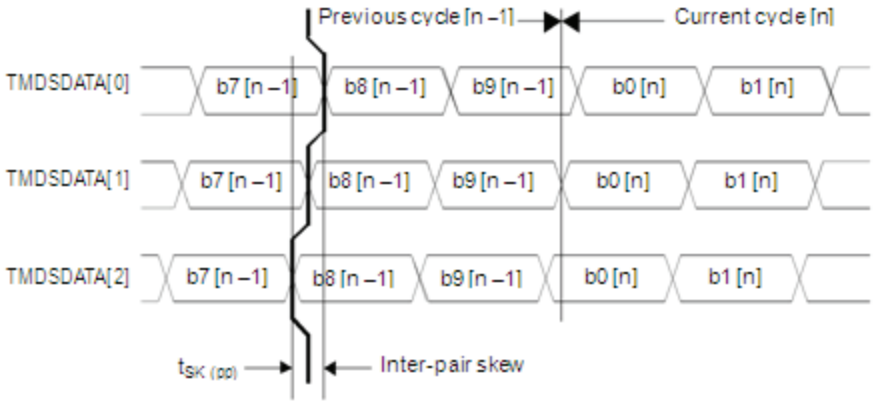

Figure 61. Inter-Pair Skew Definition

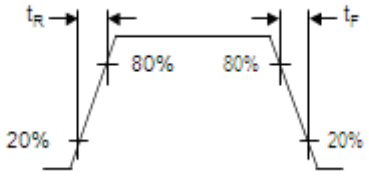

Figure 62. TMDS Output Signals Rise and Fall Time Definition

Table 67. Switching Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
TMDS Drivers Specifications						
—	Maximum serial data rate	—	—	—	3.4	Gbps
$F_{TMDSCLK}$	TMDSCLK frequency	On TMDSCLKP/N outputs	25	—	340	MHz
$P_{TMDSCLK}$	TMDSCLK period	RL = 50 Ω See Figure 58.	2.94	—	40	ns
t_{CDC}	TMDSCLK duty cycle	$t_{CDC} = t_{CPH} / P_{TMDSCLK}$ RL = 50 Ω See Figure 58.	40	50	60	%
t_{CPH}	TMDSCLK high time	RL = 50 Ω See Figure 58.	4	5	6	UI[1]
t_{CPL}	TMDSCLK low time	RL = 50 Ω See Figure 58.	4	5	6	UI[1]
—	TMDSCLK jitter[2]	RL = 50 Ω	—	—	0.25	UI[1]
$t_{SK(p)}$	Intra-pair (pulse) skew	RL = 50 Ω See Figure 60.	—	—	0.15	UI[1]

4.11.10.2 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.11.10.2.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use. On BT.656 one component per cycle is received over the SENSB_DATA bus. On BT.1120 two components per cycle are received over the SENSB_DATA bus.

4.11.10.2.2 Gated Clock Mode

The SENSB_VSYNC, SENSB_HSYNC, and SENSB_PIX_CLK signals are used in this mode. See Figure 64.

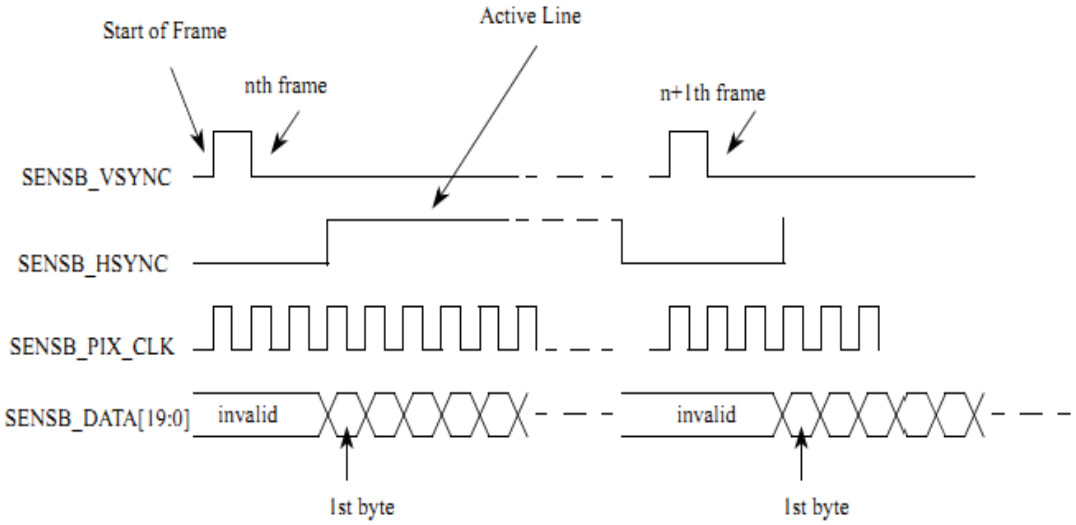

Figure 64. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on SENSB_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then SENSB_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as SENSB_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. SENSB_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI stops receiving data from the stream. For next line the SENSB_HSYNC timing repeats. For next frame the SENSB_VSYNC timing repeats.

Table 75. Electrical and Timing Information (continued)

V_{IDTL}	Differential input low voltage threshold		-70			mV
V_{IHHS}	Single ended input high voltage				460	mV
V_{ILHS}	Single ended input low voltage		-40			mV
V_{CMRXDC}	Input common mode voltage		70		330	mV
Z_{ID}	Differential input impedance		80		125	Ω
LP Line Receiver DC Specifications						
V_{IL}	Input low voltage				550	mV
V_{IH}	Input high voltage		920			mV
V_{HYST}	Input hysteresis		25			mV
Contention Line Receiver DC Specifications						
V_{ILF}	Input low fault threshold		200		450	mV

4.11.12.4 Possible ΔVCMTX and ΔVOD Distortions of the Single-ended HS Signals

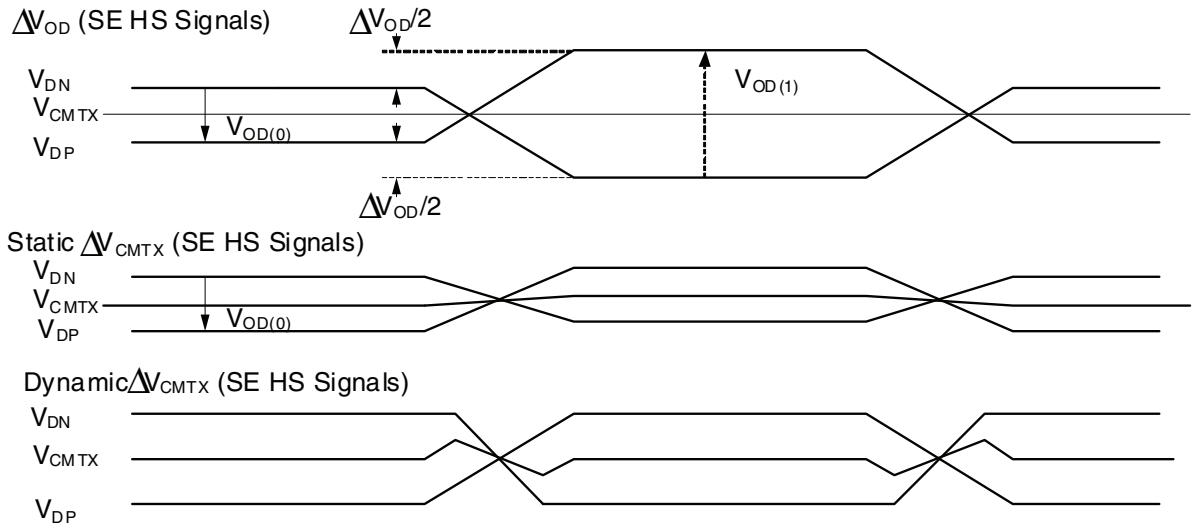

Figure 73. Possible ΔVCMTX and ΔVOD Distortions of the Single-ended HS Signals

4.11.12.5 MIPI D-PHY Switching Characteristics

Table 76. Electrical and Timing Information

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
HS Line Drivers AC Specifications						
—	Maximum serial data rate (forward direction)	On DATAP/N outputs. 80 Ω <= RL <= 125 Ω	80	—	1000	Mbps
F_{DDRCLK}	DDR CLK frequency	On DATAP/N outputs.	40	—	500	MHz
P_{DDRCLK}	DDR CLK period	80 Ω<= RL< = 125 Ω	2	—	25	ns
t_{CDC}	DDR CLK duty cycle	$t_{CDC} = t_{CPH} / P_{DDRCLK}$	—	50	—	%
t_{CPH}	DDR CLK high time		—	1	—	UI
t_{CPL}	DDR CLK low time		—	1	—	UI
—	DDR CLK / DATA Jitter		—	75	—	ps pk–pk
$t_{SKEW[PN]}$	Intra-Pair (Pulse) skew			0.075		UI
$t_{SKEW[TX]}$	Data to Clock Skew		0.350		0.650	UI
$t_{SETUP[RX]}$	Data to Clock Receiver Setup time		0.15			UI
$t_{HOLD[RX]}$	Clock to Data Receiver Hold time		0.15			UI
t_r	Differential output signal rise time	20% to 80%, RL = 50 Ω	150		0.3UI	ps
t_f	Differential output signal fall time	20% to 80%, RL = 50 Ω	150		0.3UI	ps
$\Delta V_{CMTX(HF)}$	Common level variation above 450 MHz	80 Ω<= RL< = 125 Ω			15	mV_{rms}

4.11.13 HSI Host Controller Timing Parameters

This section describes the timing parameters of the HSI Host Controller which are compliant with High-speed Synchronous Serial Interface (HSI) Physical Layer specification version1.01.

4.11.13.1 Synchronous Data Flow

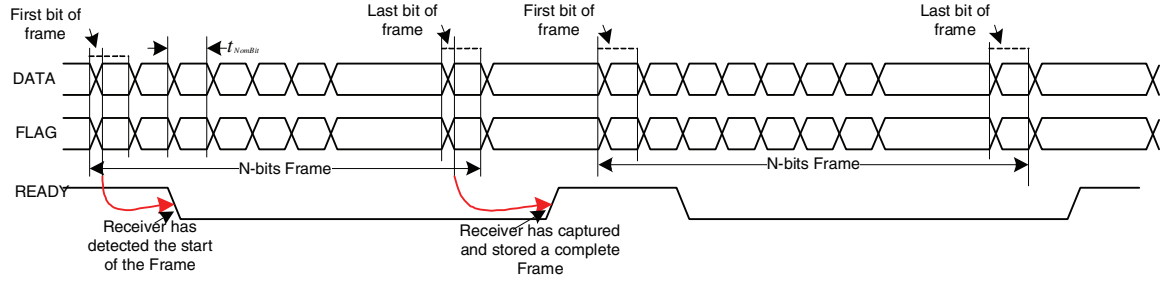

Figure 78. Synchronized Data Flow READY Signal Timing (Frame and Stream Transmission)

4.11.13.2 Pipelined Data Flow

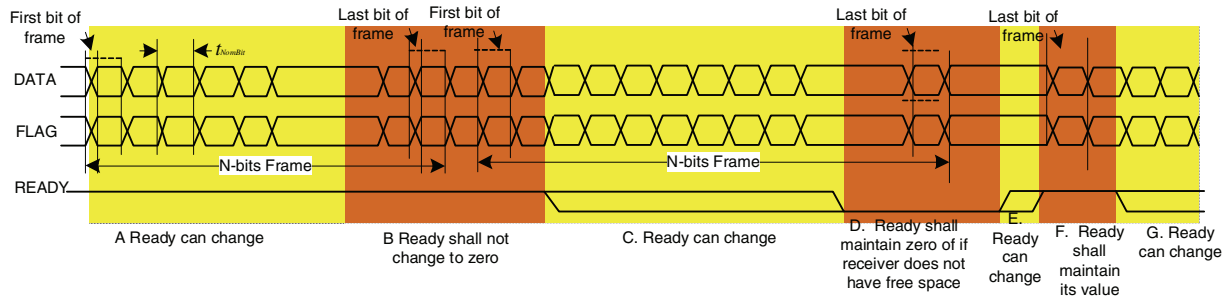

Figure 79. Pipelined Data Flow Ready Signal Timing (Frame Transmission Mode)

4.11.13.3 Receiver Real-Time Data Flow

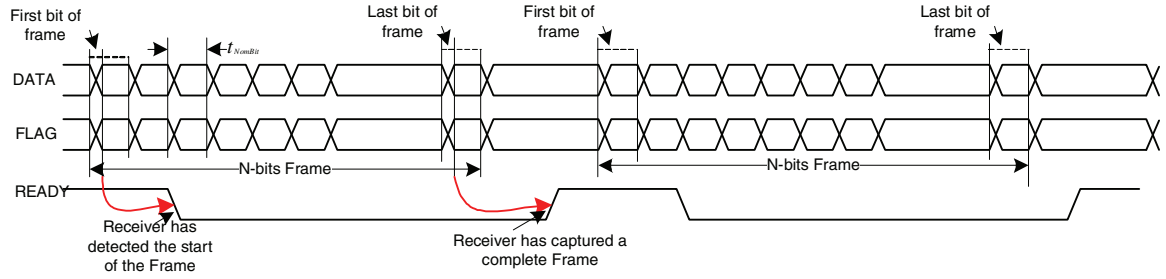

Figure 80. Receiver Real-Time Data Flow READY Signal Timing

Table 80. MLB 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK operating frequency[1]	f_{mck}	11.264	25.6	MHz	256xFs at 44.0 kHz 512xFs at 50.0 kHz
MLBCLK rise time	t_{mckr}	—	3	ns	V_{IL} TO V_{IH}
MLBCLK fall time	t_{mckf}	—	3	ns	V_{IH} TO V_{IL}
MLBCLK low time[2]	t_{mckl}	30 14	—	ns	256xFs 512xFs
MLBCLK high time	t_{mckh}	30 14	—	ns	256xFs 512xFs
MLBSIG/MLBDAT receiver input valid to MLBCLK falling	t_{dsmcf}	1	—	ns	—
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	t_{mdzh}	—	ns	—
MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0	t_{mckl}	ns	[3]
Bus Hold from MLBCLK low	t_{mdzh}	4	—	ns	—
MLBSIG/MLBDAT output valid from transition of MLBCLK (low to high)	t_{delay}		10	ns	—

1 The controller can shut off MLBCLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLBCLK.

2 MLBCLK low/high time includes the pulse width variation.

3 The MediaLB driver can release the MLBDAT/MLBSIG line as soon as MLBCLK is low; however, the logic state of the final driven bit on the line must remain on the bus for t_{mdzh}. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Ground = 0.0 V; load capacitance = 40 pF; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed in Table 81; unless otherwise noted.

Table 81. MLB 1024 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK Operating Frequency[1]	f_{mck}	45.056	51.2	MHz	1024xfs at 44.0 kHz 1024xfs at 50.0 kHz
MLBCLK rise time	t_{mckr}	—	1	ns	V_{IL} TO V_{IH}
MLBCLK fall time	t_{mckf}	—	1	ns	V_{IH} TO V_{IL}
MLBCLK low time	t_{mckl}	6.1	—	ns	[2]
MLBCLK high time	t_{mckh}	9.3	—	ns	—
MLBSIG/MLBDAT receiver input valid to MLBCLK falling	t_{dsmcf}	1	—	ns	—
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	t_{mdzh}	—	ns	—

Table 81. MLB 1024 Fs Timing Parameters (continued)

Parameter	Symbol	Min	Max	Unit	Comment
MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0	t_{mckl}	ns	[3]
Bus Hold from MLBCLK low	t_{mdzh}	2	—	ns	—
MLBSIG/MLBDAT output valid from transition of MLBCLK (low to high)	t_{delay}	—	7	ns	—

[1] The controller can shut off MLBCLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLBCLK.

[2] MLBCLK low/high time includes the pulse width variation.

[3] The MediaLB driver can release the MLBDAT/MLBSIG line as soon as MLBCLK is low; however, the logic state of the final driven bit on the line must remain on the bus for t_{mdzh}. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Table 82 lists the MediaLB 6-pin interface timing characteristics, and Figure 87 shows the MLB 6-pin delay, setup, and hold times.

Table 82. MLB 6-Pin Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
Cycle-to-cycle system jitter	t_{jitter}	—	600	ps	—
Transmitter MLBSP/N (MLBDP/N) output valid from transition of MLBCP/N (low-to-high)[1]	t_{delay}	0.6	1.3	ns	
Disable turnaround time from transition of MLBCP/N (low-to-high)	t_{phz}	0.6	3.5	ns	
Enable turnaround time from transition of MLBCP/N (low-to-high)	t_{plz}	0.6	5.6	ns	
MLBSP/N (MLBDP/N) valid to transition of MLBCP/N (low-to-high)	t_{su}	0.05	—	ns	
MLBSP/N (MLBDP/N) hold from transition of MLBCP/N (low-to-high)[2]	t_{hd}	0.6			

[1] t_{delay}, t_{phz}, t_{plz}, t_{su}, and t_{hd} may also be referenced from a low-to-high transition of the recovered clock for 2:1 and 4:1 recovered-to-external clock ratios.

[2] The transmitting device must ensure valid data on MLBSP/N (MLBDP/N) for at least $t_{hd(min)}$ following the rising edge of MLBCP/N; receivers must latch MLBSP/N (MLBDP/N) data within $t_{hd(min)}$ of the rising edge of MLBCP/N.

6 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 21x21 mm Package Information

6.1.1 Case 2240, 21 x 21 mm, 0.8 mm Pitch, 25 x 25 Ball Matrix

Figure 105 shows the top, bottom, and side views of the 21×21 mm BGA package.

6.1.2 21 x 21 mm Supplies Contact Assignments and Functional Contact Assignments

Table 100 shows supplies contact assignments for the 21 x 21 mm package.

Table 100. 21 x 21 mm Supplies Contact Assignments

Supply Rail Name	Ball(s) Position(s)	Remark
CSI_REXT	D4	
DRAM_VREF	AC2	
DSI_REXT	G4	
GND	A4, A8, A13, A25, B4, C1, C4, C6, C10, D3, D6, D8, E5, E6, E7, F5, F6, F7, F8, G3, G10, G19, H8, H12, H15, H18, J2, J8, J12, J15, J18, K8, K10, K12, K15, K18, L2, L5, L8, L10, L12, L15, L18, M8, M10, M12, M15, M18, N8, N10, N15, N18, P8, P10, P12, P15, P18, R8, R12, R15, R17, T8, T11, T12, T15, T17, T19, U8, U11, U12, U15, U17, U19, V8, V19, W3, W7, W8, W9, W10, W11, W12, W13, W15, W16, W17, W18, W19, Y5, Y24, AA7, AA10, AA13, AA16, AA19, AA22, AB3, AB24, AD4, AD7, AD10, AD13, AD16, AD19, AD22, AE1, AE25	
HDMI_REF	J1	
HDMI_VP	L7	
HDMI_VPH	M7	
NVCC_CSI	N7	Supply of the camera sensor interface
NVCC_DRAM	R18, T18, U18, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18	Supply of the DDR interface
NVCC_EIM	K19, L19, M19	Supply of the EIM interface
NVCC_ENET	R19	Supply of the ENET interface
NVCC_GPIO	P7	Supply of the GPIO interface
NVCC_JTAG	J7	Supply of the JTAG tap controller interface
NVCC_LCD	P19	Supply of the LCD interface
NVCC_LVDS2P5	V7	Supply of the LVDS display interface and DDR pre-drivers
NVCC_MIPI	K7	Supply of the MIPI interface
NVCC_NANDF	G15	Supply of the raw NAND Flash memories interface
NVCC_PLL_OUT	E8	
NVCC_RGMII	G18	Supply of the ENET interface
NVCC_SD1	G16	Supply of the SD card interface
NVCC_SD2	G17	Supply of the SD card interface
NVCC_SD3	G14	Supply of the SD card interface

Table 100. 21 x 21 mm Supplies Contact Assignments (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
NC	G13	
NC	N12	

Table 101 shows an alpha-sorted list of functional contact assignments for the 21 x 21 mm package.

Table 101. 21 x 21 mm Functional Contact Assignments[1]

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
BOOT_MODE0	C12	VDD_SNVS_IN	GPIO	ALT0	src.BOOT_MODE[0]	Input	100 kΩ pull-down
BOOT_MODE1	F12	VDD_SNVS_IN	GPIO	ALT0	src.BOOT_MODE[1]	Input	100 kΩ pull-down
CLK1_N	C7	VDDHIGH_CAP					
CLK1_P	D7	VDDHIGH_CAP					
CLK2_N	C5	VDDHIGH_CAP					
CLK2_P	D5	VDDHIGH_CAP					
CSI_CLK0M	F4	NVCC_MIPI	ANALOG				
CSI_CLK0P	F3	NVCC_MIPI	ANALOG				
CSI_D0M	E4	NVCC_MIPI	ANALOG				
CSI_D0P	E3	NVCC_MIPI	ANALOG				
CSI_D1M	D1	NVCC_MIPI	ANALOG				
CSI_D1P	D2	NVCC_MIPI	ANALOG				
CSI0_DAT10	M1	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[28]	Input	100 kΩ pull-up
CSI0_DAT11	M3	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[29]	Input	100 kΩ pull-up
CSI0_DAT12	M2	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[30]	Input	100 kΩ pull-up
CSI0_DAT13	L1	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[31]	Input	100 kΩ pull-up
CSI0_DAT14	M4	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[0]	Input	100 kΩ pull-up
CSI0_DAT15	M5	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[1]	Input	100 kΩ pull-up
CSI0_DAT16	L4	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[2]	Input	100 kΩ pull-up
CSI0_DAT17	L3	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[3]	Input	100 kΩ pull-up
CSI0_DAT18	M6	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[4]	Input	100 kΩ pull-up
CSI0_DAT19	L6	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[5]	Input	100 kΩ pull-up
CSI0_DAT4	N1	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[22]	Input	100 kΩ pull-up
CSI0_DAT5	P2	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[23]	Input	100 kΩ pull-up

Table 103. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

M	L	K	J	H	G	F	E
CSI0_DAT10	CSI0_DAT13	HDMI_HPD	HDMI_REF	DSI_D1P	DSI_D0P	NC	NC
CSI0_DAT12	GND	HDMI_DDCCEC	GND	DSI_D1M	DSI_D0M	NC	NC
CSI0_DAT11	CSI0_DAT17	HDMI_D2M	HDMI_D1M	DSI_CLK0M	GND	CSI_CLK0P	CSI_D0P
CSI0_DAT14	CSI0_DAT16	HDMI_D2P	HDMI_D1P	DSI_CLK0P	DSI_REXT	CSI_CLK0M	CSI_D0M
CSI0_DAT15	GND	HDMI_D0M	HDMI_CLKM	JTAG_TCK	JTAG_TDI	GND	GND
CSI0_DAT18	CSI0_DAT19	HDMI_D0P	HDMI_CLKP	JTAG_MOD	JTAG_TDO	GND	GND
HDMI_VPH	HDMI_VP	NVCC_MIPI	NVCC_JTAG	PCIE_VP	PCIE_VPH	GND	GND
GND	GND	GND	GND	GND	PCIE_VPTX	GND	NVCC_PLL_OUT
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDHIGH_IN	VDDHIGH_IN	VDD_SNVS_CAP	VDDUSB_CAP	USB_OTG_VBUS
GND	GND	GND	VDDHIGH_CAP	VDDHIGH_CAP	GND	USB_H1_DN	USB_H1_DP
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDD_SNVS_IN	PMIC_STBY_REQ	TAMPER
GND	GND	GND	GND	GND	NC	BOOT_MODE1	TEST_MODE
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	NC	SD3_DAT7	SD3_DAT6
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	NVCC_SD3	SD3_DAT1	SD3_DAT0
GND	GND	GND	GND	GND	NVCC_NANDF	NANDF_CS0	NANDF_WP_B
VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	NVCC_SD1	NANDF_D2	SD4_CLK
VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	NVCC_SD2	SD4_DAT2	NANDF_D6
GND	GND	GND	GND	GND	NVCC_RGMII	SD1_DAT3	SD4_DAT4
NVCC_EIM	NVCC_EIM	NVCC_EIM	EIM_D29	EIM_A25	GND	SD2_CMD	SD1_DAT2
EIM_DA11	EIM_DA0	EIM_RW	EIM_D30	EIM_D21	EIM_D20	RGMII_TD1	SD2_DAT1
EIM_DA9	EIM_DA2	EIM_EB0	EIM_A23	EIM_D31	EIM_D19	EIM_D17	RGMII_TD2
EIM_DA10	EIM_DA4	EIM_LBA	EIM_A18	EIM_A20	EIM_D25	EIM_D24	EIM_EB2
EIM_DA13	EIM_DA5	EIM_EB1	EIM_CS1	EIM_A21	EIM_D28	EIM_EB3	EIM_D22
EIM_DA12	EIM_DA8	EIM_DA3	EIM_OE	EIM_CS0	EIM_A17	EIM_A22	EIM_D26
EIM_WAIT	EIM_DA7	EIM_DA6	EIM_DA1	EIM_A16	EIM_A19	EIM_A24	EIM_D27
M	L	K	J	H	G	F	E

Table 103. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

Y	W	V	U	T	R	P	N
LVDS1_TX0_N	LVDS0_TX3_P	LVDS0_TX2_P	LVDS0_TX0_P	GPIO_2	GPIO_17	CSI0_PIXCLK	CSI0_DAT4
LVDS1_TX0_P	LVDS0_TX3_N	LVDS0_TX2_N	LVDS0_TX0_N	GPIO_9	GPIO_16	CSI0_DAT5	CSI0_VSYNC
LVDS1_CLK_N	GND	LVDS0_CLK_P	LVDS0_TX1_P	GPIO_6	GPIO_7	CSI0_DATA_EN	CSI0_DAT7
LVDS1_CLK_P	KEY_ROW2	LVDS0_CLK_N	LVDS0_TX1_N	GPIO_1	GPIO_5	CSI0_MCLK	CSI0_DAT6
GND	KEY_COL0	KEY_ROW4	KEY_COL3	GPIO_0	GPIO_8	GPIO_19	CSI0_DAT9
DRAM_RESET	KEY_COL2	KEY_ROW0	KEY_ROW1	KEY_COL4	GPIO_4	GPIO_18	CSI0_DAT8
DRAM_D20	GND	NVCC_LVDS2P5	KEY_COL1	KEY_ROW3	GPIO_3	NVCC_GPIO	NVCC_CSI
DRAM_D21	GND	GND	GND	GND	GND	GND	GND
DRAM_D19	GND	NVCC_DRAM	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN
DRAM_D25	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDSOC_CAP	GND	GND
DRAM_SDCKE0	GND	NVCC_DRAM	GND	GND	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
DRAM_A15	GND	NVCC_DRAM	GND	GND	GND	GND	NC
DRAM_A7	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
DRAM_A3	DRAM_A4	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_IN	VDDARM_IN	VDDARM_IN
DRAM_SDBA1	GND	NVCC_DRAM	GND	GND	GND	GND	GND
DRAM_CS0	GND	NVCC_DRAM	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN
DRAM_D36	GND	NVCC_DRAM	GND	GND	GND	VDDPU_CAP	VDDPU_CAP
DRAM_D37	GND	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	GND	GND
DRAM_D40	GND	GND	GND	GND	NVCC_ENET	NVCC_LCD	DI0_DISP_CLK
DRAM_D44	ENET_TXD1	ENET_MDC	ENET_TXD0	DISP0_DAT21	DISP0_DAT13	DISP0_DAT4	DI0_PIN3
DRAM_DQM7	ENET_RXD0	ENET_TX_EN	ENET_CRS_DV	DISP0_DAT16	DISP0_DAT10	DISP0_DAT3	DI0_PIN15
DRAM_D59	ENET_RXD1	ENET_REF_CLK	DISP0_DAT20	DISP0_DAT15	DISP0_DAT8	DISP0_DAT1	EIM_BCLK
DRAM_D62	ENET_RX_ER	ENET_MDIO	DISP0_DAT19	DISP0_DAT11	DISP0_DAT6	DISP0_DAT2	EIM_DA14
GND	DISP0_DAT23	DISP0_DAT22	DISP0_DAT17	DISP0_DAT12	DISP0_DAT7	DISP0_DAT0	EIM_DA15
DRAM_D58	DRAM_D63	DISP0_DAT18	DISP0_DAT14	DISP0_DAT9	DISP0_DAT5	DI0_PIN4	DI0_PIN2
Y	W	V	U	T	R	P	N