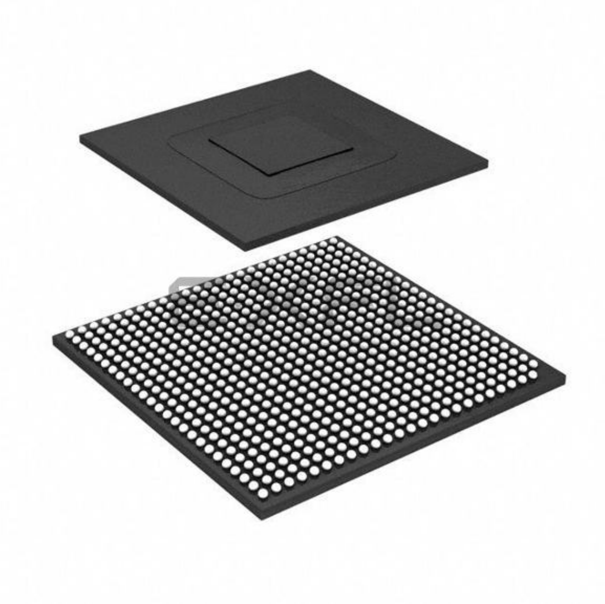

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6u1avm08ac

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

MC IMX6 X @ + VV $$ % B

Qualification Level	MC
Prototype Samples	PC
Mass Production	MC
Special	SC

Part # Series	X
i.MX 6DualLite	U
i.MX 6Solo	S

Part differentiator	@
Consumer with VPU, GPU, EPD, No MLB	8
Industrial with VPU, GPU, No EPD, No MLB	7
Automotive with VPU, GPU, No EPD	6
Consumer, with VPU, GPU, No EPD, No MLB	5
Automotive with GPU, No VPU, No EPD	4
Automotive, No VPU, No GPU, No display	1

Temperature Tj	+
Consumer: 0 to + 95C	D
Extended Consumer: -20 to + 105C	E
Industrial: -40 to +105C	C
Automotive: -40 to + 125C	A

Package Type	ROHS
MAPBGA 21x21 0.8mm	VM

Frequency	$$
800 MHz[2]	08
1 GHz[3]	10

Fusing	%
Real Codec off & no HDCP or DTCP	A
Real Codec off with HDCP on	C

Silicon Rev[1]	B
Rev 1.1	B

1. See the freescale.com\imx6series Web page for latest information on the available silicon revision.
2. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 792 MHz.
3. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz.

Figure 1. Part Number Nomenclature—i.MX 6DualLite and 6Solo

1.2 Features

The i.MX 6Solo/6DualLite processors are based on ARM Cortex-A9 MPCore™ Platform, which has the following features:

- The i.MX 6Solo supports single ARM Cortex-A9 MPCore (with TrustZone)
- The i.MX 6DualLite supports dual ARM Cortex-A9 MPCore (with TrustZone)
- The core configuration is symmetric, where each core includes:
  - — 32 KByte L1 Instruction Cache
  - — 32 KByte L1 Data Cache
  - — Private Timer and Watchdog
  - — Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CCM GPC SRC	Clock Control Module, Global Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSI	MIPI CSI-2 i/f	Multimedia Peripherals	The CSI IP provides MIPI CSI-2 standard camera interface port. The CSI-2 interface supports from 80 Mbps to 1 Gbps speed per data lane.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6Solo/6DualLite platform.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCIC-0 DCIC-1	Display Content Integrity Checker	Automotive IP	The DCIC provides integrity check on portion(s) of the display. Each i.MX 6Solo/6DualLite processor has two such modules.
DSI	MIPI DSI i/f	Multimedia Peripherals	The MIPI DSI IP provides DSI standard display port interface. The DSI interface support 80 Mbps to 1 Gbps speed per data lane.
DTCP	DTCP	Multimedia Peripherals	Provides encryption function according to Digital Transmission Content Protection standard for traffic over MLB150.
eCSPI1-4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.

Table 7. Absolute Maximum Ratings (continued)

Parameter Description	Symbol	Min	Max	Unit
ESD damage immunity: • Human Body Model (HBM) • Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	V
Storage temperature range	$T_{STORAGE}$	-40	150	^{o}C

1 OVDD is the I/O supply voltage.

4.1.2 Thermal Resistance

4.1.2.1 BGA Case 2240 Package Thermal Resistance

Table 8 displays the thermal resistance data.

Table 8. Thermal Resistance Data

Rating	Test Conditions	Symbol	Value	Unit
Junction to Ambient[1]	Single-layer board (1s); natural convection[2] Four-layer board (2s2p); natural convection[2]	$R_{\theta JA}$ $R_{\theta JA}$	38 23	^{o}C/W ^{o}C/W
Junction to Ambient[1]	Single-layer board (1s); airflow 200 ft/min[2,3] Four-layer board (2s2p); airflow 200 ft/min[2,3]	$R_{\theta JA}$ $R_{\theta JA}$	30 20	^{o}C/W ^{o}C/W
Junction to Board[1,4]		$R_{\theta JB}$	14	^{o}C/W
Junction to Case[1,5]		$R_{\theta JC}$	6	^{o}C/W
Junction to Package Top[1,6]	Natural Convection	Ψ_{JT}	2	^{o}C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-2 with the single layer board horizontal. Thermal test board meets JEDEC specification for the specified package.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

[4] External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 11 are required for use with Freescale BSPs to ensure precise time keeping and USB operation. For RTC_XTAL operation, two clock sources are available.

- On-chip 40 kHz ring oscillator—this clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit:
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximal Supply Currents

The Power Virus numbers shown in Table 12 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The MMPF0100xxxx, Freescale's power management IC targeted for the i.MX 6x family, supports the Power Virus mode operating at 1% duty cycle. Higher duty cycles are allowed, but a robust thermal design is required for the increased system power dissipation.

See the i.MX 6Solo/6DualLite Power Consumption Measurement Application Note (AN4576) for more details on typical power consumption under various use case definitions.

Table 12. Maximal Supply Currents

Power Line	Conditions	Max Current	Unit
VDDARM_IN	996 MHz ARM clock based on Power Virus operation	2200	mA
VDDSOC_IN	996 MHz ARM clock	1260	mA
VDDHIGH_IN		125[1]	mA
VDD_SNVS_IN		275[2]	µA
USB_OTG_VBUS/USB_H1_VBUS (LDO 3P0)		25[3]	mA
Primary Interface (IO) Supplies			

2 Vid(ac) specifies the input differential voltage | Vtr - Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 32 shows the AC parameters for DDR I/O operating in DDR3/DDR3L mode.

Table 32. DDR I/O DDR3/DDR3L Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref - 0.175	V
AC differential input voltage[2]	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	Vref - 0.15	—	Vref + 0.15	V
Over/undershoot peak	Vpeak	—	—	—	0.4	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.5	V-ns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	Driver impedance = 34 Ω	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC JESD79_3C specification supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage | Vtr-Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.7.3 LVDS I/O AC Parameters

The differential output transition time waveform is shown in Figure 6.

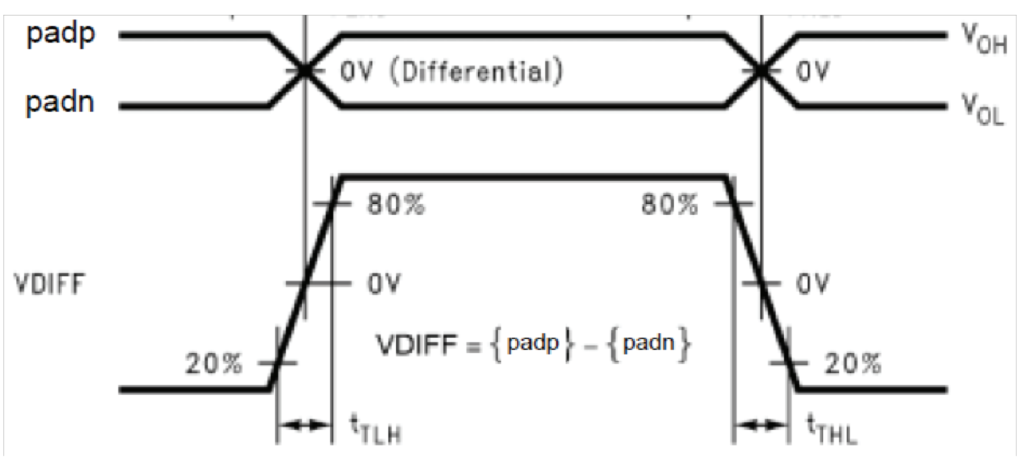

Figure 6. Differential LVDS Driver Transition Time Waveform

4.8.1 GPIO Output Buffer Impedance

Table 35 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 35. GPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	260 130 90 60 50 40 33	Ω

Table 36 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 36. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	150 75 50 37 30 25 20	Ω

4.8.2 DDR I/O Output Buffer Impedance

The LPDDR2 interface fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 37 shows DDR I/O output buffer impedance of i.MX 6Solo/6DualLite processors.

Table 37. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions DSE(Drive Strength)	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	000 001 010 011 100 101 110 111	Hi-Z 240 120 80 60 48 40 34	Hi-Z 240 120 80 60 48 40 34	Ω

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.

4.9.3.4 Examples of EIM Synchronous Accesses

Table 43. EIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	BCLK Cycle time[2]	t	—	2 x t		3 x t	—	4 x t	—
WE2	BCLK Low Level Width	0.4 x t	—	0.8 x t		1.2 x t	—	1.6 x t	—
WE3	BCLK High Level Width	0.4 x t	—	0.8 x t		1.2 x t	—	1.6 x t	—
WE4	Clock rise to address valid[3]	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE5	Clock rise to address invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE6	Clock rise to CSx_B valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE7	Clock rise to CSx_B invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE8	Clock rise to WE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE9	Clock rise to WE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE10	Clock rise to OE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE11	Clock rise to OE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE12	Clock rise to BEy_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE13	Clock rise to BEy_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE14	Clock rise to ADV_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE15	Clock rise to ADV_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE16	Clock rise to Output Data Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE17	Clock rise to Output Data Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE18	Input Data setup time to Clock rise	2	—	4	—	—	—	—	—

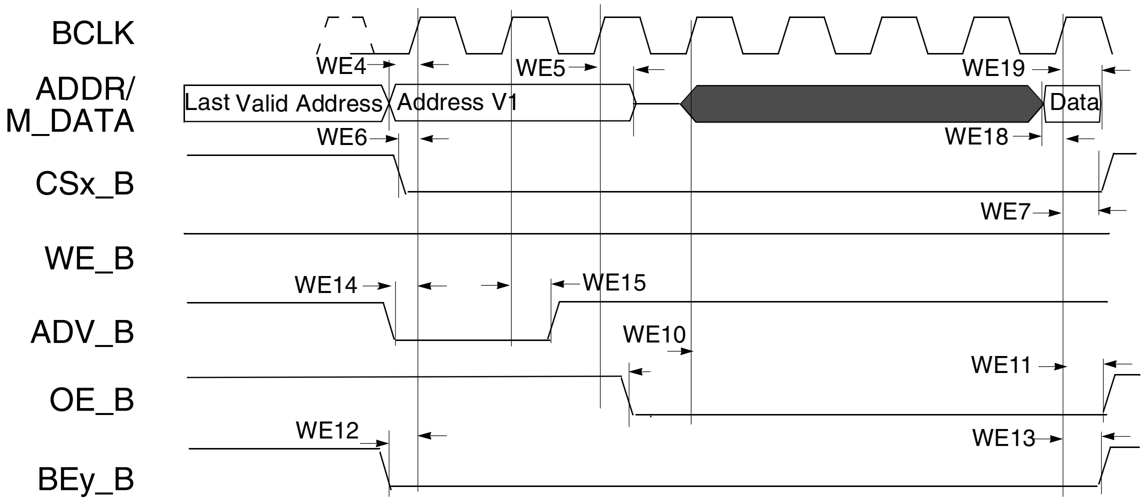

Figure 17. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.5 General EIM Timing-Asynchronous Mode

Figure 18 through Figure 22, and Table 44 help you determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 18 through Figure 21 as RWSC, OEN & CSN is configured differently. See the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for the EIM programming model.

Table 44. EIM Asynchronous Timing Parameters Table Relative Chip Select (continued)

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max (If 132 MHz is supported by SoC)	Unit
WE43	Input Data Valid to CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	CSx_B Valid to BEy_B Valid (Write access)	WE12 - WE6 + (WBEA - WCSA)	—	3 + (WBEA - WCSA)	ns
WE46	BEy_B Invalid to CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - WCSN)	—	-3 + (WBEN - WCSN)	ns
MAXDTI	DTACK MAXIMUM delay from chip dtack input to its internal FF + 2 cycles for synchronization	10	—	—	—
WE47	Dtack Active to CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	CSx_B Invalid to Dtack invalid	0	0	—	ns

1 For more information on configuration parameters mentioned in this table, see the i.MX 6Solo/6DualLite reference manual.
2 In this table, CSA means WCSA when write operation or RCSA when read operation.
3 In this table, CSN means WCSN when write operation or RCSN when read operation.
4 t is axi_clk cycle time.
5 In this table, ADVN means WADVN when write operation or RADVN when read operation.
6 In this table, ADVA means WADVA when write operation or RADVA when read operation.

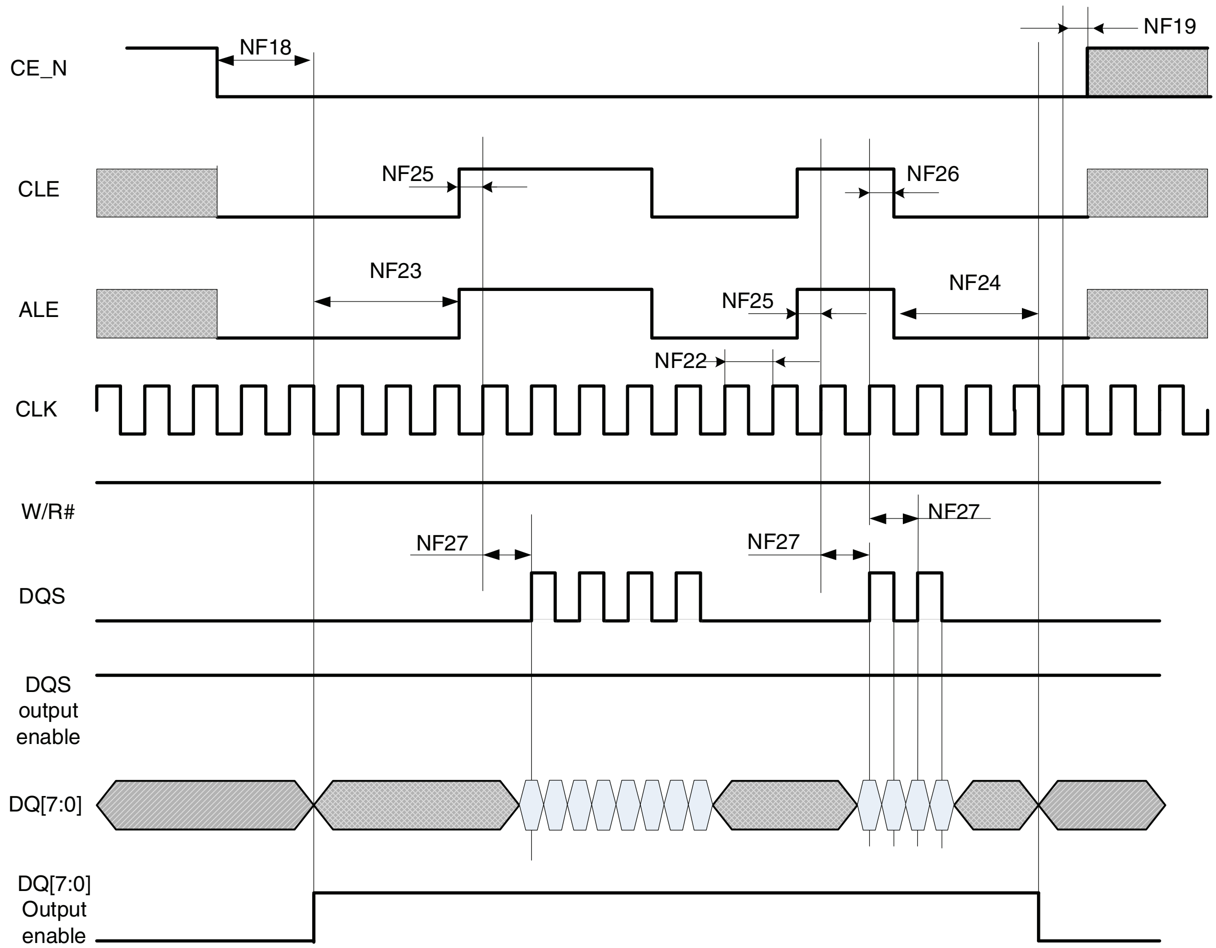

Figure 35. Source Synchronous Mode Data Write Timing Diagram

Table 53. Samsung Toggle Mode Timing Parameters (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF23	preamble delay	tPRE	(PRE_DELAY+1) x tCK	—	ns
NF24	postamble delay	tPOST	POST_DELAY x tCK	—	ns
NF25	CLE and ALE setup time	tCALS	0.5 x tCK	—	ns
NF26	CLE and ALE hold time	tCALH	0.5 x tCK	—	ns

For DDR Toggle mode, Figure 37 shows the timing diagram of DQS/DQ read valid window. The typical value of tDQSQ is 1.4 ns(max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI will sample DQ[7:0] at both rising and falling edge of an delayed DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the i.MX 6Solo/6DualLite reference manual). Generally, the typical delay value is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11 External Peripheral Interface Parameters

The following subsections provide information on external peripheral interfaces.

4.11.1 AUDMUX Timing Parameters

The AUDMUX provides a programmable interconnect logic for voice, audio, and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.11.2 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

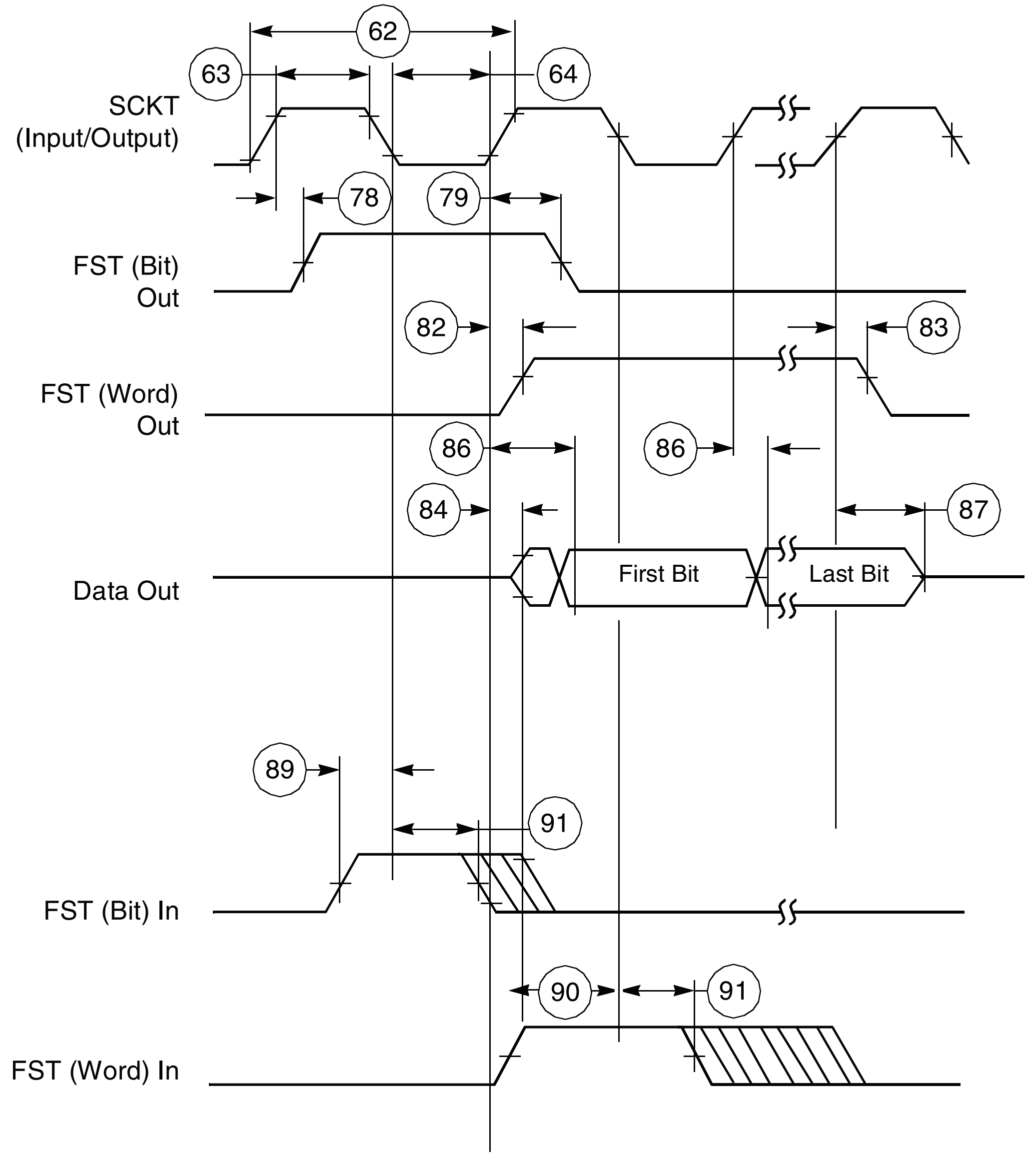

Figure 42. ESAI Transmitter Timing

Figure 48 shows MII transmit signal timings. Table 61 describes the timing parameters (M5–M8) shown in the figure.

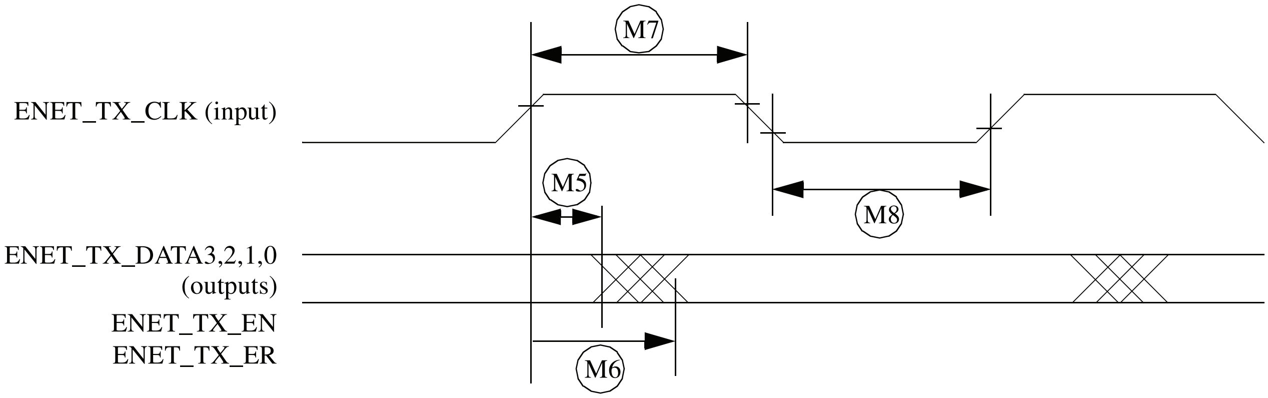

Figure 48. MII Transmit Signal Timing Diagram

Table 61. MII Transmit Signal Timing

ID	Characteristic[1]	Min.	Max.	Unit
M5	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid	5	—	ns
M6	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid	—	20	ns
M7	ENET_TX_CLK pulse width high	35%	65%	ENET_TX_CLK period
M8	ENET_TX_CLK pulse width low	35%	65%	ENET_TX_CLK period

[1] ENET_TX_EN, ENET_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

4.11.5.1.3 MII Asynchronous Inputs Signal Timing (ENET_CRS and ENET_COL)

Figure 49 shows MII asynchronous input timings. Table 62 describes the timing parameter (M9) shown in the figure.

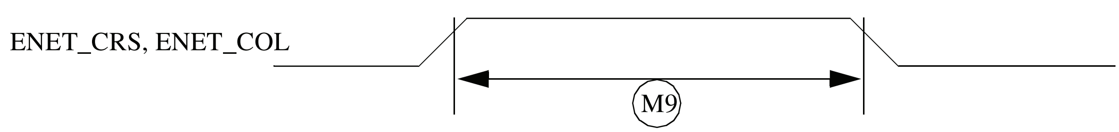

Figure 49. MII Async Inputs Timing Diagram

Table 62. MII Asynchronous Inputs Signal Timing

ID	Characteristic	Min.	Max.	Unit
M9[1]	ENET_CRS to ENET_COL minimum pulse width	1.5	—	ENET_TX_CLK period

[1] ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

4.11.5.1.4 MII Serial Management Channel Timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 50 shows MII asynchronous input timings. Table 63 describes the timing parameters (M10–M15) shown in the figure.

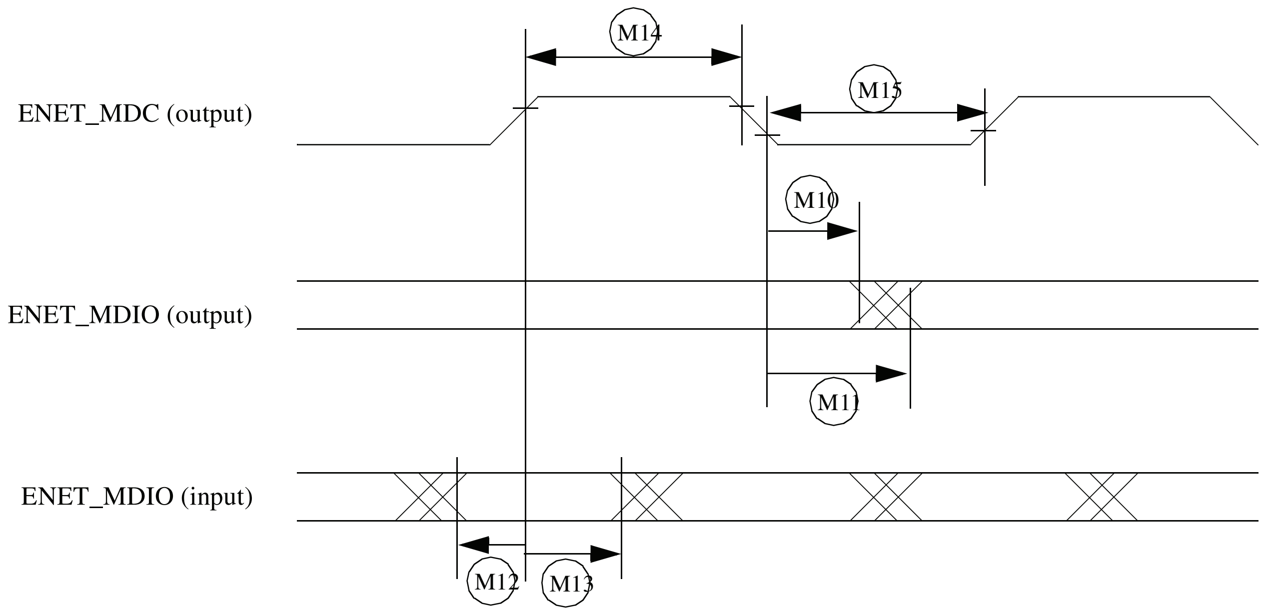

Figure 50. MII Serial Management Channel Timing Diagram

Table 63. MII Serial Management Channel Timing

ID	Characteristic	Min.	Max.	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

4.11.5.2 RMII Mode Timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the CRS_DV in RMII. Other signals under RMII mode include ENET_TX_EN, ENET0_TXD[1:0], ENET0_RXD[1:0] and ENET_RX_ER.

4.11.10.6.3 TFT Panel Sync Pulse Timing Diagrams

Figure 68 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All the parameters shown in the figure are programmable. All controls are started by corresponding internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC, and DRDY signals.

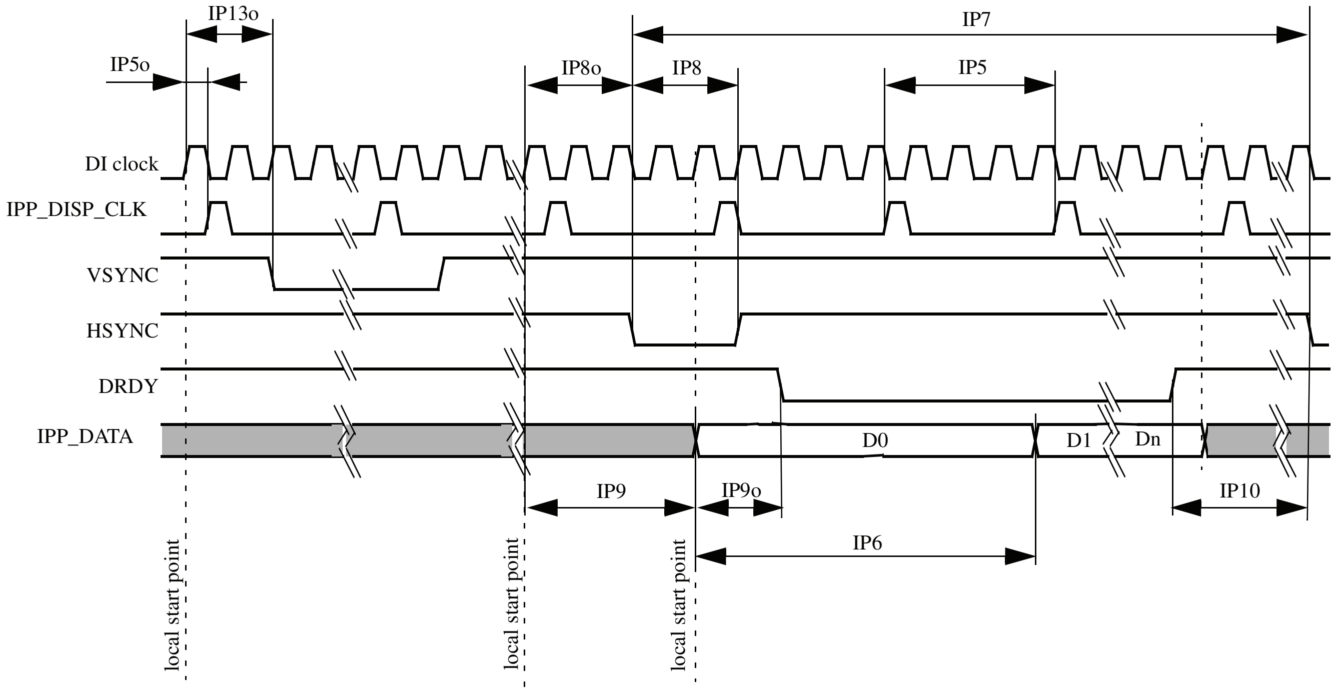

Figure 68. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 69 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

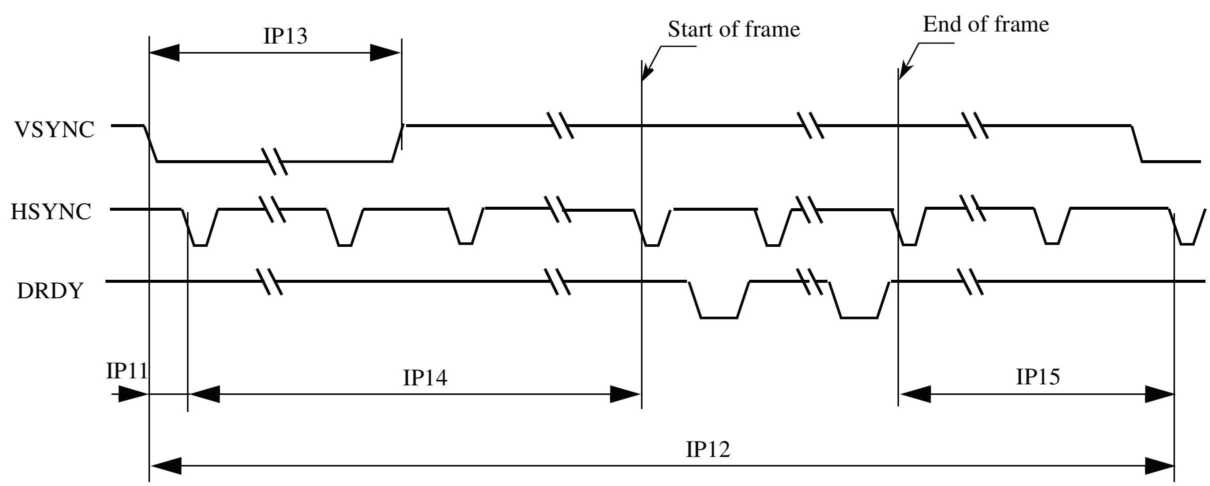

Figure 69. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 87. SSI Transmitter Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.11.21.2 Receive Timing

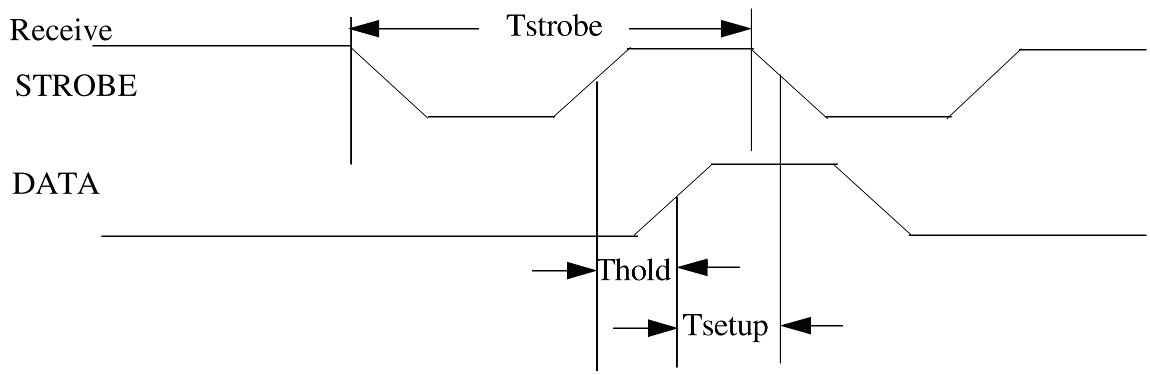

Figure 104. USB HSIC Receive Waveform

Table 97. USB HSIC Receive Parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	
Thold	data hold time	300		ps	Measured at 50% point
Tsetup	data setup time	365		ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

[1] The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.11.22 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0

6.1.2 21 x 21 mm Supplies Contact Assignments and Functional Contact Assignments

Table 100 shows supplies contact assignments for the 21 x 21 mm package.

Table 100. 21 x 21 mm Supplies Contact Assignments

Supply Rail Name	Ball(s) Position(s)	Remark
CSI_REXT	D4	
DRAM_VREF	AC2	
DSI_REXT	G4	
GND	A4, A8, A13, A25, B4, C1, C4, C6, C10, D3, D6, D8, E5, E6, E7, F5, F6, F7, F8, G3, G10, G19, H8, H12, H15, H18, J2, J8, J12, J15, J18, K8, K10, K12, K15, K18, L2, L5, L8, L10, L12, L15, L18, M8, M10, M12, M15, M18, N8, N10, N15, N18, P8, P10, P12, P15, P18, R8, R12, R15, R17, T8, T11, T12, T15, T17, T19, U8, U11, U12, U15, U17, U19, V8, V19, W3, W7, W8, W9, W10, W11, W12, W13, W15, W16, W17, W18, W19, Y5, Y24, AA7, AA10, AA13, AA16, AA19, AA22, AB3, AB24, AD4, AD7, AD10, AD13, AD16, AD19, AD22, AE1, AE25	
HDMI_REF	J1	
HDMI_VP	L7	
HDMI_VPH	M7	
NVCC_CSI	N7	Supply of the camera sensor interface
NVCC_DRAM	R18, T18, U18, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18	Supply of the DDR interface
NVCC_EIM	K19, L19, M19	Supply of the EIM interface
NVCC_ENET	R19	Supply of the ENET interface
NVCC_GPIO	P7	Supply of the GPIO interface
NVCC_JTAG	J7	Supply of the JTAG tap controller interface
NVCC_LCD	P19	Supply of the LCD interface
NVCC_LVDS2P5	V7	Supply of the LVDS display interface and DDR pre-drivers
NVCC_MIPI	K7	Supply of the MIPI interface
NVCC_NANDF	G15	Supply of the raw NAND Flash memories interface
NVCC_PLL_OUT	E8	
NVCC_RGMII	G18	Supply of the ENET interface
NVCC_SD1	G16	Supply of the SD card interface
NVCC_SD2	G17	Supply of the SD card interface
NVCC_SD3	G14	Supply of the SD card interface

Table 101. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
DISP0_DAT3	P21	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[24]	Input	100 kΩ pull-up
DISP0_DAT4	P20	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[25]	Input	100 kΩ pull-up
DISP0_DAT5	R25	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[26]	Input	100 kΩ pull-up
DISP0_DAT6	R23	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[27]	Input	100 kΩ pull-up
DISP0_DAT7	R24	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[28]	Input	100 kΩ pull-up
DISP0_DAT8	R22	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[29]	Input	100 kΩ pull-up
DISP0_DAT9	T25	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[30]	Input	100 kΩ pull-up
DRAM_A0	AC14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[0]	Output	Low
DRAM_A1	AB14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[1]	Output	Low
DRAM_A10	AA15	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[10]	Output	Low
DRAM_A11	AC12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[11]	Output	Low
DRAM_A12	AD12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[12]	Output	Low
DRAM_A13	AC17	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[13]	Output	Low
DRAM_A14	AA12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[14]	Output	Low
DRAM_A15	Y12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[15]	Output	Low
DRAM_A2	AA14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[2]	Output	Low
DRAM_A3	Y14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[3]	Output	Low
DRAM_A4	W14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[4]	Output	Low
DRAM_A5	AE13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[5]	Output	Low
DRAM_A6	AC13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[6]	Output	Low
DRAM_A7	Y13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[7]	Output	Low
DRAM_A8	AB13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[8]	Output	Low
DRAM_A9	AE12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[9]	Output	Low
DRAM_CAS	AE16	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_CAS	Output	Low
DRAM_CS0	Y16	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_CS[0]	Output	Low
DRAM_CS1	AD17	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_CS[1]	Output	Low
DRAM_D0	AD2	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[0]	Input	100 kΩ pull-up
DRAM_D1	AE2	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[1]	Input	100 kΩ pull-up
DRAM_D10	AA6	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[10]	Input	100 kΩ pull-up
DRAM_D11	AE7	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[11]	Input	100 kΩ pull-up

Table 101. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
EIM_D19	G21	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[19]	Input	100 kΩ pull-up
EIM_D20	G20	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[20]	Input	100 kΩ pull-up
EIM_D21	H20	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[21]	Input	100 kΩ pull-up
EIM_D22	E23	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[22]	Input	100 kΩ pull-down
EIM_D23	D25	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[23]	Input	100 kΩ pull-up
EIM_D24	F22	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[24]	Input	100 kΩ pull-up
EIM_D25	G22	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[25]	Input	100 kΩ pull-up
EIM_D26	E24	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[26]	Input	100 kΩ pull-up
EIM_D27	E25	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[27]	Input	100 kΩ pull-up
EIM_D28	G23	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[28]	Input	100 kΩ pull-up
EIM_D29	J19	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[29]	Input	100 kΩ pull-up
EIM_D30	J20	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[30]	Input	100 kΩ pull-up
EIM_D31	H21	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[31]	Input	100 kΩ pull-down
EIM_DA0	L20	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[0]	Input	100 kΩ pull-up
EIM_DA1	J25	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[1]	Input	100 kΩ pull-up
EIM_DA10	M22	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[10]	Input	100 kΩ pull-up
EIM_DA11	M20	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[11]	Input	100 kΩ pull-up
EIM_DA12	M24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[12]	Input	100 kΩ pull-up
EIM_DA13	M23	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[13]	Input	100 kΩ pull-up
EIM_DA14	N23	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[14]	Input	100 kΩ pull-up
EIM_DA15	N24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[15]	Input	100 kΩ pull-up
EIM_DA2	L21	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[2]	Input	100 kΩ pull-up
EIM_DA3	K24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[3]	Input	100 kΩ pull-up
EIM_DA4	L22	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[4]	Input	100 kΩ pull-up
EIM_DA5	L23	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[5]	Input	100 kΩ pull-up
EIM_DA6	K25	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[6]	Input	100 kΩ pull-up
EIM_DA7	L25	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[7]	Input	100 kΩ pull-up
EIM_DA8	L24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[8]	Input	100 kΩ pull-up
EIM_DA9	M21	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[9]	Input	100 kΩ pull-up
EIM_EB0	K21	NVCC_EIM	GPIO	ALT0	weim.WEIM_EB[0]	Output	High