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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	DDR3, DDR3L, LPDDR2
Graphics Acceleration	Yes
Display & Interface Controllers	HDMI, Keypad, LCD, LVDS, MIPI
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6u1avm08acr

- Snoop Control Unit (SCU)
- 512 KB unified I/D L2 cache:
  - Used by one core in i.MX 6Solo
  - Shared by two cores in i.MX 6DualLite
- Two Master AXI bus interfaces output of L2 cache
- Frequency of the core (including Neon and L1 cache), as per Table 9, "Operating Ranges," on page 24.
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The memory system consists of the following components:

- Level 1 Cache—32 KB Instruction, 32 KB Data cache per core
- Level 2 Cache—Unified instruction and data (512 KB)
- On-Chip Memory:
  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 128 KB)
  - Secure/non-secure RAM (16 KB)
- External memory interfaces: The i.MX 6Solo/6DualLite processors support latest, high volume, cost effective handheld DRAM, NOR, and NAND Flash memory standards.
  - 16/32-bit LP-DDR2-800, 16/32-bit DDR3-800 and LV-DDR3-800 in i.MX 6Solo; 16/32/64-bit LP-DDR2-800, 16/32/64-bit DDR3-800 and LV-DDR3-800, supporting DDR interleaving mode for 2x32 LPDDR2-800 in i.MX 6DualLite
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bit.
  - 16/32-bit NOR Flash. All WEIMv2 pins are muxed on other interfaces.
  - 16/32-bit PSRAM, Cellular RAM

Each i.MX 6Solo/6DualLite processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Displays—Total four interfaces available. Total raw pixel rate of all interfaces is up to 450 Mpixels/sec, 24 bpp. Up to two interfaces may be active in parallel.
  - One Parallel 24-bit display port, up to 225 Mpixels/sec (for example, WUXGA at 60 Hz or dual HD1080 and WXGA at 60 Hz)
  - LVDS serial ports—One port up to 165 Mpixels/sec or two ports up to 85 MP/sec (for example, WUXGA at 60 Hz) each
  - HDMI 1.4 port

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface, which is used on the AP to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options. The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.
TEMPMON	Temperature Monitor	System Control Peripherals	The Temperature sensor IP is used for detecting die temperature. The temperature read out does not reflect case or ambient temperature. It reflects the temperature in proximity of the sensor location on the die. Temperature distribution may not be uniformly distributed, therefore the read out value may not be the reflection of the temperature value of the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 4 MHz. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard and the i.MX31 UART modules. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOH3	USB 2.0 High Speed OTG and 3x HS Hosts	Connectivity Peripherals	USBOH3 contains: • One high-speed OTG module with integrated HS USB PHY • One high-speed Host module with integrated HS USB PHY • Two identical high-speed Host modules connected to HSIC USB ports.
VDOA	VDOA	Multimedia Peripherals	Video Data Order Adapter (VDOA): used to re-order video data from the “tiled” order used by the VPU to the conventional raster-scan order needed by the IPU.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
VPU	Video Processing Unit	Multimedia Peripherals	A high-performing video processing unit (VPU), which covers many SD-level and HD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing, such as rotation and mirroring. See the i.*MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for complete list of VPU's decoding/encoding capabilities.
WDOG-1	Watch Dog	Timer Peripherals	The Watch Dog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watch Dog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW.
WEIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The WEIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
XTALOSC	Crystal Oscillator I/F	Clocks, Resets, and Power Control	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator to provide USB required frequency.

Table 27 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 27. LVDS I/O DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Differential Voltage	VOD	Rload-100 Ω Diff	250	350	450	mV
Output High Voltage	VOH	IOH = 0 mA	1.25	1.375	1.6	V
Output Low Voltage	VOL	IOL = 0 mA	0.9	1.025	1.25	V
Offset Voltage	VOS		1.125	1.2	1.375	V

4.6.4 MLB I/O DC Parameters

The MLB interface complies with Analog Interface of 6-pin differential Media Local Bus specification version 4.1. See 6-pin differential MLB specification v4.1, “MediaLB 6-pin interface Electrical Characteristics” for details.

NOTE

The MLB 6-pin interface does not support speed mode 8192 fs.

Table 28 shows the Media Local Bus (MLB) I/O DC parameters.

Table 28. MLB I/O DC Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Differential Voltage	VOD	Rload-50Ω Diff	300	500	mV
Output High Voltage	VOH	Rload-50Ω Diff	1.25	1.75	V
Output Low Voltage	VOL	Rload-50Ω Diff	0.75	1.25	V
Common-mode output voltage ((Vpadp*+Vpadn*)/2)	Vocm	Rload-50Ω Diff	1	1.5	V
Differential output impedance	Zo		1.6		kΩ

4.7 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O
- MLB I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 4 and Figure 5.

Table 33 shows the AC parameters for LVDS I/O.

Table 33. I/O AC Parameters of LVDS Pad

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential pulse skew[1]	t_{SKD}	Rload = 100 Ω, Cload = 2 pF	—	—	0.25	ns
Transition Low to High Time[2]	t_{TLH}		—	—	0.5	
Transition High to Low Time[2]	t_{THL}		—	—	0.5	
Operating Frequency	f	—	—	600	800	MHz
Offset voltage imbalance	Vos	—	—	—	150	mV

1 t_{SKD} = | t_{PHLD} - t_{PLHD} |, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

2 Measurement levels are 20-80% from output voltage.

4.7.4 MLB I/O AC Parameters

The differential output transition time waveform is shown in Figure 7.

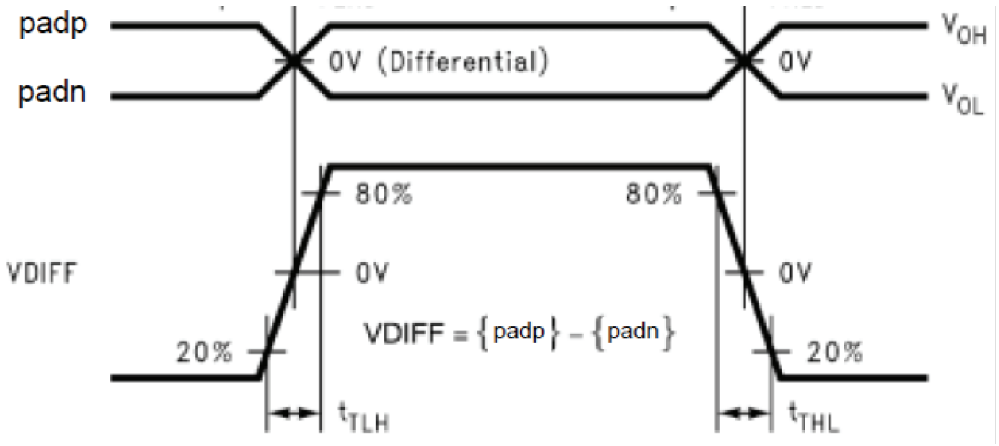


Figure 7. Differential MLB Driver Transition Time Waveform

A 4-stage pipeline is utilized in the MLB 6-pin implementation in order to facilitate design, maximize throughput, and allow for reasonable PCB trace lengths. Each cycle is one ipp_clk_in* (internal clock from MLB PLL) clock period. Cycles 2, 3, and 4 are MLB PHY related. Cycle 2 includes clock-to-output delay of Signal/Data sampling flip-flop and Transmitter, Cycle 3 includes clock-to-output delay of Signal/Data clocked receiver, Cycle 4 includes clock-to-output delay of Signal/Data sampling flip-flop.

MLB 6-pin pipeline diagram is shown in Figure 8.

4.8.1 GPIO Output Buffer Impedance

Table 35 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 35. GPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	260 130 90 60 50 40 33	Ω

Table 36 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 36. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	150 75 50 37 30 25 20	Ω

4.8.2 DDR I/O Output Buffer Impedance

The LPDDR2 interface fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 37 shows DDR I/O output buffer impedance of i.MX 6Solo/6DualLite processors.

Table 37. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions DSE(Drive Strength)	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	000 001 010 011 100 101 110 111	Hi-Z 240 120 80 60 48 40 34	Hi-Z 240 120 80 60 48 40 34	Ω

Note:
1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.

4.9.3.3 General EIM Timing-Synchronous Mode

Figure 12, Figure 13, and Table 43 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

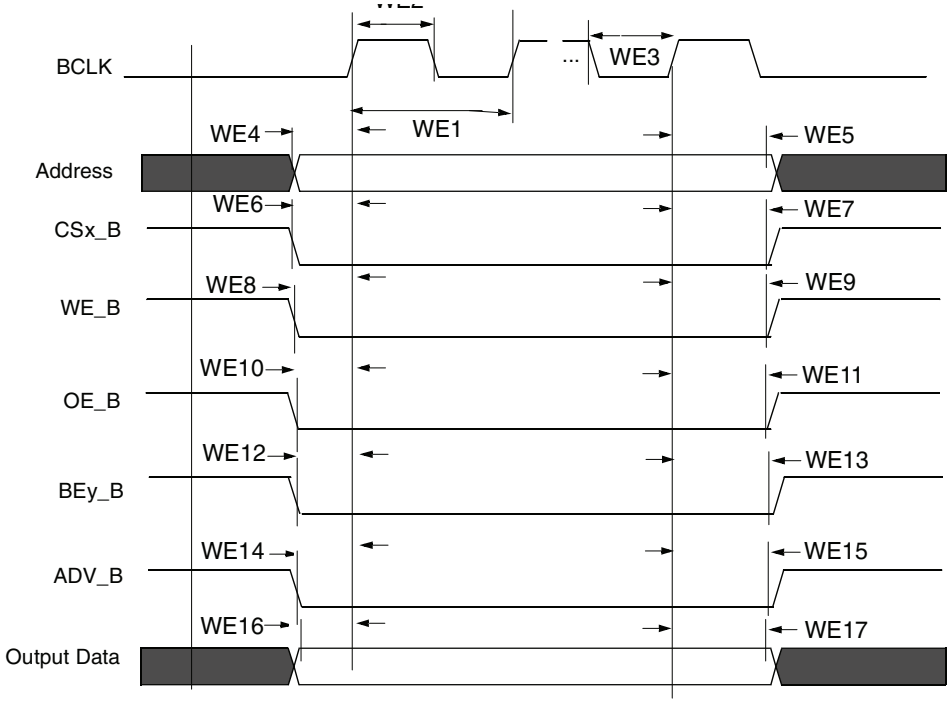


Figure 12. EIM Outputs Timing Diagram

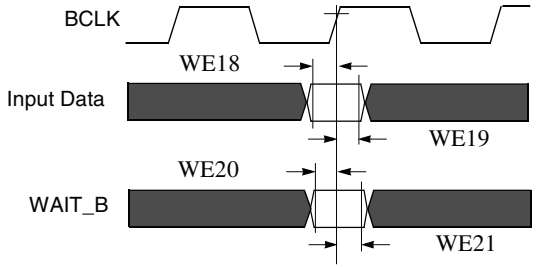


Figure 13. EIM Inputs Timing Diagram

Figure 29 shows the read timing parameters. The timing parameters for this diagram appear in Table 50.

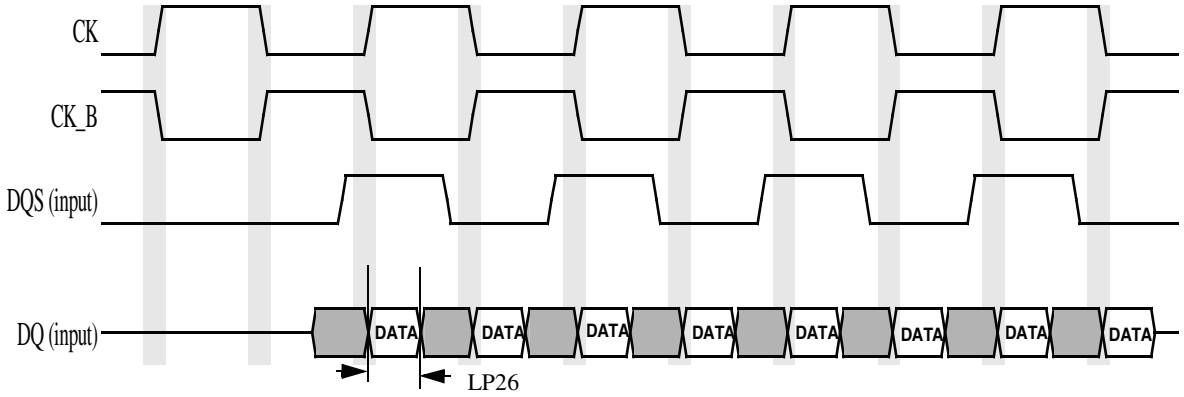


Figure 29. LPDDR2 Read Cycle

Table 50. LPDDR2 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP26	Minimum required DQ valid window width for LPDDR2	—	270	—	ps

1 To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

2 All measurements are in reference to Vref level.

3 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

4.10 General-Purpose Media Interface (GPMI) Timing

The i.MX 6Solo/6DualLite GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous timing mode, Source Synchronous timing mode and Samsung Toggle timing mode separately described in the following subsections.

4.10.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The maximum I/O speed of GPMI in asynchronous mode is about 50 MB/s. Figure 30 through Figure 33 depicts the relative timing between GPMI signals at the module level for different operations under asynchronous mode. Table 51 describes the timing parameters (NF1–NF17) that are shown in the figures.

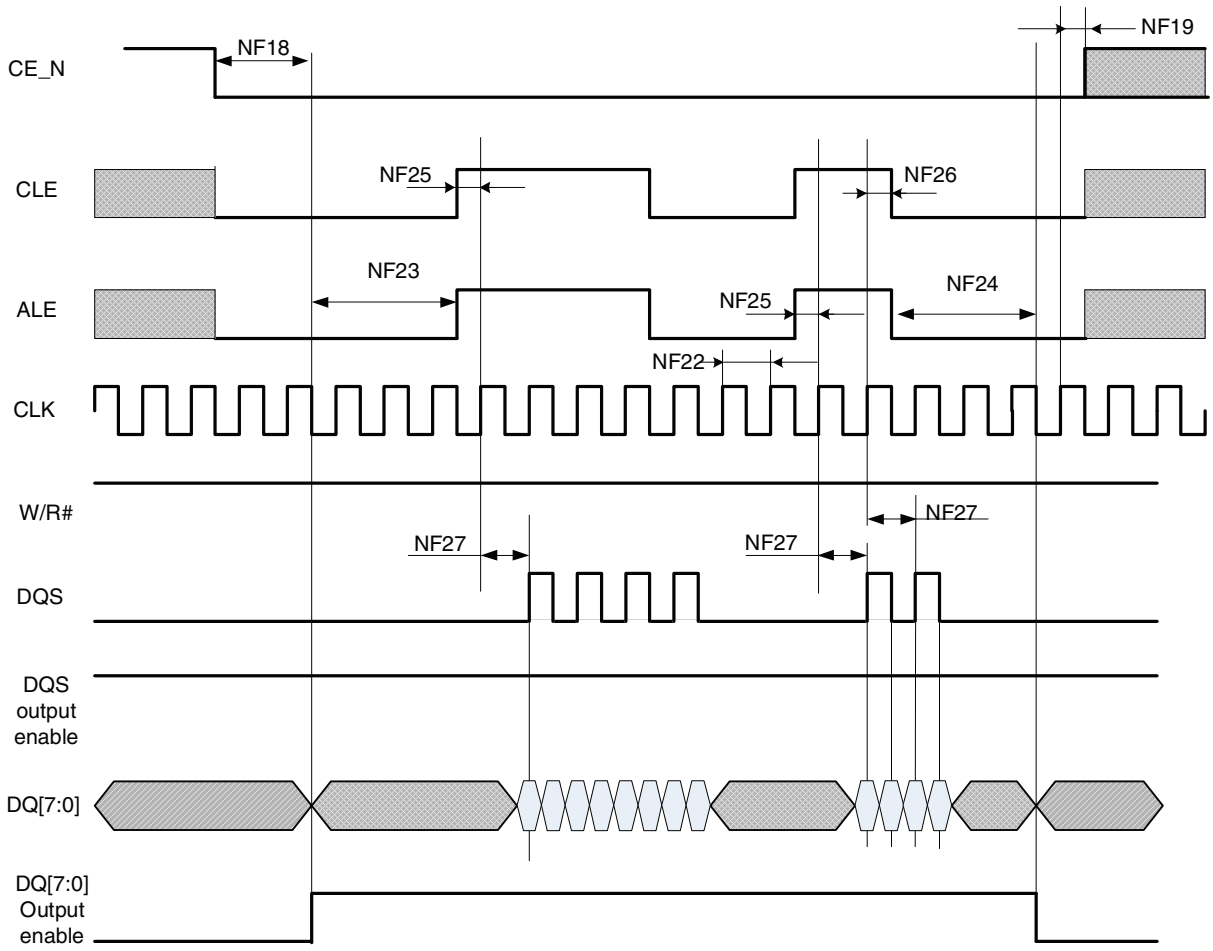


Figure 35. Source Synchronous Mode Data Write Timing Diagram

Table 52. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	tCE	CE_DELAY x tCK	—	ns
NF19	CE# hold time	tCH	0.5 x tCK	—	ns
NF20	Command/address DQ setup time	tCAS	0.5 x tCK	—	ns
NF21	Command/address DQ hold time	tCAH	0.5 x tCK	—	ns
NF22	clock period	tCK	5	--	ns
NF23	preamble delay	tPRE	PRE_DELAY x tCK	—	ns
NF24	postamble delay	tPOST	POST_DELAY x tCK	—	ns
NF25	CLE and ALE setup time	tCALS	0.5 x tCK	—	ns
NF26	CLE and ALE hold time	tCALH	0.5 x tCK	—	ns
NF27	Data input to first DQS latching transition	tDQSS	tCK	—	ns

1 GPMI's Sync Mode output timing could be controlled by module's internal registers, say HW_GPMI_TIMING2_CE_DELAY, HW_GPMI_TIMING_PREAMBLE_DELAY, and HW_GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers' settings. In the above table, we use CE_DELAY/PRE_DELAY/POST_DELAY to represent each of these settings.

For DDR Source sync mode, Figure 37 shows the timing diagram of DQS/DQ read valid window. The typical value of tDQSQ is 0.85ns (max) and 1ns (max) for tQHS at 200MB/s. GPMI will sample DQ[7:0] at both rising and falling edge of an delayed DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET(see the GPMI chapter of the i.MX 6Solo/6DualLite reference manual). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.10.3 Samsung Toggle Mode AC Timing

4.10.3.1 Command and Address Timing

NOTE

Samsung Toggle Mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 4.10.1, "Asynchronous Mode AC Timing (ONFI 1.0 Compatible)," for details.

4.11.2.2 ECSPI Slave Mode Timing

Figure 41 depicts the timing of ECSPI in slave mode. Table 55 lists the ECSPI slave mode timing characteristics.

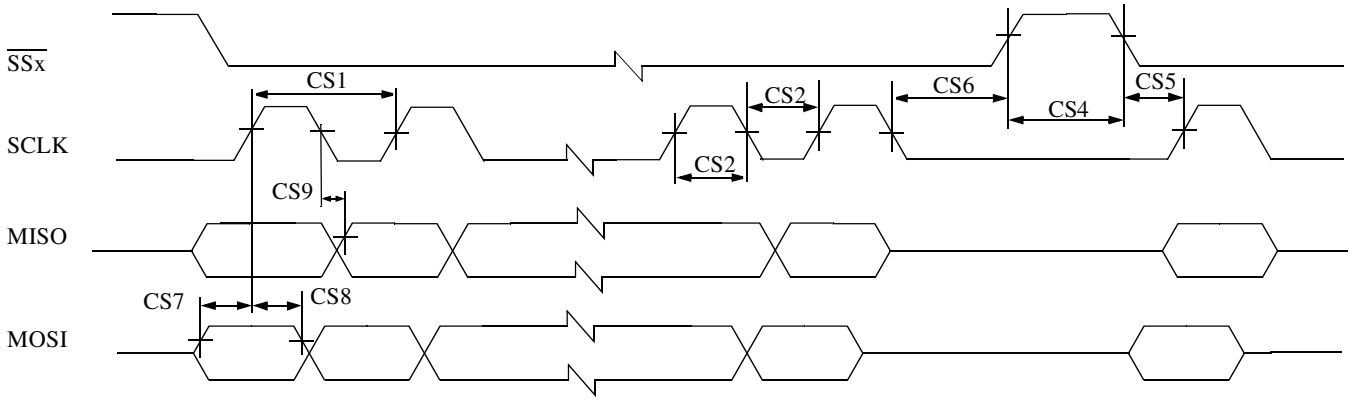


Figure 41. ECSPI Slave Mode Timing Diagram

Table 55. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time–Read SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	SCLK High or Low Time–Read SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	19	ns

Table 76. Electrical and Timing Information

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
$\Delta V_{CMTX(LF)}$	Common level variation between 50 MHz and 450 MHz.	80 Ω<= RL< = 125 Ω			25	mV_p
LP Line Drivers AC Specifications						
t_{rlp}, t_{flp}	Single ended output rise/fall time	15% to 85%, C_L<70 pF			25	ns
t_{reo}		30% to 85%, C_L<70 pF			35	ns
$\delta V/\delta t_{SR}$	Signal slew rate	15% to 85%, C_L<70 pF			120	mV/ns
C_L	Load capacitance		0		70	pF
HS Line Receiver AC Specifications						
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz				200	mVpp
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 MHz and 450 MHz.		-50		50	mVpp
C_{CM}	Common mode termination				60	pF
LP Line Receiver AC Specifications						
e_{SPIKE}	Input pulse rejection				300	Vps
T_{MIN}	Minimum pulse response		50			ns
V_{INT}	Pk-to-Pk interference voltage				400	mV
f_{INT}	Interference frequency		450			MHz
Model Parameters used for Driver Load switching performance evaluation						
C_{PAD}	Equivalent Single ended I/O PAD capacitance.				1	pF
C_{PIN}	Equivalent Single ended Package + PCB capacitance.				2	pF
L_S	Equivalent wire bond series inductance				1.5	nH
R_S	Equivalent wire bond series resistance				0.15	Ω
R_L	Load resistance		80	100	125	Ω

4.11.12.6 High-Speed Clock Timing

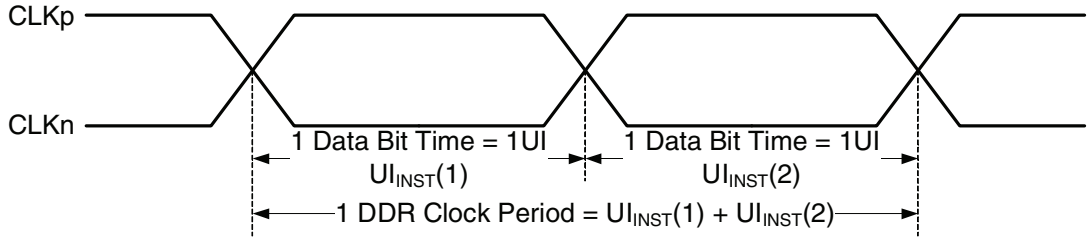
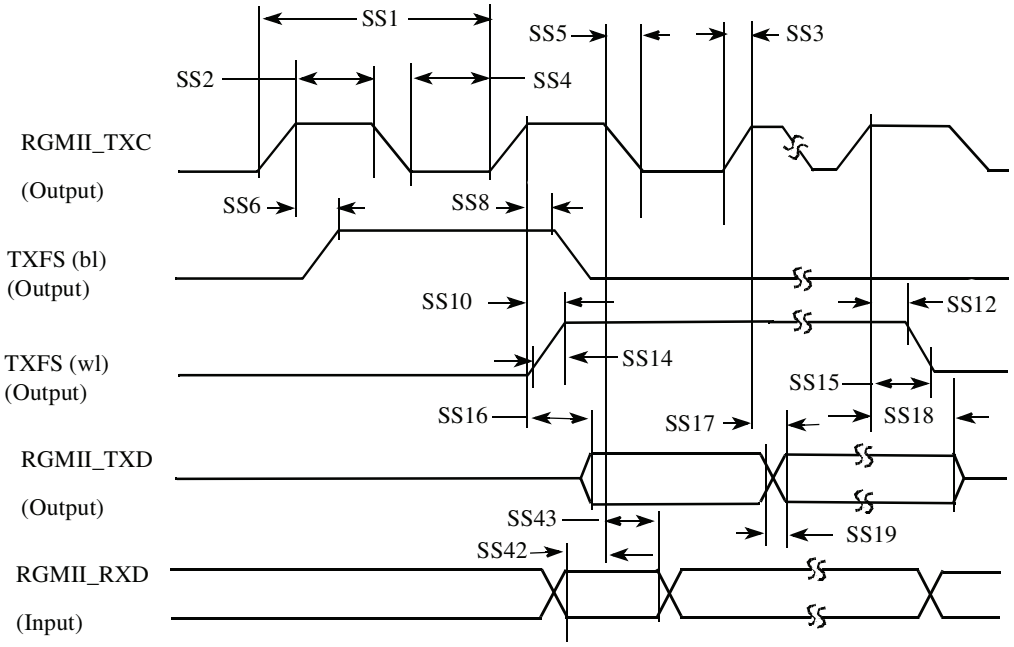


Figure 74. DDR Clock Definition

4.11.19.1 SSI Transmitter Timing with Internal Clock

Figure 95 depicts the SSI transmitter internal clock timing and Table 87 lists the timing parameters for the SSI transmitter internal clock.



Note: SRXD input in synchronous mode only

Figure 95. SSI Transmitter Internal Clock Timing Diagram

Table 87. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6.0	ns
SS15	(Tx/Rx) Internal FS fall time	—	6.0	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns

4.11.19.2 SSI Receiver Timing with Internal Clock

Figure 96 depicts the SSI receiver internal clock timing and Table 88 lists the timing parameters for the receiver timing with the internal clock.

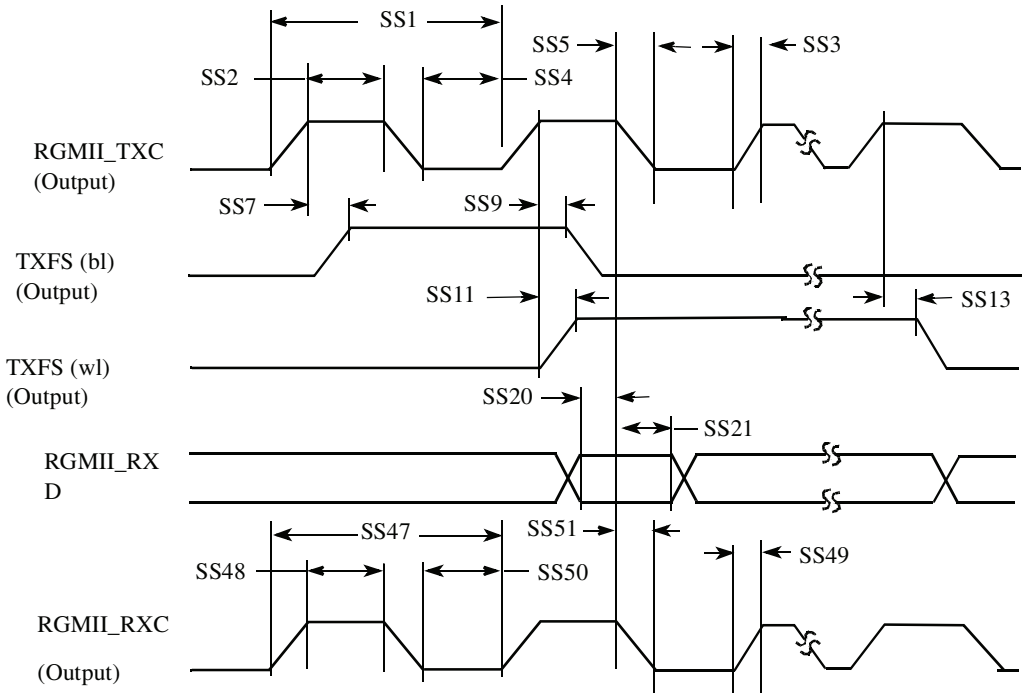


Figure 96. SSI Receiver Internal Clock Timing Diagram

Table 88. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0.0	—	ns
Oversampling Clock Operation				

Table 89. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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TITLE: PBGA, LOW PROFILE, FINE PITCH, 624 I/O, 21 X 21 PKG, 0.8 MM PITCH (MAP)		DOCUMENT NO: 98ASA00404D	REV: O
		CASE NUMBER: 2240–01	27 SEP 2011
		STANDARD: NON–JEDEC	

Figure 105. 21 x 21 mm BGA, Case 2240 Package Top, Bottom, and Side Views

Table 100. 21 x 21 mm Supplies Contact Assignments (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
PCIE_REXT	A2	
PCIE_VP	H7	
PCIE_VPH	G7	PCI PHY supply
PCIE_VPTX	G8	PCI PHY supply
VDD_SNVS_CAP	G9	Secondary supply for the SNVS (internal regulator output—requires capacitor if internal regulator is used)
VDD_SNVS_IN	G11	Primary supply for the SNVS regulator
VDDARM_CAP	H11, H13, J11, J13, K11, K13, L11, L13, M11, M13, N11, N13, P11, P13, R11, R13	Secondary supply for core (internal regulator output—requires capacitor if internal regulator is used)
VDDARM_IN	H14, J14, K9, K14, L9, L14, M9, M14, N9, N14, P9, P14, R9, R14, T9, U9	Primary supply for the ARM core's regulator
VDDHIGH_CAP	H10, J10	Secondary supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)
VDDHIGH_IN	H9, J9	Primary supply for the 2.5 V regulator
VDDPU_CAP	H17, J17, K17, L17, M17, N17, P17	Secondary supply for VPU and GPUs (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_CAP	R10, T10, T13, T14, U10, U13, U14	Secondary supply for SoC and PU regulators (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_IN	H16, J16, K16, L16, M16, N16, P16, R16, T16, U16	Primary supply for SoC and PU regulators
VDDUSB_CAP	F9	Secondary supply for the 3 V Domain (internal regulator output—requires capacitor if internal regulator is used)
USB_H1_VBUS	D10	Primary supply for the 3 V regulator
USB_OTG_VBUS	E9	Primary supply for the 3 V regulator
HDMI_DDCCEC	K2	Analog Ground(Ground reference for the Hot Plug Detect signal)
FA_ANA	A5	
GPANAIO	C8	
VDD_FA	B5	
ZQPAD	AE17	
NC	C14	
NC	G12	

Table 101. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
LVDS0_TX1_N	U4	NVCC_LVDS2P5					
LVDS0_TX1_P	U3	NVCC_LVDS2P5		ALT0	ldb.LVDS0_TX1	Input	Keeper
LVDS0_TX2_N	V2	NVCC_LVDS2P5					
LVDS0_TX2_P	V1	NVCC_LVDS2P5		ALT0	ldb.LVDS0_TX2	Input	Keeper
LVDS0_TX3_N	W2	NVCC_LVDS2P5					
LVDS0_TX3_P	W1	NVCC_LVDS2P5		ALT0	ldb.LVDS0_TX3	Input	Keeper
LVDS1_CLK_N	Y3	NVCC_LVDS2P5					
LVDS1_CLK_P	Y4	NVCC_LVDS2P5		ALT0	ldb.LVDS1_CLK	Input	Keeper
LVDS1_TX0_N	Y1	NVCC_LVDS2P5					
LVDS1_TX0_P	Y2	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX0	Input	Keeper
LVDS1_TX1_N	AA2	NVCC_LVDS2P5					
LVDS1_TX1_P	AA1	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX1	Input	Keeper
LVDS1_TX2_N	AB1	NVCC_LVDS2P5					
LVDS1_TX2_P	AB2	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX2	Input	Keeper
LVDS1_TX3_N	AA3	NVCC_LVDS2P5					
LVDS1_TX3_P	AA4	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX3	Input	Keeper
MLB_CN	A11	VDDHIGH_CAP					
MLB_CP	B11	VDDHIGH_CAP					
MLB_DN	B10	VDDHIGH_CAP					
MLB_DP	A10	VDDHIGH_CAP					
MLB_SN	A9	VDDHIGH_CAP					
MLB_SP	B9	VDDHIGH_CAP					
NANDF_ALE	A16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[8]	Input	100 kΩ pull-up
NANDF_CLE	C15	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[7]	Input	100 kΩ pull-up
NANDF_CS0	F15	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[11]	Input	100 kΩ pull-up
NANDF_CS1	C16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[14]	Input	100 kΩ pull-up
NANDF_CS2	A17	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[15]	Input	100 kΩ pull-up
NANDF_CS3	D16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[16]	Input	100 kΩ pull-up
NANDF_D0	A18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[0]	Input	100 kΩ pull-up
NANDF_D1	C17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[1]	Input	100 kΩ pull-up

Table 102. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

R	P	N	M	L	K	J	H
GPIO_17	CSI0_PIXCLK	CSI0_DAT4	CSI0_DAT10	CSI0_DAT13	HDMI_HPD	HDMI_REF	DSI_D1P
GPIO_16	CSI0_DAT5	CSI0_VSYNC	CSI0_DAT12	GND	HDMI_DDCCEC	GND	DSI_D1M
GPIO_7	CSI0_DATA_EN	CSI0_DAT7	CSI0_DAT11	CSI0_DAT17	HDMI_D2M	HDMI_D1M	DSI_CLK0M
GPIO_5	CSI0_MCLK	CSI0_DAT6	CSI0_DAT14	CSI0_DAT16	HDMI_D2P	HDMI_D1P	DSI_CLK0P
GPIO_8	GPIO_19	CSI0_DAT9	CSI0_DAT15	GND	HDMI_D0M	HDMI_CLKM	JTAG_TCK
GPIO_4	GPIO_18	CSI0_DAT8	CSI0_DAT18	CSI0_DAT19	HDMI_D0P	HDMI_CLKP	JTAG_MOD
GPIO_3	NVCC_GPIO	NVCC_CSI	HDMI_VPH	HDMI_VP	NVCC_MIPI	NVCC_JTAG	PCIE_VP
GND	GND	GND	GND	GND	GND	GND	GND
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDHIGH_IN	VDDHIGH_IN
VDDSOC_CAP	GND	GND	GND	GND	GND	VDDHIGH_CAP	VDDHIGH_CAP
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
GND	GND	NC	GND	GND	GND	GND	GND
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN
GND	GND	GND	GND	GND	GND	GND	GND
VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN
GND	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP
NVCC_DRAM	GND	GND	GND	GND	GND	GND	GND
NVCC_ENET	NVCC_LCD	DI0_DISP_CLK	NVCC_EIM	NVCC_EIM	NVCC_EIM	EIM_D29	EIM_A25
DISP0_DAT13	DISP0_DAT4	DI0_PIN3	EIM_DA11	EIM_DA0	EIM_RW	EIM_D30	EIM_D21
DISP0_DAT10	DISP0_DAT3	DI0_PIN15	EIM_DA9	EIM_DA2	EIM_EB0	EIM_A23	EIM_D31
DISP0_DAT8	DISP0_DAT1	EIM_BCLK	EIM_DA10	EIM_DA4	EIM_LBA	EIM_A18	EIM_A20
DISP0_DAT6	DISP0_DAT2	EIM_DA14	EIM_DA13	EIM_DA5	EIM_EB1	EIM_CS1	EIM_A21
DISP0_DAT7	DISP0_DAT0	EIM_DA15	EIM_DA12	EIM_DA8	EIM_DA3	EIM_OE	EIM_CS0
DISP0_DAT5	DI0_PIN4	DI0_PIN2	EIM_WAIT	EIM_DA7	EIM_DA6	EIM_DA1	EIM_A16
R	P	N	M	L	K	J	H

7 Revision History

Table 104 provides a revision history for this datasheet.

Table 104. i.MX 6Solo/6DualLite Datasheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 1	11/2012	• Updated Table 1, "Orderable Part Numbers," on page 3. • Updated Figure 1, "Part Number Nomenclature—i.MX 6DualLite and 6Solo," on page 4. • In Section 1.2, “Features,” added a footnote on the bottom of page 6 to specify performance limitation of 1 Gbps ENET. • In Table 7, "Absolute Maximum Ratings," on page 22, added details of VDD_SNVS_IN parameter. • Updated Table 9, "Operating Ranges," on page 24. • In Table 10, "On-Chip LDOs and their On-Chip Loads," on page 25, removed VDD_CACHE_CAP load. • Updated Table 12, "Maximal Supply Currents," on page 27. • Updated Table 15, "PCIe PHY Current Drain," on page 30. • Updated Table 16, "HDMI PHY Current Drain," on page 31. • In Table 23, "OSC32K Main Characteristics," on page 36, added 100 kΩ as ESR parameter max value. • Updated Table 27, "LVDS I/O DC Characteristics," on page 41. • In Table 42, "EIM Internal Module Multiplexing," on page 51, Multiplexed Address/Data mode, 16 Bit column, changed DSZ value to “001.” • In Table 54, "ECSPI Master Mode Timing Parameters," on page 78, updated CS5 and CS6 min values. • Updated Table 64, "RMII Signal Timing," on page 91. • Updated Section 4.11.5.3, “RGMII Signal Switching Specifications.” • Updated Section 4.11.6, “Flexible Controller Area Network (FLEXCAN) AC Electrical Specifications.” • Updated Table 64, "RMII Signal Timing," on page 91. • In Table 76, "Electrical and Timing Information," on page 116, updated $\Delta V_{CMTX(LF)}$ max value. • Updated Figure 88, "PWM Timing," on page 127. • Updated Table 83, "PWM Output Timing Parameters," on page 127. • Updated Section 4.11.22, “USB PHY Parameters.”
Rev. 0	10/2012	Initial public release.