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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	ARM® Cortex® -A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx6u4avm08ab

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
512x8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6Solo/6DualLite processors consist of 512x8-bit fuse box accessible through OCOTP_CTRL interface.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPMI	General Media Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices. 40-bit ECC encryption/decryption for NAND Flash controller (GPMI2). The GPMI supports separate DMA channels per NAND device.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU3Dv5	Graphics Processing Unit, ver.5	Multimedia Peripherals	The GPU3Dv5 provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays up to HD1080 resolution. The GPU3D provides OpenGL ES 2.0, including extensions, OpenGL ES 1.1, and OpenVG 1.1
GPU2Dv2	Graphics Processing Unit-2D, ver 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.
HDMI Tx	HDMI Tx i/f	Multimedia Peripherals	The HDMI module provides HDMI standard i/f port to an HDMI 1.4 compliant display.
HSI	MIPI HSI i/f	Connectivity Peripherals	The MIPI HSI provides a standard MIPI interface to the applications processor.
I ² C-1 I ² C-2 I ² C-3 I ² C-4	I ² C Interface	Connectivity Peripherals	I ² C provide serial interface for external devices. Data rates of up to 400 kbps are supported.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
VPU	Video Processing Unit	Multimedia Peripherals	A high-performing video processing unit (VPU), which covers many SD-level and HD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing, such as rotation and mirroring. See the <i>i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)</i> for complete list of VPU's decoding/encoding capabilities.
WDOG-1	Watch Dog	Timer Peripherals	The Watch Dog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watch Dog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW.
WEIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The WEIM NOR-FLASH / PSRAM provides: <ul style="list-style-type: none"> • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
XTALOSC	Crystal Oscillator I/F	Clocks, Resets, and Power Control	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator to provide USB required frequency.

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6Solo/6DualLite processors.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See [Table 6](#) for a quick reference to the individual tables and sections.

Table 6. i.MX 6Solo/6DualLite Chip-Level Conditions

For these characteristics, ...	Topic appears ...
Absolute Maximum Ratings	on page 22
BGA Case 2240 Package Thermal Resistance	on page 23
Operating Ranges	on page 24
External Clock Sources	on page 26
Maximal Supply Currents	on page 27
Low Power Mode Supply Currents	on page 29
USB PHY Current Consumption	on page 30
PCIe 2.0 Power Consumption	on page 30

4.1.1 Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core supply voltages	VDDARM_IN VDDSOC_IN	-0.3	1.5	V
Internal supply voltages	VDDARM_CAP VDDSOC_CAP VDDPU_CAP	-0.3	1.3	V
GPIO supply voltage	Supplies denoted as I/O supply	-0.5	3.6	V
DDR I/O supply voltage	Supplies denoted as I/O supply	-0.4	1.975	V
MLB I/O supply voltage	Supplies denoted as I/O supply	-0.3	2.8	V
LVDS I/O supply voltage	Supplies denoted as I/O supply	-0.3	2.8	V
VDD_SNVS_IN supply voltage	VDD_SNVS_IN	-0.3	3.3	V
VDDHIGH_IN supply voltage	VDDHIGH_IN	-0.3	3.6	V
USB VBUS	VBUS	—	5.25	V
Input voltage on USB_OTG_DP, USB_OTG_DN, USB_H1_DP, USB_H1_DN pins	USB_DP/USB_DN	-0.3	3.63	V
Input/output voltage range	V _{in} /V _{out}	-0.5	OVDD ¹ +0.3	V

4.1.3 Operating Ranges

Table 9 provides the operating ranges of the i.MX 6Solo/6DualLite processors. For details on the chip's power structure, see the “Power Management Unit (PMU)” chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

Table 9. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max ¹	Unit	Comment
Run mode: LDO enabled	VDDARM_IN	1.275 ²	—	1.5	V	LDO Output Set Point (VDDARM_CAP) = 1.150 V minimum for operation up to 792 MHz.
		1.175 ²	—	1.5	V	LDO Output Set Point (VDDARM_CAP) = 1.05 V minimum for operation up to 396 MHz.
	VDDSOC_IN ³	1.275 ^{2,4}	—	1.5	V	VPU <= 328 MHz, VDDSOC and VDDPU LDO outputs (VDDSOC_CAP and VDDPU_CAP) = 1.225 V maximum and 1.15 V minimum.
Run mode: LDO bypassed	VDDARM_IN	1.150	—	1.3	V	LDO bypassed for operation up to 792 MHz
		1.05	—	1.3	V	LDO bypassed for operation up to 396 MHz
	VDDSOC_IN ³	1.15 ⁴	—	1.225	V	LDO bypassed for operation VPU <= 328 MHz
Standby/DSM mode	VDDARM_IN	0.9	—	1.3	V	Refer to Table 13, “Stop Mode Current and Power Consumption,” on page 29.
	VDDSOC_IN	0.9	—	1.225	V	
VDDHIGH internal regulator	VDDHIGH_IN	2.8	—	3.3	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN ⁵	2.9	—	3.3	V	Should be supplied from the same supply as VDDHIGH_IN if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG_VBUS	4.4	—	5.25	V	
	USB_H1_VBUS	4.4	—	5.25	V	
DDR I/O supply voltage	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2, DDR3-U
		1.425	1.5	1.575	V	DDR3
		1.283	1.35	1.45	V	DDR3_L
Supply for RGMII I/O power group ⁶	NVCC_RGMII	1.15	—	2.625	V	1.15 V – 1.30 V in HSIC 1.2 V mode 1.43 V – 1.58 V in RMGII 1.5 V mode 1.70 V – 1.90 V in RMGII 1.8 V mode 2.25 V – 2.625 V in RMGII 2.5 V mode

- VDDARM_IN supply must be turned ON together with VDDSOC_IN supply or not delayed more than 1 ms
- VDDARM_CAP must not exceed VDDSOC_CAP by more than 50 mV.

NOTE

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the *i.MX 6Solo/6DualLite Reference Manual* for further details and to ensure that all necessary requirements are being met.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG_VBUS and USB_H1_VBUS are not part of the power supply sequence and may be powered at any time.

4.2.2 Power-Down Sequence

No special restrictions for i.MX 6Solo/6DualLite IC.

4.2.3 Power Supplies Usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_XXX) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Rail” columns in pin list tables of [Section 6, “Package Information and Contact Assignments.”](#)

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for details on the power tree scheme.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of

enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω .

For additional information, see the i.MX 6Solo/6DualLite reference manual.

4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB_OTG_VBUS and USB_H1_VBUS voltages (4.4 V–5.25 V) to produce a nominal 3.0 V output voltage. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 μ F (2.2 μ F should be considered the recommended minimum value for component selection), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either VBUS supply, when both are present. If only one of the VBUS voltages is present, then, the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets.

For additional information, see the i.MX 6Solo/6DualLite reference manual.

4.4 PLL's Electrical Characteristics

4.4.1 Audio/Video PLL's Electrical Parameters

Table 17. Audio/Video PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.2 528 MHz PLL

Table 18. 528 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles

Table 23. OSC32K Main Characteristics

	Min	Typ	Max	Comments
Bias resistor		14 M Ω		This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Crystal Properties				
Cload		10 pF		Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR		50 k Ω	100 k Ω	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes
- LVDS I/O
- MLB I/O

NOTE

The term 'OVDD' in this section refers to the associated supply rail of an input or output.

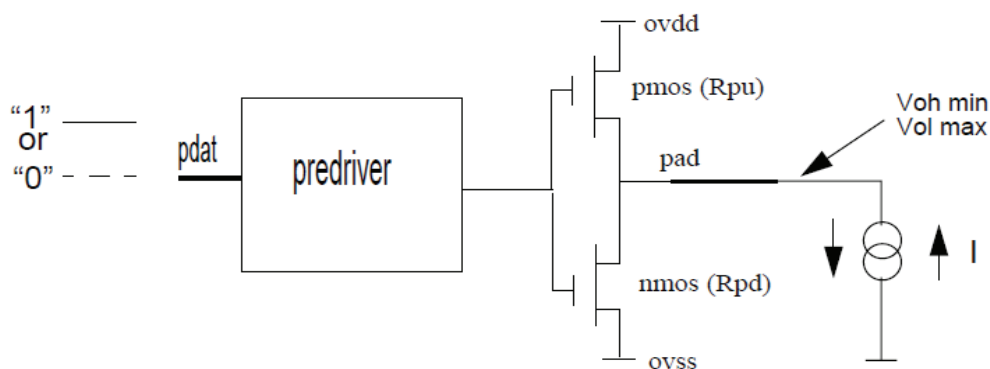


Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

Table 33 shows the AC parameters for LVDS I/O.

Table 33. I/O AC Parameters of LVDS Pad

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential pulse skew ¹	t_{SKD}	$R_{load} = 100\ \Omega$ $C_{load} = 2\ pF$	—	—	0.25	ns
Transition Low to High Time ²	t_{TLH}		—	—	0.5	
Transition High to Low Time ²	t_{THL}		—	—	0.5	
Operating Frequency	f	—	—	600	800	MHz
Offset voltage imbalance	Vos	—	—	—	150	mV

¹ $t_{SKD} = |t_{PHLD} - t_{PLHD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

² Measurement levels are 20-80% from output voltage.

4.7.4 MLB I/O AC Parameters

The differential output transition time waveform is shown in Figure 7.

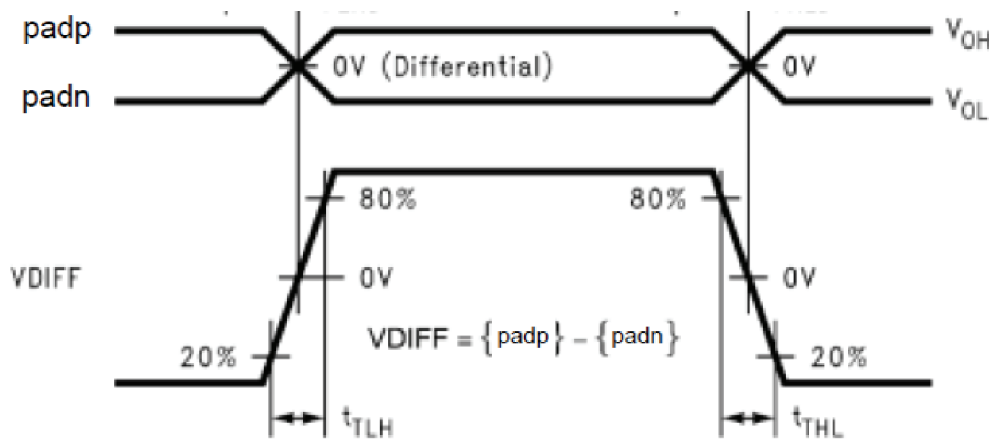


Figure 7. Differential MLB Driver Transition Time Waveform

A 4-stage pipeline is utilized in the MLB 6-pin implementation in order to facilitate design, maximize throughput, and allow for reasonable PCB trace lengths. Each cycle is one $ipp_clk_in^*$ (internal clock from MLB PLL) clock period. Cycles 2, 3, and 4 are MLB PHY related. Cycle 2 includes clock-to-output delay of Signal/Data sampling flip-flop and Transmitter, Cycle 3 includes clock-to-output delay of Signal/Data clocked receiver, Cycle 4 includes clock-to-output delay of Signal/Data sampling flip-flop.

MLB 6-pin pipeline diagram is shown in Figure 8.

4.9.4 DDR SDRAM Specific Parameters (DDR3/DDR3L and LPDDR2)

4.9.4.1 DDR3/DDR3L Parameters

Figure 24 shows the basic timing parameters. The timing parameters for this diagram appear in Table 45.

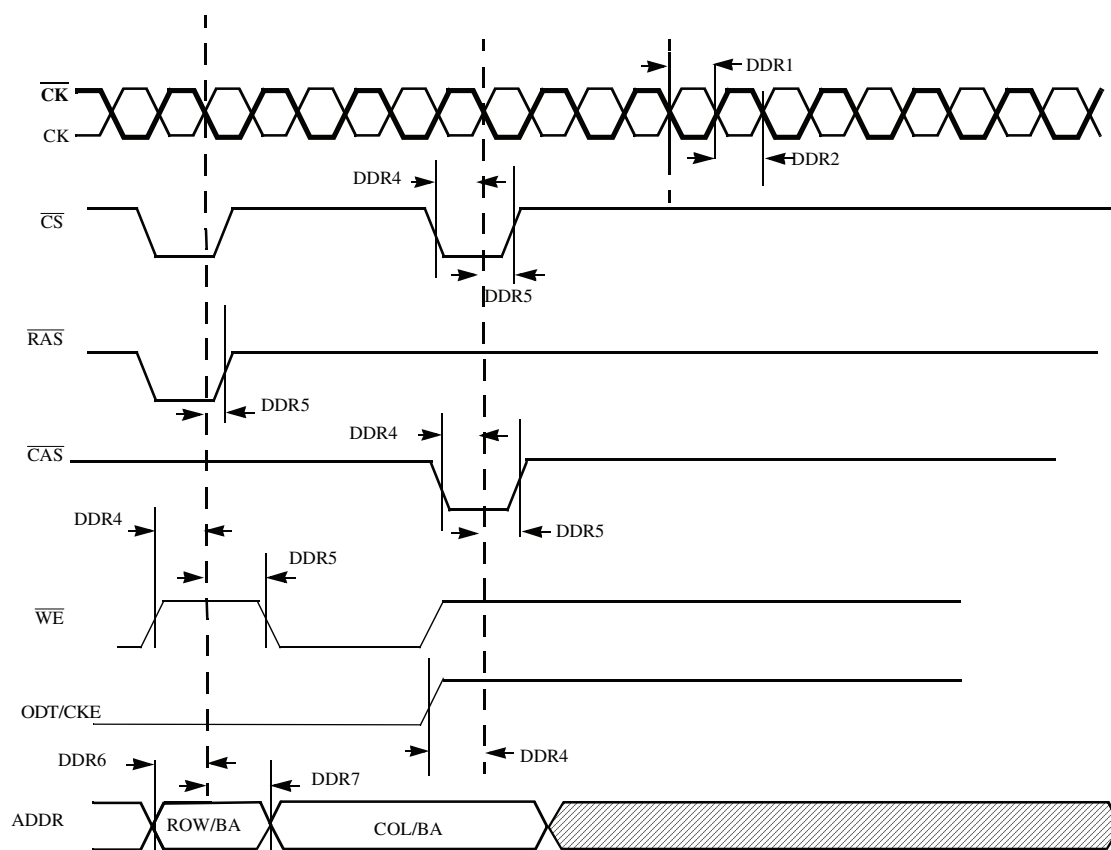


Figure 24. DDR3 Command and Address Timing Parameters

Table 45. DDR3/DDR3L Timing Parameter Table

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR1	CK clock high-level width	t _{CH}	0.47	0.53	t _{CK}
DDR2	CK clock low-level width	t _{CL}	0.47	0.53	t _{CK}
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	t _{IS}	800	—	ps
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	t _{IH}	580	—	ps
DDR6	Address output setup time	t _{IS}	800	—	ps
DDR7	Address output hold time	t _{IH}	580	—	ps

Table 59. SDR50/SDR104 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs CMD, DAT in SDR104 (Reference to CLK) ¹					
SD8	Card Output Data Window	t_{ODW}	$0.5 \cdot t_{CLK}$	—	ns

¹Data window in SDR100 mode is variable.

4.11.4.4 Bus Operation Condition for 3.3 V and 1.8 V Signaling

Signaling level of SD/eMMC4.3 and eMMC4.4 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1, NVCC_SD2 and NVCC_SD3 supplies are identical to those shown in [Table 24, "GPIO DC Parameters,"](#) on page 38.

4.11.5 Ethernet Controller (ENET) AC Electrical Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

4.11.5.1 ENET MII Mode Timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

4.11.5.1.1 MII Receive Signal Timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

Electrical Characteristics

Power-up time for the HDMI 3D Tx PHY while operating with the fastest input reference clock supported (340 MHz) is 133 μ s.

4.11.7.2 Electrical Characteristics

The table below provides electrical characteristics for the HDMI 3D Tx PHY. The following three figures illustrate various definitions and measurement conditions specified in the table below.

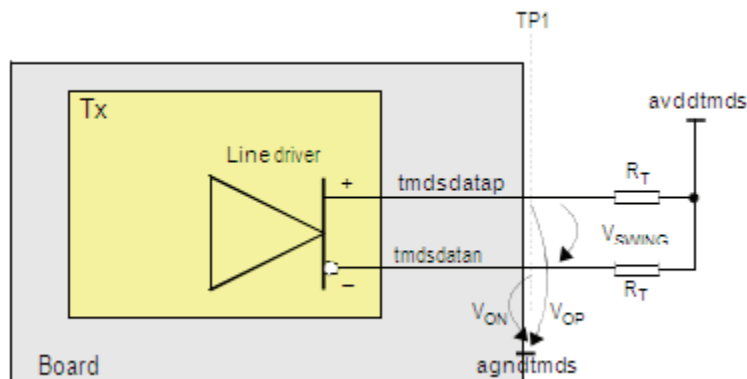


Figure 55. Driver Measuring Conditions

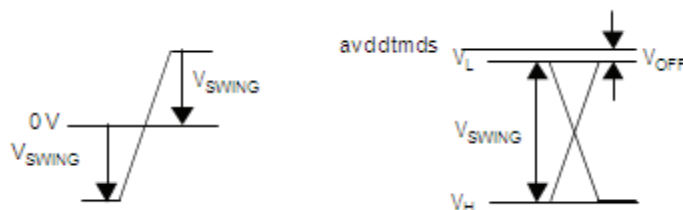


Figure 56. Driver Definitions

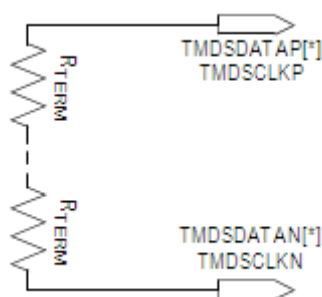


Figure 57. Source Termination

Table 75. Electrical and Timing Information (continued)

V_{LEAK}	Input leakage current	$V_{GNDSH(min)} = V_I = V_{GNDSH(max)} + V_{OH(absmax)}$ Lane module in LP Receive Mode	-10	—	10	mA
V_{GNDSH}	Ground Shift		-50	—	50	mV
$V_{OH(absmax)}$	Maximum transient output voltage level		—	—	1.45	V
$t_{voh(absmax)}$	Maximum transient time above $V_{OH(absmax)}$		—	—	20	ns
HS Line Drivers DC Specifications						
$ V_{OD} $	HS Transmit Differential output voltage magnitude	$80\ \Omega \leq R_L < 125\ \Omega$	140	200	270	mV
$\Delta V_{OD} $	Change in Differential output voltage magnitude between logic states	$80\ \Omega \leq R_L < 125\ \Omega$			10	mV
V_{CMTX}	Steady-state common-mode output voltage.	$80\ \Omega \leq R_L < 125\ \Omega$	150	200	250	mV
$\Delta V_{CMTX(1,0)}$	Changes in steady-state common-mode output voltage between logic states	$80\ \Omega \leq R_L < 125\ \Omega$			5	mV
V_{OHHS}	HS output high voltage	$80\ \Omega \leq R_L < 125\ \Omega$			360	mV
Z_{OS}	Single-ended output impedance.		40	50	62.5	Ω
ΔZ_{OS}	Single-ended output impedance mismatch.				10	%
LP Line Drivers DC Specifications						
V_{OL}	Output low-level SE voltage		-50		50	mV
V_{OH}	Output high-level SE voltage		1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance.		110			Ω
$\Delta Z_{OLP(01-10)}$	Single-ended output impedance mismatch driving opposite level				20	%
$\Delta Z_{OLP(0-11)}$	Single-ended output impedance mismatch driving same level				5	%
HS Line Receiver DC Specifications						
V_{IDTH}	Differential input high voltage threshold				70	mV

4.11.12.2 MIPI D-PHY Signaling Levels

The signal levels are different for differential HS mode and single-ended LP mode. Figure 71 shows both the HS and LP signal levels on the left and right sides, respectively. The HS signaling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

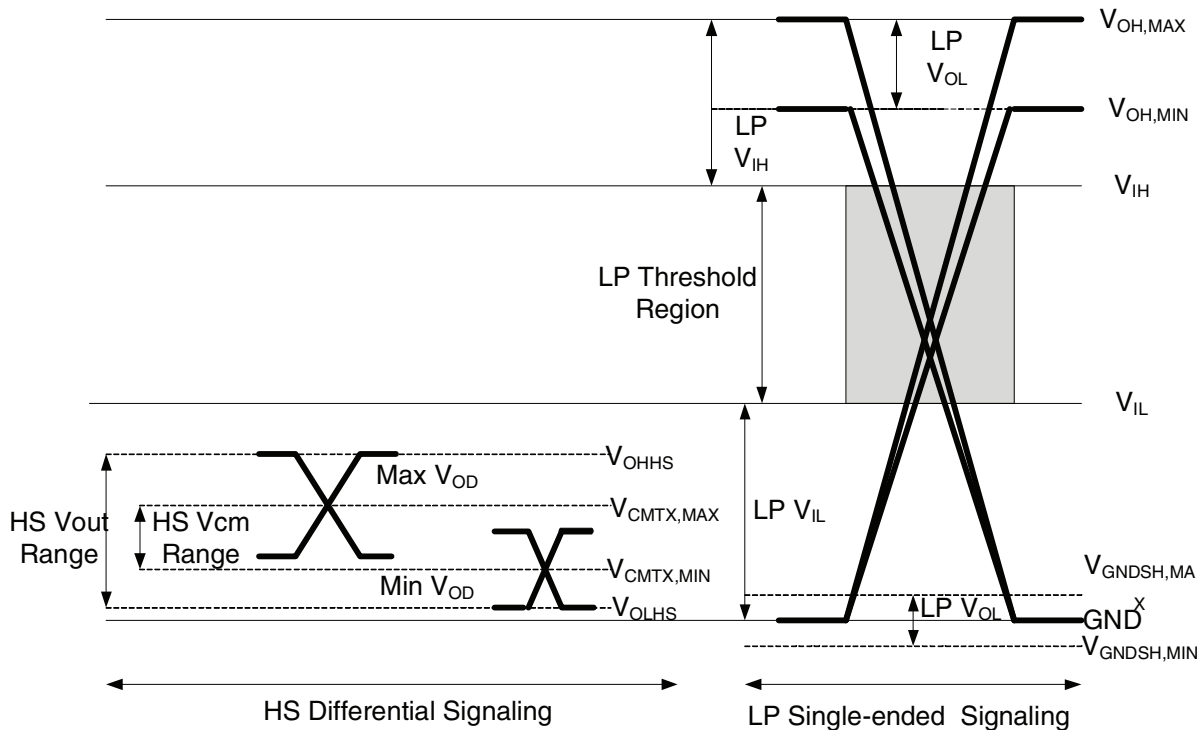


Figure 71. D-PHY Signaling Levels

4.11.12.3 MIPI HS Line Driver Characteristics

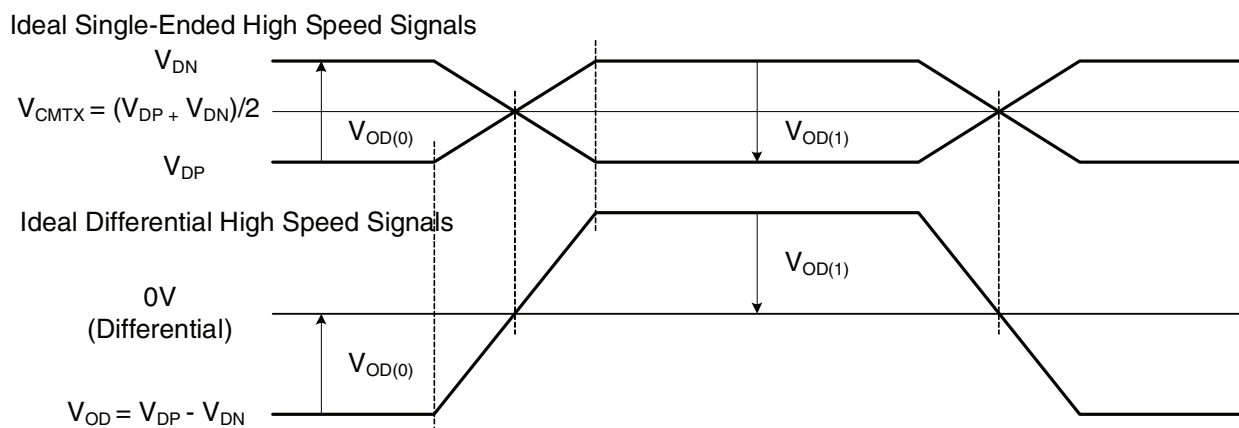


Figure 72. Ideal Single-ended and Resulting Differential HS Signals

4.11.13.7 Frame Transmission Mode (Pipelined Data Flow)

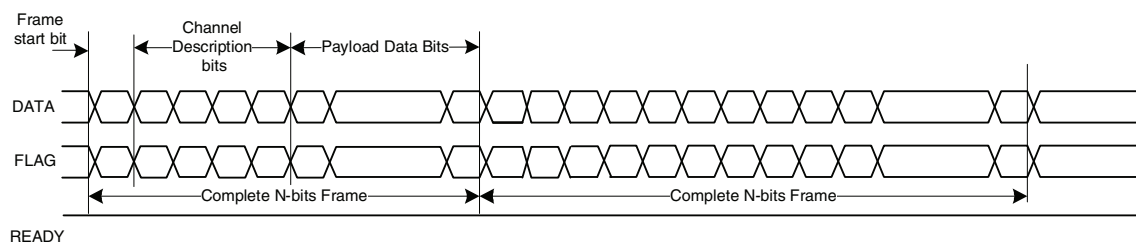


Figure 84. Frame Transmission Mode Transfer of Two Frames (Pipelined Data Flow)

4.11.13.8 DATA and FLAG Signal Timing Requirement for a 15 pF Load

Table 77. DATA and FLAG Timing

Parameter	Description	1 Mbit/s	100 Mbit/s	200 Mbit/s
$t_{\text{Bit, nom}}$	Nominal bit time	1000 ns	10.0 ns	5.00 ns
$t_{\text{Rise, min}}$ and $t_{\text{Fall, min}}$	Minimum allowed rise and fall time	2.00 ns	2.00 ns	1.00 ns
$t_{\text{TxToRxSkew, maxfq}}$	Maximum skew between transmitter and receiver package pins	50.0 ns	0.5.0 ns	0.25 ns
$t_{\text{EageSepTx, min}}$	Minimum allowed separation of signal transitions at transmitter package pins, including all timing defects, for example, jitter and skew, inside the transmitter.	400 ns	4.00 ns	2.00 ns
$t_{\text{EageSepRx, min}}$	Minimum separation of signal transitions, measured at the receiver package pins, including all timing defects, for example, jitter and skew, inside the receiver.	350 ns	3.5 ns	1.75 ns

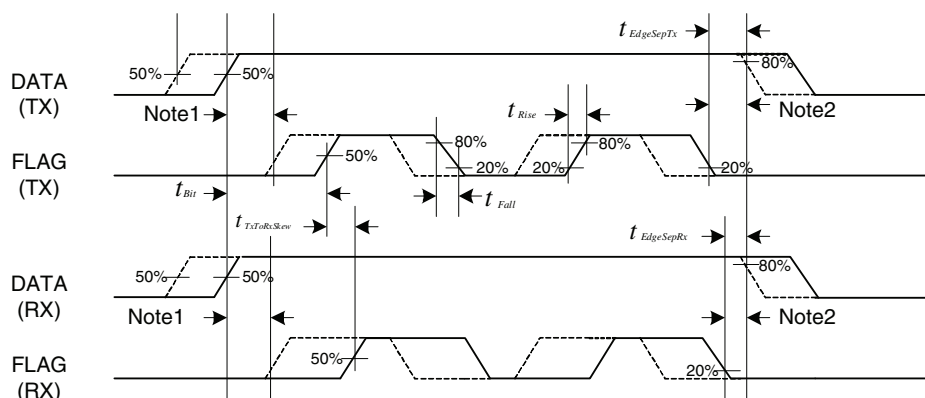


Figure 85. DATA and FLAG Signal Timing

Note:

- ¹ This case shows that the DATA signal has slowed down more compared to the FLAG signal
- ² This case shows that the FLAG signal has slowed down more compared to the DATA signal.

4.11.19.1 SSI Transmitter Timing with Internal Clock

Figure 95 depicts the SSI transmitter internal clock timing and Table 87 lists the timing parameters for the SSI transmitter internal clock.

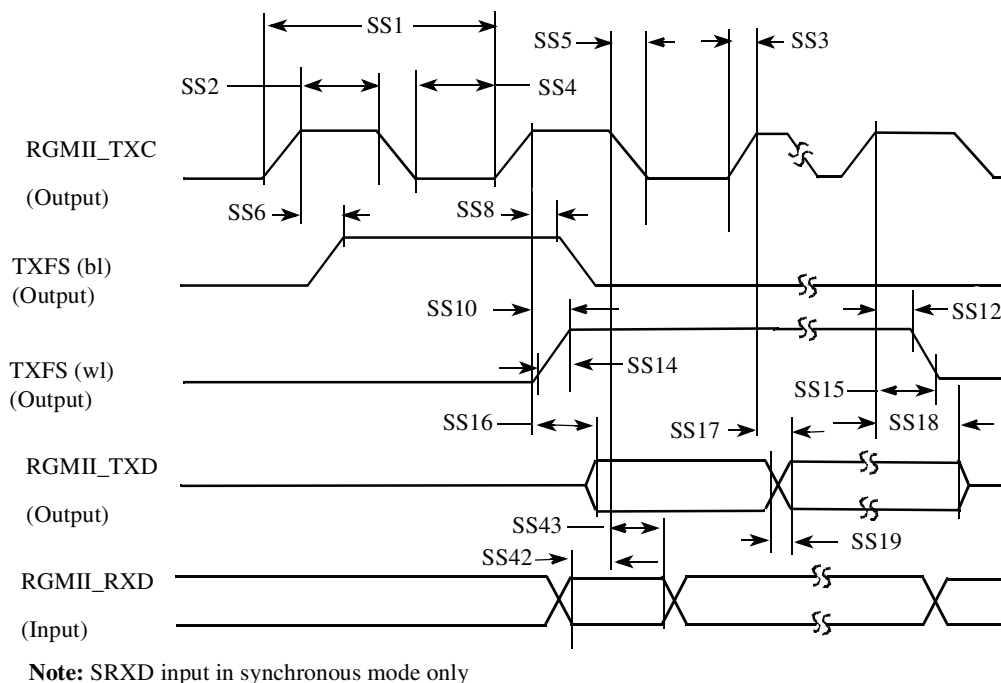


Figure 95. SSI Transmitter Internal Clock Timing Diagram

Table 87. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6.0	ns
SS15	(Tx/Rx) Internal FS fall time	—	6.0	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns

Table 87. SSI Transmitter Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

Table 88. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

Table 89. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFISI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

Table 101. 21 x 21 mm Functional Contact Assignments¹ (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ²			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DRAM_DQM0	AC3	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[0]	Output	Low
DRAM_DQM1	AC6	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[1]	Output	Low
DRAM_DQM2	AB8	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[2]	Output	Low
DRAM_DQM3	AE10	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[3]	Output	Low
DRAM_DQM4	AB18	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[4]	Output	Low
DRAM_DQM5	AC20	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[5]	Output	Low
DRAM_DQM6	AD24	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[6]	Output	Low
DRAM_DQM7	Y21	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[7]	Output	Low
DRAM_RAS	AB15	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_RAS	Output	Low
DRAM_RESET	Y6	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_RESET	Output	Low
DRAM_SDBA0	AC15	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_SDBA[0]	Output	Low
DRAM_SDBA1	Y15	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_SDBA[1]	Output	Low
DRAM_SDBA2	AB12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_SDBA[2]	Output	Low
DRAM_SDCKE0	Y11	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_SDCKE[0]	Output	Low
DRAM_SDCKE1	AA11	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_SDCKE[1]	Output	Low
DRAM_SDCLK_0	AD15	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDCLK0	Output	Low
DRAM_SDCLK_0_B	AE15	NVCC_DRAM			DRAM_SDCLK_0_B	-	-
DRAM_SDCLK_1	AD14	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDCLK1	Output	Low
DRAM_SDCLK_1_B	AE14	NVCC_DRAM			DRAM_SDCLK_1_B	-	-
DRAM_SDOT0	AC16	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_ODT[0]	Output	Low
DRAM_SDOT1	AB17	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_ODT[1]	Output	Low
DRAM_SDQS0	AE3	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[0]	Input	Hi-Z
DRAM_SDQS0_B	AD3	NVCC_DRAM			DRAM_SDQS0_B	-	-
DRAM_SDQS1	AD6	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[1]	Input	Hi-Z
DRAM_SDQS1_B	AE6	NVCC_DRAM			DRAM_SDQS1_B	-	-
DRAM_SDQS2	AD8	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[2]	Input	Hi-Z
DRAM_SDQS2_B	AE8	NVCC_DRAM			DRAM_SDQS2_B	-	-
DRAM_SDQS3	AC10	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[3]	Input	Hi-Z
DRAM_SDQS3_B	AB10	NVCC_DRAM			DRAM_SDQS3_B	-	-
DRAM_SDQS4	AD18	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[4]	Input	Hi-Z

Table 101. 21 x 21 mm Functional Contact Assignments¹ (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ²			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
LVDS0_TX1_N	U4	NVCC_LVDS2P5					
LVDS0_TX1_P	U3	NVCC_LVDS2P5		ALT0	ldb.LVDS0_TX1	Input	Keeper
LVDS0_TX2_N	V2	NVCC_LVDS2P5					
LVDS0_TX2_P	V1	NVCC_LVDS2P5		ALT0	ldb.LVDS0_TX2	Input	Keeper
LVDS0_TX3_N	W2	NVCC_LVDS2P5					
LVDS0_TX3_P	W1	NVCC_LVDS2P5		ALT0	ldb.LVDS0_TX3	Input	Keeper
LVDS1_CLK_N	Y3	NVCC_LVDS2P5					
LVDS1_CLK_P	Y4	NVCC_LVDS2P5		ALT0	ldb.LVDS1_CLK	Input	Keeper
LVDS1_TX0_N	Y1	NVCC_LVDS2P5					
LVDS1_TX0_P	Y2	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX0	Input	Keeper
LVDS1_TX1_N	AA2	NVCC_LVDS2P5					
LVDS1_TX1_P	AA1	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX1	Input	Keeper
LVDS1_TX2_N	AB1	NVCC_LVDS2P5					
LVDS1_TX2_P	AB2	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX2	Input	Keeper
LVDS1_TX3_N	AA3	NVCC_LVDS2P5					
LVDS1_TX3_P	AA4	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX3	Input	Keeper
MLB_CN	A11	VDDHIGH_CAP					
MLB_CP	B11	VDDHIGH_CAP					
MLB_DN	B10	VDDHIGH_CAP					
MLB_DP	A10	VDDHIGH_CAP					
MLB_SN	A9	VDDHIGH_CAP					
MLB_SP	B9	VDDHIGH_CAP					
NANDF_ALE	A16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[8]	Input	100 kΩ pull-up
NANDF_CLE	C15	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[7]	Input	100 kΩ pull-up
NANDF_CS0	F15	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[11]	Input	100 kΩ pull-up
NANDF_CS1	C16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[14]	Input	100 kΩ pull-up
NANDF_CS2	A17	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[15]	Input	100 kΩ pull-up
NANDF_CS3	D16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[16]	Input	100 kΩ pull-up
NANDF_D0	A18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[0]	Input	100 kΩ pull-up
NANDF_D1	C17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[1]	Input	100 kΩ pull-up