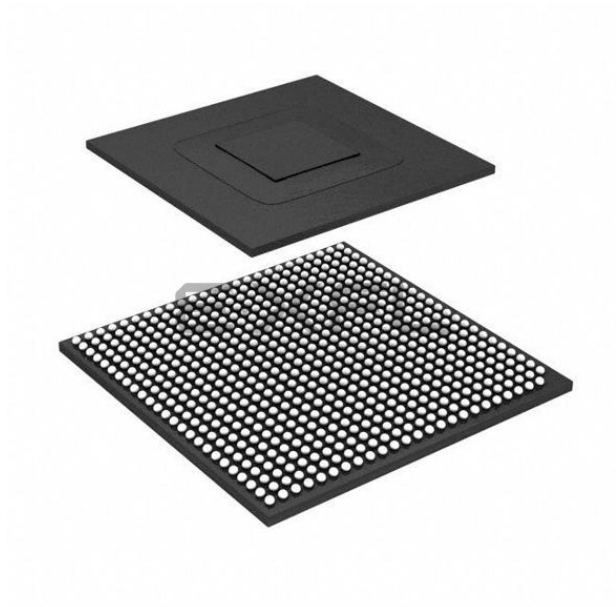

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6u4avm08abr

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
IPUv3H	Image Processing Unit, ver.3H	Multimedia Peripherals	IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation. The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces: • Parallel Interfaces for both display and camera • Single/dual channel LVDS display interface • HDMI transmitter • MIPI/DSI transmitter • MIPI/CSI-2 receiver The processing includes: • Image conversions: resizing, rotation, inversion, and color space conversion • A high-quality de-interlacing filter • Video/graphics combining • Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement • Support for display backlight reduction
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8x8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: • One clock pair • Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MLB150	MediaLB	Connectivity / Multimedia Peripherals	The MLB interface module provides a link to a MOST® data network, using the standardized MediaLB protocol (up to 6144 fs). The module is backward compatible to MLB-50.
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Supports 16/32-bit DDR3-800 (LV) or LPDDR2-800 in i.MX 6Solo • Supports 16/32/64-bit DDR3-800 (LV) or LPDDR2-800 in i.MX 6DualLite • Supports 2x32 LPDDR2-800 in i.MX 6DualLite • Supports up to 4 GByte DDR memory space

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6Solo/6DualLite processors.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 6Solo/6DualLite Chip-Level Conditions

For these characteristics, …	Topic appears …
Absolute Maximum Ratings	on page 22
BGA Case 2240 Package Thermal Resistance	on page 23
Operating Ranges	on page 24
External Clock Sources	on page 26
Maximal Supply Currents	on page 27
Low Power Mode Supply Currents	on page 29
USB PHY Current Consumption	on page 30
PCIe 2.0 Power Consumption	on page 30

4.1.1 Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core supply voltages	VDDARM_IN VDDSOC_IN	-0.3	1.5	V
Internal supply voltages	VDDARM_CAP VDDSOC_CAP VDDPU_CAP	-0.3	1.3	V
GPIO supply voltage	Supplies denoted as I/O supply	-0.5	3.6	V
DDR I/O supply voltage	Supplies denoted as I/O supply	-0.4	1.975	V
MLB I/O supply voltage	Supplies denoted as I/O supply	-0.3	2.8	V
LVDS I/O supply voltage	Supplies denoted as I/O supply	-0.3	2.8	V
VDD_SNVS_IN supply voltage	VDD_SNVS_IN	-0.3	3.3	V
VDDHIGH_IN supply voltage	VDDHIGH_IN	-0.3	3.6	V
USB VBUS	VBUS	—	5.25	V
Input voltage on USB_OTG_DP, USB_OTG_DN, USB_H1_DP, USB_H1_DN pins	USB_DP/USB_DN	-0.3	3.63	V
Input/output voltage range	V_{in}/V_{out}	-0.5	OVDD[1]+0.3	V

Table 7. Absolute Maximum Ratings (continued)

Parameter Description	Symbol	Min	Max	Unit
ESD damage immunity: • Human Body Model (HBM) • Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	V
Storage temperature range	$T_{STORAGE}$	-40	150	°C

1 OVDD is the I/O supply voltage.

4.1.2 Thermal Resistance

4.1.2.1 BGA Case 2240 Package Thermal Resistance

Table 8 displays the thermal resistance data.

Table 8. Thermal Resistance Data

Rating	Test Conditions	Symbol	Value	Unit
Junction to Ambient[1]	Single-layer board (1s); natural convection[2] Four-layer board (2s2p); natural convection[2]	$R_{\theta JA}$ $R_{\theta JA}$	38 23	°C/W °C/W
Junction to Ambient[1]	Single-layer board (1s); airflow 200 ft/min[2,3] Four-layer board (2s2p); airflow 200 ft/min[2,3]	$R_{\theta JA}$ $R_{\theta JA}$	30 20	°C/W °C/W
Junction to Board[1,4]		$R_{\theta JB}$	14	°C/W
Junction to Case[1,5]		$R_{\theta JC}$	6	°C/W
Junction to Package Top[1,6]	Natural Convection	Ψ_{JT}	2	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-2 with the single layer board horizontal. Thermal test board meets JEDEC specification for the specified package.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1.9 HDMI Power Consumption

Table 16 provides HDMI PHY currents for both Active 3D Tx with LFSR15 data and power-down modes.

Table 16. HDMI PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
Active	Bit rate 251.75 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.1	mA
	Bit rate 279.27 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.2	mA
	Bit rate 742.5 Mbps	HDMI_VPH	17	mA
		HDMI_VP	7.5	mA
	Bit rate 1.485 Gbps	HDMI_VPH	17	mA
		HDMI_VP	12	mA
	Bit rate 2.275 Gbps	HDMI_VPH	16	mA
		HDMI_VP	17	mA
	Bit rate 2.97 Gbps	HDMI_VPH	19	mA
		HDMI_VP	22	mA
Power-down		HDMI_VPH	49	µA
		HDMI_VP	1100	µA

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.2.1 Power-Up Sequence

The below restrictions must be followed:

- VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDDHIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- If VDDARM_IN and VDDSOC_IN are connected to different external supply sources, then the following restrictions apply:

4.4.3 Ethernet PLL

Table 19. Ethernet PLL's Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.4 480 MHz PLL

Table 20. 480 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles

4.4.5 MLB PLL

The MediaLB PLL is necessary in the MediaLB 6-Pin implementation to phase align the internal and external clock edges, effectively tuning out the delay of the differential clock receiver and is also responsible for generating the higher speed internal clock, when the internal-to-external clock ratio is not 1:1.

Table 21. MLB PLL's Electrical Parameters

Parameter	Value
Lock time	<1 ms

4.4.6 ARM PLL

Table 22. ARM PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~ 1.3 GHz
Reference clock	24 MHz
Lock time	<2250 reference cycles

4.6.2.2 DDR3/DDR3L Mode I/O DC Parameters

The DDR3/DDR3L interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008. The parameters in Table 26 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 26. DDR3/DDR3L I/O DC Electrical Characteristics

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -0.1mA Voh (for ipp_dse=001)	0.8*OVDD[1]		V
Low-level output voltage	VOL	Iol= 0.1mA Vol (for ipp_dse=001)	0.2*OVDD	V	
High-level output voltage	VOH	Ioh= -1mA Voh (for all except ipp_dse=001)	0.8*OVDD		V
Low-level output voltage	VOL	Iol= 1mA Vol (for all except ipp_dse=001)	0.2*OVDD	V	
Input Reference Voltage	Vref		0.49*ovdd	0.51*ovdd	V
DC High-Level input voltage	Vih_DC		Vref[2]+0.1	OVDD	V
DC Low-Level input voltage	Vil_DC		OVSS	Vref-0.1	V
DifferentialInput Logic High	Vih_diff		0.2	See Note[3]	V
DifferentialInput Logic Low	Vil_diff		See Note[3]	-0.2	V
Termination Voltage	Vtt	Vtt tracking OVDD/2	0.49*OVDD	0.51*OVDD	V
Pull-up/Pull-down Impedance Mismatch	Mmpupd		-10	10	%
240 Ω unit calibration resolution	Rres			10	Ω
Keeper Circuit Resistance	Rkeep		105	165	kΩ
Input current (no pull-up/down)	Iin	VI = 0,VI = OVDD	-2.9	2.9	μA

1 OVDD – I/O power supply (1.425 V–1.575 V for DDR3 and 1.283 V–1.45 V for DDR3L)

2 Vref – DDR3/DDR3L external reference voltage

3 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4.6.3 LVDS I/O DC Parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

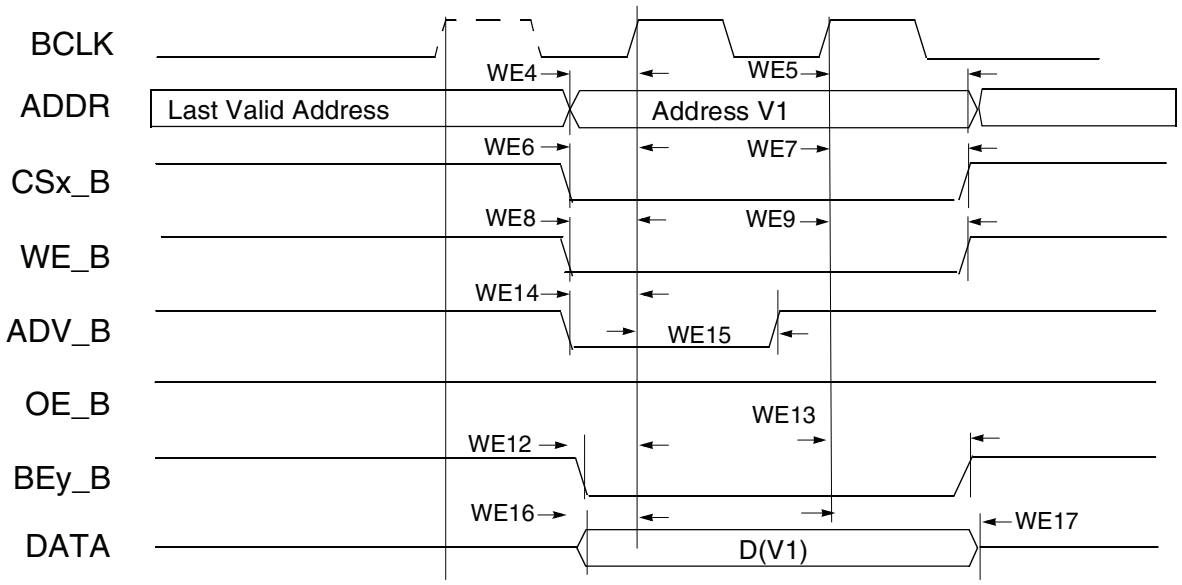

Figure 15. Synchronous Memory, Write Access, WSC=1, WBEA=0 and WADVN=0

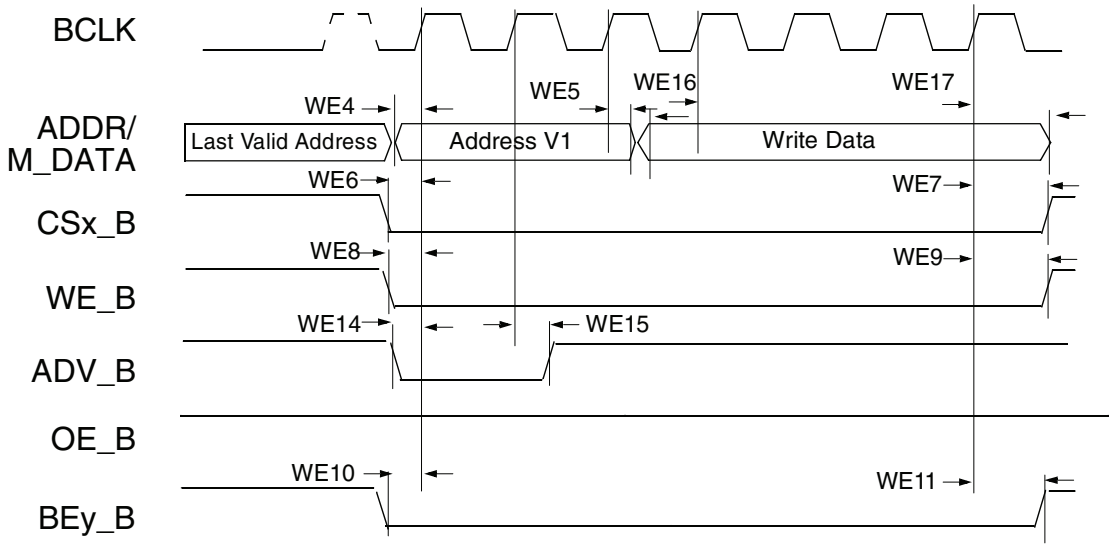

Figure 16. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6,ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

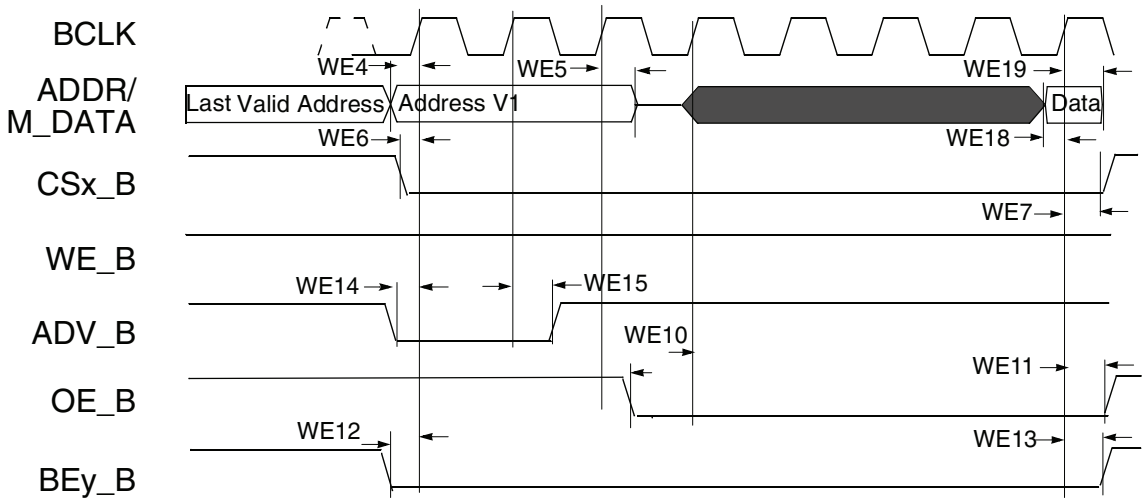

Figure 17. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.5 General EIM Timing-Asynchronous Mode

Figure 18 through Figure 22, and Table 44 help you determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 18 through Figure 21 as RWSC, OEN & CSN is configured differently. See the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for the EIM programming model.

Table 44. EIM Asynchronous Timing Parameters Table Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max (If 132 MHz is supported by SoC)	Unit
WE31	CSx_B valid to Address Valid	WE4 - WE6 - CSA[2]	—	3 - CSA	ns
WE32	Address Invalid to CSx_B invalid	WE7 - WE5 - CSN[3]	—	3 - CSN	ns
WE32A(muxed A/D	CSx_B valid to Address Invalid	t[4] + WE4 - WE7 + (ADVN[5] + ADVA[6] + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	—	ns
WE33	CSx_B Valid to WE_B Valid	WE8 - WE6 + (WEA - WCSA)	—	3 + (WEA - WCSA)	ns
WE34	WE_B Invalid to CSx_B Invalid	WE7 - WE9 + (WEN - WCSN)	—	3 - (WEN_WCSN)	ns
WE35	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA - RCSA)	—	3 + (OEA - RCSA)	ns
WE35A (muxed A/D)	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - RCSA)	-3 + (OEA + RADVN+RADVA+ ADH+1-RCSA)	3 + (OEA + RADVN+RADVA+AD H+1-RCSA)	ns
WE36	OE_B Invalid to CSx_B Invalid	WE7 - WE11 + (OEN - RCSN)	—	3 - (OEN - RCSN)	ns
WE37	CSx_B Valid to BEy_B Valid (Read access)	WE12 - WE6 + (RBEA - RCSA)	—	3 + (RBEA - RCSA)	ns
WE38	BEy_B Invalid to CSx_B Invalid (Read access)	WE7 - WE13 + (RBEN - RCSN)	—	3 - (RBEN- RCSN)	ns
WE39	CSx_B Valid to ADV_B Valid	WE14 - WE6 + (ADVA - CSA)	—	3 + (ADVA - CSA)	ns
WE40	ADV_B Invalid to CSx_B Invalid (ADVL is asserted)	WE7 - WE15 - CSN	—	3 - CSN	ns
WE40A (muxed A/D)	CSx_B Valid to ADV_B Invalid	WE14 - WE6 + (ADVN + ADVA + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	3 + (ADVN + ADVA + 1 - CSA)	ns
WE41	CSx_B Valid to Output Data Valid	WE16 - WE6 - WCSA	—	3 - WCSA	ns
WE41A (muxed A/D)	CSx_B Valid to Output Data Valid	WE16 - WE6 + (WADVN + WADVA + ADH + 1 - WCSA)	—	3 + (WADVN + WADVA + ADH + 1 - WCSA)	ns
WE42	Output Data Invalid to CSx_B Invalid	WE17 - WE7 - CSN	—	3 - CSN	ns
MAXCO	Output max. delay from internal driving ADDR/control FFs to chip outputs.	10	—	—	ns
MAXCS O	Output max. delay from CSx internal driving FFs to CSx out.	10	—	—	
MAXDI	DATA MAXIMUM delay from chip input data to its internal FF	5	—	—	

1 All measurements are in reference to Vref level.

2 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 25shows the DDR3/DDR3L write timing parameters. The timing parameters for this diagram appear in Table 46.

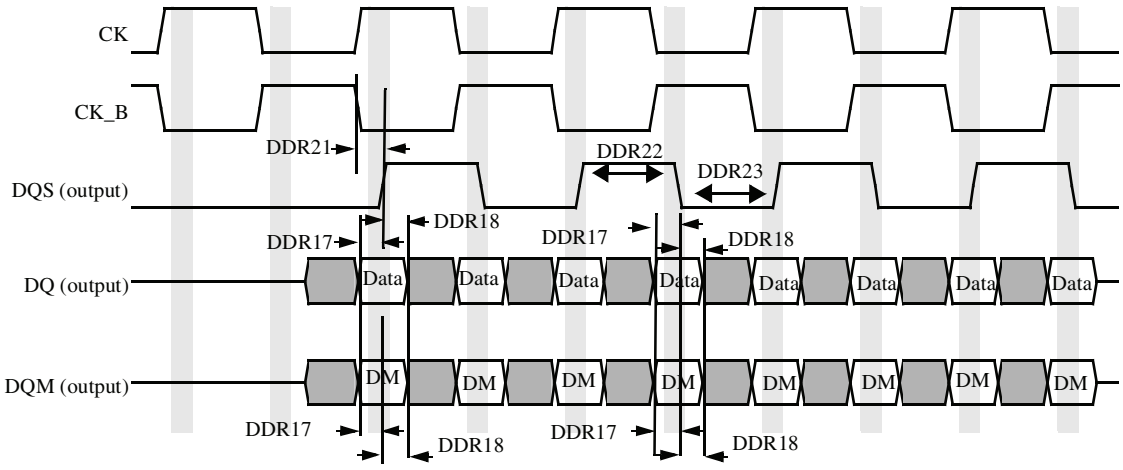

Figure 25. DDR3/DDR3L Write Cycle

Table 46. DDR3/DDR3L Write Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (differential strobe)	t_{DS}	420	—	ps
DDR18	DQ and DQM hold time to DQS (differential strobe)	t_{DH}	345	—	ps
DDR21	DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.25	+0.25	tCK
DDR22	DQS high level width	t_{DQSH}	0.45	0.55	tCK
DDR23	DQS low level width	t_{DQSL}	0.45	0.55	tCK

1 To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

2 All measurements are in reference to Vref level.

3 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

4.11.2.2 ECSPI Slave Mode Timing

Figure 41 depicts the timing of ECSPI in slave mode. Table 55 lists the ECSPI slave mode timing characteristics.

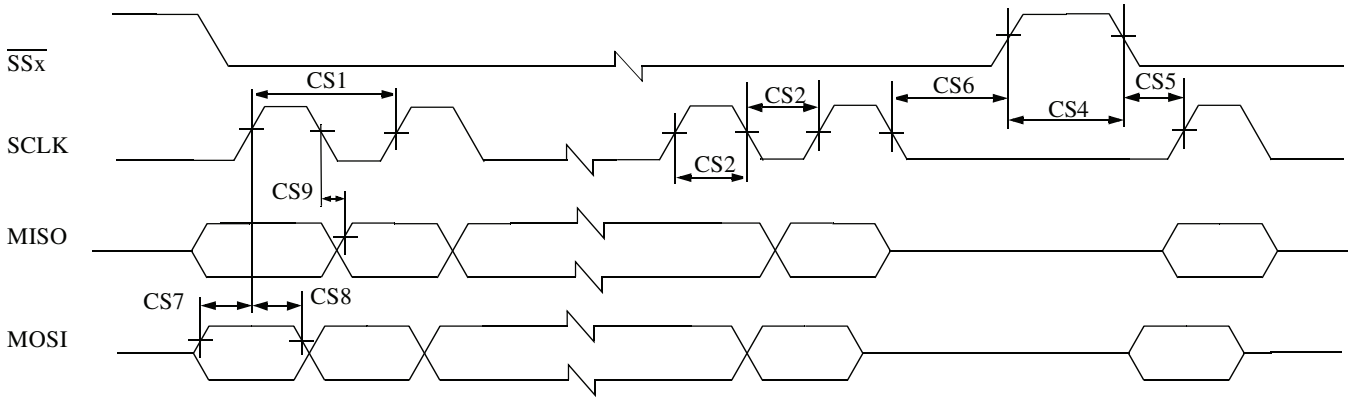

Figure 41. ECSPI Slave Mode Timing Diagram

Table 55. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time–Read SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	SCLK High or Low Time–Read SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	19	ns

Table 56. Enhanced Serial Audio Interface (ESAI) Timing (continued)

No.	Characteristics[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
81	SCKT rising edge to FST out (wr) low[5]	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	SCKT rising edge to data out valid	— —	— —	— —	18.0 13.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance [67]	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge[5]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns
95	HCKR/HCKT clock cycle	—	2 x T_C	15	—	—	ns
96	HCKT input rising edge to SCKT output	—	—	—	18.0	—	ns
97	HCKR input rising edge to SCKR output	—	—	—	18.0	—	ns

1 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that SCKT and SCKR are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that SCKT and SCKR are the same clock)

2 bl = bit length
wl = word length
wr = word length relative

3 SCKT(SCKT pin) = transmit clock
SCKR(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

4 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

5 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

6 Periodically sampled and not 100% tested.

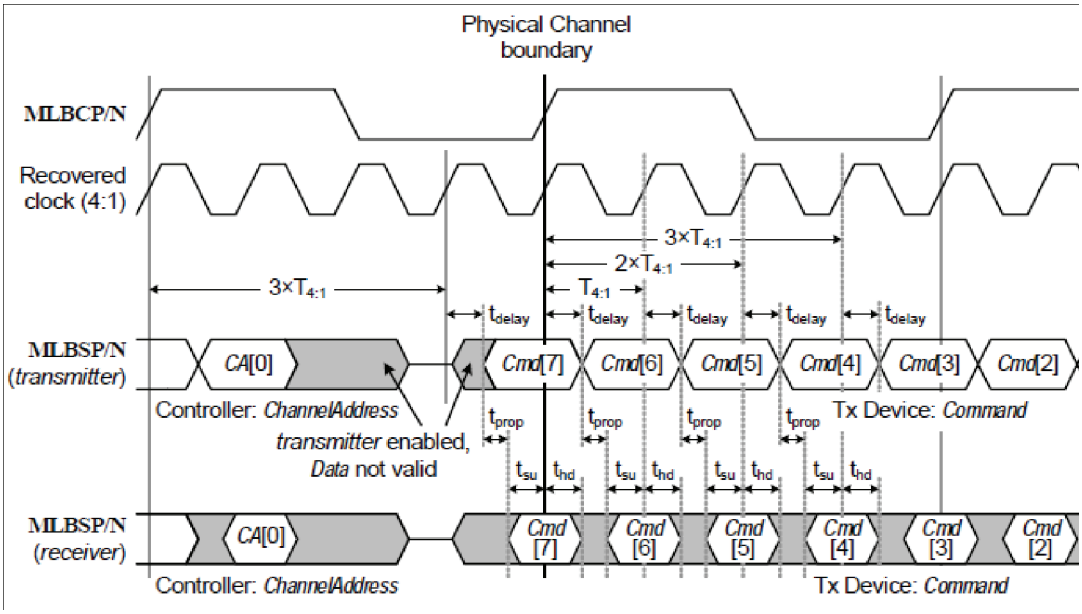

Figure 87. MLB 6-Pin Delay, Setup, and Hold Times

4.11.15 PCIe PHY Parameters

The PCIe interface complies with PCIe specification Gen2 x1 lane and supports the PCI Express 1.1/2.0 standard.

4.11.15.1 PCIE_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 200 Ω. 1% precision resistor on PCIE_REXT pads to ground. It is used for termination impedance calibration.

4.11.16 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 88 depicts the timing of the PWM, and Table 83 lists the PWM timing parameters.

Table 88. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

[1] The UART receiver can tolerate 1/(16 x F_{baud_rate}) tolerance in each bit. But accumulation tolerance in one frame must not exceed 3/(16 x F_{baud_rate}).

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.11.21 USB HSIC Timings

This section describes the electrical information of the USB HSIC port.

NOTE

HSIC is DDR signal, following timing spec is for both rising and falling edge.

4.11.21.1 Transmit Timing

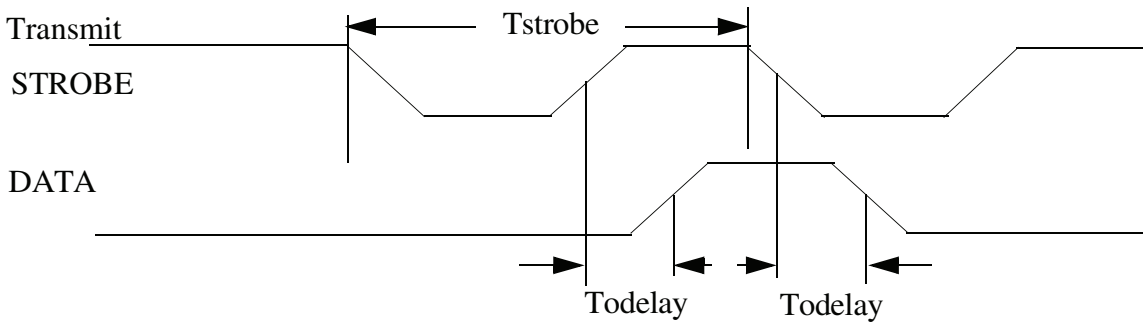

Figure 103. USB HSIC Transmit Waveform

Table 96. USB HSIC Transmit Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	
Todelay	data output delay time	550	1350	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 98 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6Solo/6DualLite Fuse Map document and the System Boot chapter in *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

Table 98. Fuses and Associated Pins Used for Boot

Pin	Direction at Reset	eFuse Name	Details
BOOT_MODE1	Input	N/A	Boot Mode selection
BOOT_MODE0	Input	N/A	Boot Mode Selection

Table 98. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFuse Name	Details
EIM_DA0	Input	BOOT_CFG1[0]	Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
EIM_DA1	Input	BOOT_CFG1[1]	
EIM_DA2	Input	BOOT_CFG1[2]	
EIM_DA3	Input	BOOT_CFG1[3]	
EIM_DA4	Input	BOOT_CFG1[4]	
EIM_DA5	Input	BOOT_CFG1[5]	
EIM_DA6	Input	BOOT_CFG1[6]	
EIM_DA7	Input	BOOT_CFG1[7]	
EIM_DA8	Input	BOOT_CFG2[0]	
EIM_DA9	Input	BOOT_CFG2[1]	
EIM_DA10	Input	BOOT_CFG2[2]	
EIM_DA11	Input	BOOT_CFG2[3]	
EIM_DA12	Input	BOOT_CFG2[4]	
EIM_DA13	Input	BOOT_CFG2[5]	
EIM_DA14	Input	BOOT_CFG2[6]	
EIM_DA15	Input	BOOT_CFG2[7]	
EIM_A16	Input	BOOT_CFG3[0]	
EIM_A17	Input	BOOT_CFG3[1]	
EIM_A18	Input	BOOT_CFG3[2]	
EIM_A19	Input	BOOT_CFG3[3]	
EIM_A20	Input	BOOT_CFG3[4]	
EIM_A21	Input	BOOT_CFG3[5]	
EIM_A22	Input	BOOT_CFG3[6]	
EIM_A23	Input	BOOT_CFG3[7]	
EIM_A24	Input	BOOT_CFG4[0]	
EIM_WAIT	Input	BOOT_CFG4[1]	
EIM_LBA	Input	BOOT_CFG4[2]	
EIM_EB0	Input	BOOT_CFG4[3]	
EIM_EB1	Input	BOOT_CFG4[4]	
EIM_RW	Input	BOOT_CFG4[5]	
EIM_EB2	Input	BOOT_CFG4[6]	
EIM_EB3	Input	BOOT_CFG4[7]	

Table 101. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
RTC_XTALI	D9	VDD_SNVS_CAP					
RTC_XTALO	C9	VDD_SNVS_CAP					
SD1_CLK	D20	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[20]	Input	100 kΩ pull-up
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[18]	Input	100 kΩ pull-up
SD1_DAT0	A21	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[16]	Input	100 kΩ pull-up
SD1_DAT1	C20	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[17]	Input	100 kΩ pull-up
SD1_DAT2	E19	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[19]	Input	100 kΩ pull-up
SD1_DAT3	F18	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[21]	Input	100 kΩ pull-up
SD2_CLK	C21	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[10]	Input	100 kΩ pull-up
SD2_CMD	F19	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[11]	Input	100 kΩ pull-up
SD2_DAT0	A22	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[15]	Input	100 kΩ pull-up
SD2_DAT1	E20	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[14]	Input	100 kΩ pull-up
SD2_DAT2	A23	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[13]	Input	100 kΩ pull-up
SD2_DAT3	B22	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[12]	Input	100 kΩ pull-up
SD3_CLK	D14	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[3]	Input	100 kΩ pull-up
SD3_CMD	B13	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[2]	Input	100 kΩ pull-up
SD3_DAT0	E14	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[4]	Input	100 kΩ pull-up
SD3_DAT1	F14	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[5]	Input	100 kΩ pull-up
SD3_DAT2	A15	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[6]	Input	100 kΩ pull-up
SD3_DAT3	B15	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[7]	Input	100 kΩ pull-up
SD3_DAT4	D13	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[1]	Input	100 kΩ pull-up
SD3_DAT5	C13	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[0]	Input	100 kΩ pull-up
SD3_DAT6	E13	NVCC_SD3	GPIO	ALT5	gpio6.GPIO[18]	Input	100 kΩ pull-up
SD3_DAT7	F13	NVCC_SD3	GPIO	ALT5	gpio6.GPIO[17]	Input	100 kΩ pull-up
SD3_RST	D15	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[8]	Input	100 kΩ pull-up
SD4_CLK	E16	NVCC_NANDF	GPIO	ALT5	gpio7.GPIO[10]	Input	100 kΩ pull-up
SD4_CMD	B17	NVCC_NANDF	GPIO	ALT5	gpio7.GPIO[9]	Input	100 kΩ pull-up
SD4_DAT0	D18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[8]	Input	100 kΩ pull-up
SD4_DAT1	B19	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[9]	Input	100 kΩ pull-up
SD4_DAT2	F17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[10]	Input	100 kΩ pull-up

Table 102. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

	AE	AD
1	GND	DRAM_D5
2	DRAM_D1	DRAM_D0
3	DRAM_SDQS0	DRAM_SDQS0_B
4	DRAM_D7	GND
5	DRAM_D9	DRAM_D8
6	DRAM_SDQS1_B	DRAM_SDQS1
7	DRAM_D11	GND
8	DRAM_SDQS2_B	DRAM_SDQS2
9	DRAM_D24	DRAM_D29
10	DRAM_DQM3	GND
11	DRAM_D26	DRAM_D30
12	DRAM_A9	DRAM_A12
13	DRAM_A5	GND
14	DRAM_SDCLK_1_B	DRAM_SDCLK_1
15	DRAM_SDCLK_0_B	DRAM_SDCLK_0
16	DRAM_CAS	GND
17	ZQPAD	DRAM_CS1
18	NC	NC
19	NC	GND
20	NC	NC
21	NC	NC
22	NC	GND
23	NC	NC
24	NC	NC
25	GND	NC
	AE	AD

Table 103 shows the 21 x 21 mm, 0.8 mm pitch ball map for the i.MX 6DualLite.

Table 103. 21 x 21 mm, 0.8 mm Pitch Ball Map

	D	C	B	A	
1	CSI_D1M	GND	PCIE_RXM	NC	1
2	CSI_D1P	JTAG_TRSTB	PCIE_RXP	PCIE_REXT	2
3	GND	JTAG_TMS	PCIE_TXP	PCIE_TXM	3
4	CSI_REXT	GND	GND	GND	4
5	CLK2_P	CLK2_N	VDD_FA	FA_ANA	5
6	GND	GND	USB_OTG_DN	USB_OTG_DP	6
7	CLK1_P	CLK1_N	XTALO	XTALI	7
8	GND	GPANAIO	USB_OTG_CHD_B	GND	8
9	RTC_XTALI	RTC_XTALO	MLB_SP	MLB_SN	9
10	USB_H1_VBUS	GND	MLB_DN	MLB_DP	10
11	PMIC_ON_REQ	POR_B	MLB_CP	MLB_CN	11
12	ONOFF	BOOT_MODE0	NC	NC	12
13	SD3_DAT4	SD3_DAT5	SD3_CMD	GND	13
14	SD3_CLK	NC	NC	NC	14
15	SD3_RST	NANDF_CLE	SD3_DAT3	SD3_DAT2	15
16	NANDF_CS3	NANDF_CS1	NANDF_RB0	NANDF_ALE	16
17	NANDF_D3	NANDF_D1	SD4_CMD	NANDF_CS2	17
18	SD4_DAT0	NANDF_D7	NANDF_D5	NANDF_D0	18
19	SD4_DAT7	SD4_DAT5	SD4_DAT1	NANDF_D4	19
20	SD1_CLK	SD1_DAT1	SD4_DAT6	SD4_DAT3	20
21	RGMII_TXC	SD2_CLK	SD1_CMD	SD1_DAT0	21
22	RGMII_RX_CTL	RGMII_TD0	SD2_DAT3	SD2_DAT0	22
23	RGMII_RD3	RGMII_TX_CTL	RGMII_RD1	SD2_DAT2	23
24	EIM_D18	RGMII_RD0	RGMII_RD2	RGMII_TD3	24
25	EIM_D23	EIM_D16	RGMII_RXC	GND	25
	D	C	B	A	

Table 103. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

Y	W	V	U	T	R	P	N
LVDS1_TX0_N	LVDS0_TX3_P	LVDS0_TX2_P	LVDS0_TX0_P	GPIO_2	GPIO_17	CSI0_PIXCLK	CSI0_DAT4
LVDS1_TX0_P	LVDS0_TX3_N	LVDS0_TX2_N	LVDS0_TX0_N	GPIO_9	GPIO_16	CSI0_DAT5	CSI0_VSYNC
LVDS1_CLK_N	GND	LVDS0_CLK_P	LVDS0_TX1_P	GPIO_6	GPIO_7	CSI0_DATA_EN	CSI0_DAT7
LVDS1_CLK_P	KEY_ROW2	LVDS0_CLK_N	LVDS0_TX1_N	GPIO_1	GPIO_5	CSI0_MCLK	CSI0_DAT6
GND	KEY_COL0	KEY_ROW4	KEY_COL3	GPIO_0	GPIO_8	GPIO_19	CSI0_DAT9
DRAM_RESET	KEY_COL2	KEY_ROW0	KEY_ROW1	KEY_COL4	GPIO_4	GPIO_18	CSI0_DAT8
DRAM_D20	GND	NVCC_LVDS2P5	KEY_COL1	KEY_ROW3	GPIO_3	NVCC_GPIO	NVCC_CSI
DRAM_D21	GND	GND	GND	GND	GND	GND	GND
DRAM_D19	GND	NVCC_DRAM	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN
DRAM_D25	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDSOC_CAP	GND	GND
DRAM_SDCKE0	GND	NVCC_DRAM	GND	GND	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
DRAM_A15	GND	NVCC_DRAM	GND	GND	GND	GND	NC
DRAM_A7	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
DRAM_A3	DRAM_A4	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_IN	VDDARM_IN	VDDARM_IN
DRAM_SDBA1	GND	NVCC_DRAM	GND	GND	GND	GND	GND
DRAM_CS0	GND	NVCC_DRAM	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN
DRAM_D36	GND	NVCC_DRAM	GND	GND	GND	VDDPU_CAP	VDDPU_CAP
DRAM_D37	GND	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	GND	GND
DRAM_D40	GND	GND	GND	GND	NVCC_ENET	NVCC_LCD	DI0_DISP_CLK
DRAM_D44	ENET_TXD1	ENET_MDC	ENET_TXD0	DISP0_DAT21	DISP0_DAT13	DISP0_DAT4	DI0_PIN3
DRAM_DQM7	ENET_RXD0	ENET_TX_EN	ENET_CRS_DV	DISP0_DAT16	DISP0_DAT10	DISP0_DAT3	DI0_PIN15
DRAM_D59	ENET_RXD1	ENET_REF_CLK	DISP0_DAT20	DISP0_DAT15	DISP0_DAT8	DISP0_DAT1	EIM_BCLK
DRAM_D62	ENET_RX_ER	ENET_MDIO	DISP0_DAT19	DISP0_DAT11	DISP0_DAT6	DISP0_DAT2	EIM_DA14
GND	DISP0_DAT23	DISP0_DAT22	DISP0_DAT17	DISP0_DAT12	DISP0_DAT7	DISP0_DAT0	EIM_DA15
DRAM_D58	DRAM_D63	DISP0_DAT18	DISP0_DAT14	DISP0_DAT9	DISP0_DAT5	DI0_PIN4	DI0_PIN2
Y	W	V	U	T	R	P	N